



Crystalfontz America, Incorporated

CHARACTER LCD MODULE SPECIFICATIONS



| | |
|---------------------------|--|
| Crystalfontz Model Number | CFAH0802A-GYH-JT |
| Hardware Version | Revision C |
| Data Sheet Version | Revision 1.0, July 2008 |
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REVISION HISTORY

| HARDWARE | |
|------------|--|
| 2008/07/31 | Current hardware version: vC This new “-JT” module replaces the discontinued “-JP” module. |

| DATA SHEET | |
|------------|--|
| 2008/07/31 | Current Data Sheet version: v1.0 New Data Sheet. |

The Fine Print

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MAIN FEATURES

- ❑ 8 characters by 2 lines LCD has a large display area in a compact 58.0 (W) x 32.0 (H) x 13.5 (D) millimeter package (2.28" (W) x 1.26" (H) x 0.53" (D)).
- ❑ 4-bit or 8-bit parallel interface.
- ❑ Standard Hitachi HD44780 equivalent controller.
- ❑ Green array LED backlight with STN, positive, yellow-green, transfective mode LCD (displays dark characters on green background).
- ❑ Wide temperature operation: -20°C to +70°C.
- ❑ Direct sunlight readable.
- ❑ RoHS compliant.

MODULE CLASSIFICATION INFORMATION







CFA H 08 02 A - G Y H - J T *
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

| | | |
|---|---|--|
| ① | Brand | CrystalFontz America, Inc. |
| ② | Display Type | H – Character |
| ③ | Number of Characters (Width) | 8 Characters |
| ④ | Number of Lines (Height) | 2 Lines |
| ⑤ | Model Identifier | A |
| ⑥ | Backlight Type & Color | G – LED, green |
| ⑦ | Fluid Type, Image (Positive or Negative), & LCD Glass Color | Y – STN, positive, yellow-green |
| ⑧ | Polarizer Film Type, Wide (WT) Temperature Range, & Viewing Angle (O'clock) | H – Transflective, WT, 6:00 ¹ |
| ⑨ | Character Set (CGROM) | J – English and Japanese fonts |
| ⑩ | Controller | T – Sitronix ST7066U |
| ⑪ | Special Codes | * – May have additional manufacturer's codes at this location. |

¹Note: For more information on Viewing Angle, see [Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles \(Pg. 17\)](#).



ORDERING INFORMATION

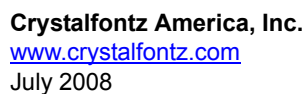
| PART NUMBER | FLUID | LCD GLASS COLOR | IMAGE | POLARIZER FILM | BACKLIGHT COLOR/TYPE |
|---|-------|-----------------|----------|----------------|--|
| CFAH0802A-GYH-JT | STN | yellow-green | positive | transflective | green LED  |
| <i>Additional variants (same form factor, different LCD mode or backlight):</i> | | | | | |
| CFAH0802A-GGH-JT | STN | grey | positive | transflective | green LED  |
| CFAH0802A-TMI-JT | STN | blue | negative | transmissive | white LED  |
| CFAH0802A-TTI-JT | FSTN | near-black | negative | transmissive | white LED  |
| CFAH0802A-YMI-JT | STN | blue | negative | transmissive | yellow-green LED  |
| CFAH0802A-YYH-JT | STN | yellow-green | positive | transflective | yellow-green LED  |



MECHANICAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

| ITEM | SIZE |
|--------------------------------|-----------------------------------|
| Number of Characters and Lines | 8 Characters x 2 Lines |
| Module Dimensions | 58.0 (W) x 32.0 (H) x 13.5 (D) mm |
| Viewing Area | 38.0 (W) x 16.0 (H) mm |
| Active Area | 27.81 (W) x 11.5 (H) mm |
| Character Size | 2.96 (W) x 5.56 (H) mm |
| Character Pitch | 3.55 (W) x 5.94 (H) mm |
| Dot Size | 0.56 (W) x 0.66 (H) mm |
| Dot Pitch | 0.60 (W) x 0.70 (H) mm |
| Weight | 21 grams (typical) |



Tolerance is ± 0.3 mm unless specified.

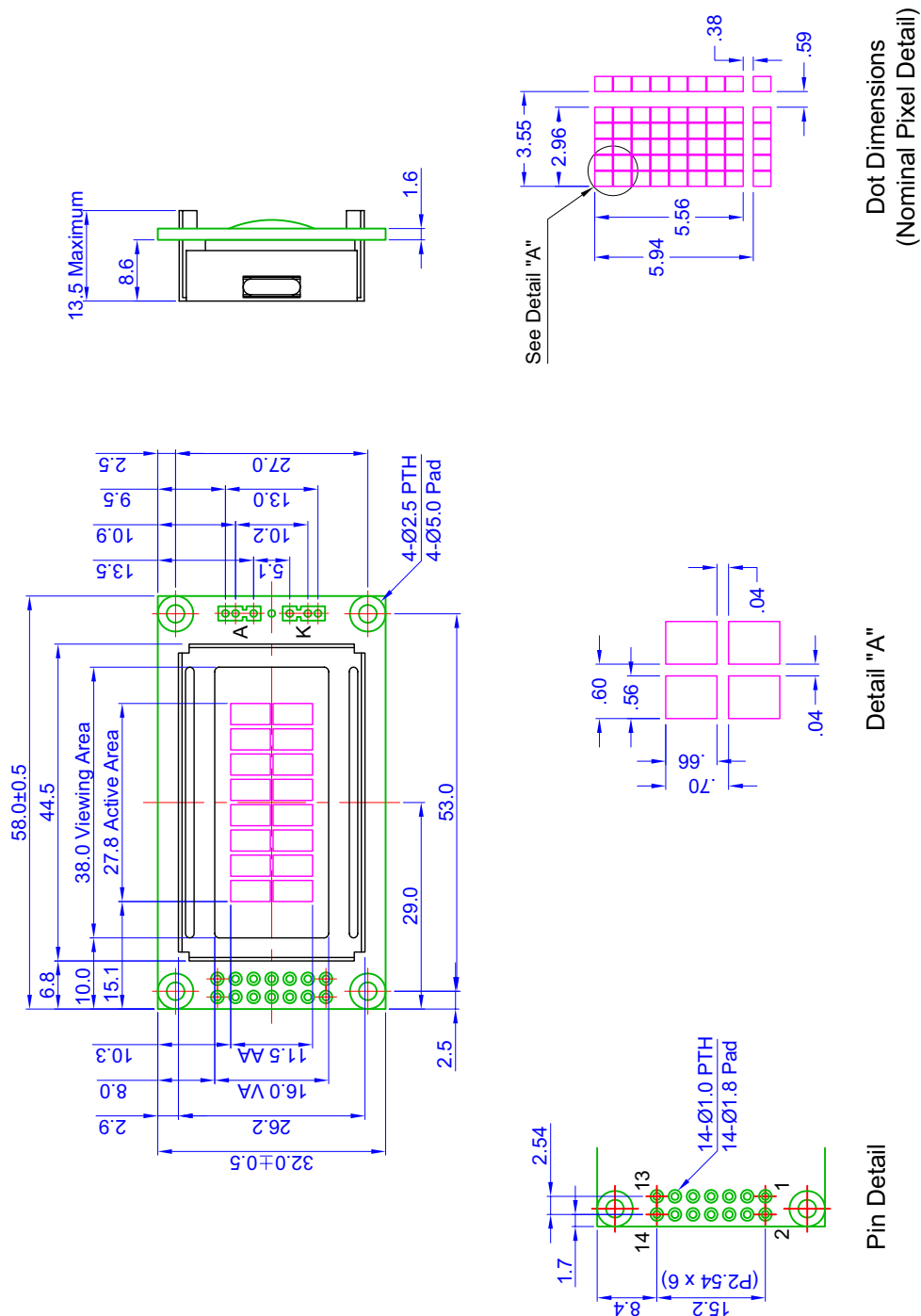


Figure 1. Module Outline Drawing



ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM

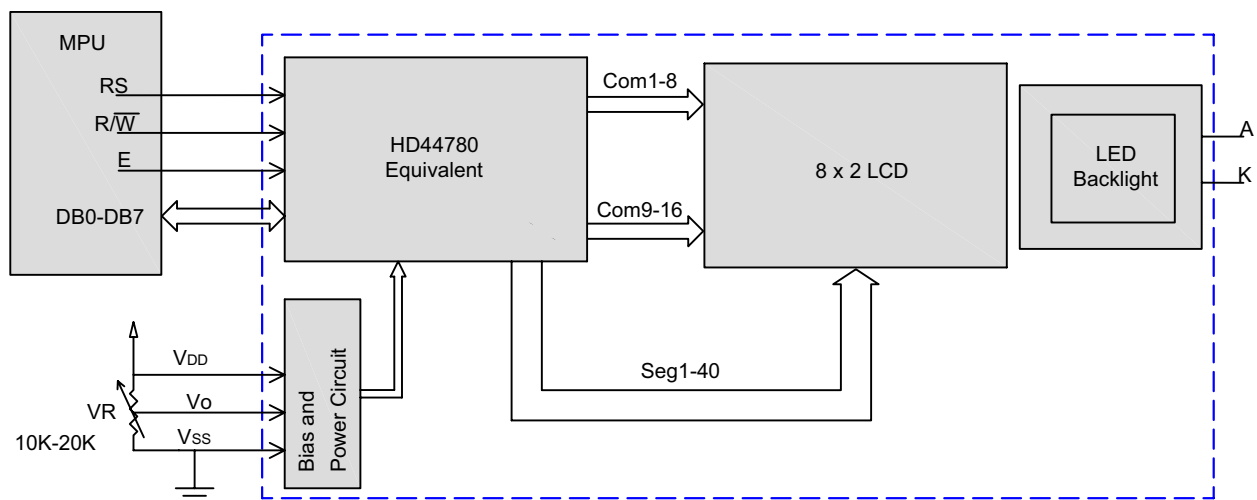


Figure 2. System Block Diagram



DRIVING METHOD

| DRIVING METHOD | SPECIFICATION |
|----------------|---------------|
| Duty | 1/16 |
| Bias | 1/5 |

ABSOLUTE MAXIMUM RATINGS

| ABSOLUTE MAXIMUM RATINGS | SYMBOL | MINIMUM | MAXIMUM |
|--|-------------------|----------|----------|
| Operating Temperature* | T_{OP} | -20°C | +70°C |
| Storage Temperature* | T_{ST} | -30°C | +80°C |
| Input Voltage | V_I | V_{SS} | V_{DD} |
| Supply Voltage for Logic | $V_{DD} - V_{SS}$ | -0.3v | +7v |
| Supply Voltage for LCD | $V_{DD} - V_O$ | -0.3v | +13v |
| <i>*Note: Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.</i> | | | |

DC CHARACTERISTICS (5V AND 3.3V OPERATION)

| 5V OPERATION | | | | | | | |
|----------------------|--|---------------------------|-------------------|---------|---------|----------|---|
| PART | DC CHARACTERISTICS (4.5 to 5.5 volts) | TEST CONDITION | SYMBOL | MINIMUM | TYPICAL | MAXIMUM | NOTES |
| Controller and Board | Supply Voltage for Logic | | $V_{DD} - V_{SS}$ | +4.5v | +5.0v | +5.5v | |
| | Input High Voltage | $V_{DD} = 5V$ | V_{IH} | +3.5v | | V_{DD} | Pins: E, RS, R/W, DB0 - DB7 |
| | Input Low Voltage | | V_{IL} | | | +0.6v | |
| | Output High Voltage | $V_{DD} = 5V$ | V_{OH} | +3.7v | | | $I_{OH} = -0.1 \text{ mA}$ Pins: DB0 - DB7 |
| | Output Low Voltage | | V_{OL} | | | +0.4v | $I_{OL} = 0.1 \text{ mA}$ Pins: DB0 - DB7 |
| | Supply Current | without backlight | I_{DD} | | 1.2 mA | | |
| LCD Glass | Supply Voltage for Driving LCD | $T_A = -20^\circ\text{C}$ | $V_{DD} - V_O$ | | | +4.2v | |
| | | $T_A = +25^\circ\text{C}$ | | | +3.8v | | |
| | | $T_A = +70^\circ\text{C}$ | | +3.6v | | | |

This is a summary of the module's major operating parameters. For detailed information, see [APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET \(Pg. 30\)](#).

| 3.3V OPERATION | | | | | | | |
|----------------------------|--|----------------------|-------------------|---------|---------|----------|--|
| PART | DC CHARACTERISTICS (2.7 to 4.5 volts) | TEST CONDITION | SYMBOL | MINIMUM | TYPICAL | MAXIMUM | NOTES |
| Controller and Board | Supply Voltage for Logic | | $V_{DD} - V_{SS}$ | +2.7v | +3.3v | +4.5v | |
| | Input High Voltage | $V_{DD} = 3.3V$ | V_{IH} | +2.3v | | V_{DD} | Pins: E, RS, $\overline{R/W}$, DB0 - DB7 |
| | Input Low Voltage | | V_{IL} | | | +0.6v | |
| | Output High Voltage | $V_{DD} = 3.3V$ | V_{OH} | +2.4v | | | $I_{OH} = -0.1\text{ mA}$ Pins: DB0 - DB7 |
| | Output Low Voltage | | V_{OL} | | | +0.4v | $I_{OL} = 0.1\text{ mA}$ Pins: DB0 - DB7 |
| | Supply Current | without backlight | I_{DD} | | 1.2 mA | | |
| LCD Glass | Supply Voltage for Driving LCD | TA = -20°C | $V_{DD} - V_O$ | | | +4.2v | |
| | | TA = +25°C | | | +3.8v | | |
| | | TA = +70°C | | +3.6v | | | |

This is a summary of the module's major operating parameters. For detailed information see [APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET \(Pg. 30\)](#).

For more information about 3.3v operation, please see [APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION \(Pg. 28\)](#).



DETAILS OF INTERFACE PIN FUNCTIONS

| PIN | SIGNAL | LEVEL | DIRECTION | DESCRIPTION |
|---|-------------------|----------|-----------|--|
| 1 | V _{SS} | 0v | | Ground |
| 2 | V _{DD} | +5.0v | | Supply voltage for logic |
| 3 | V _O | variable | | Supply voltage for driving LCD is V _O = +1v typical at V _{DD} = +5v which gives a V _{LCD} = (V _{DD} - V _O) = +4v |
| 4 | RS | H/L | I | Register selection input. H: Data register (for read and write) L: Instruction code (for write) |
| 5 | R/ \overline{W} | H/L | I | H: Read (Host←Module) L: Write (Host→Module) |
| 6 | E | H, H→L | I | Read/write enable signal. H: Read data is enabled by a high level. H→L: Write data is latched on the falling edge. |
| 7 | DB0 | H/L | I/O | Data bit 0 |
| 8 | DB1 | H/L | I/O | Data bit 1 |
| 9 | DB2 | H/L | I/O | Data bit 2 |
| 10 | DB3 | H/L | I/O | Data bit 3 |
| 11 | DB4 | H/L | I/O | Data bit 4 |
| 12 | DB5 | H/L | I/O | Data bit 5 |
| 13 | DB6 | H/L | I/O | Data bit 6 |
| 14 | DB7 | H/L | I/O | Data bit 7 |
| For backlight connections, please refer to LED Backlight Characteristics (Pg. 18) . | | | | |



QUICK REFERENCE FOR PIN FUNCTIONS (FRONT & BACK PHOTOS)

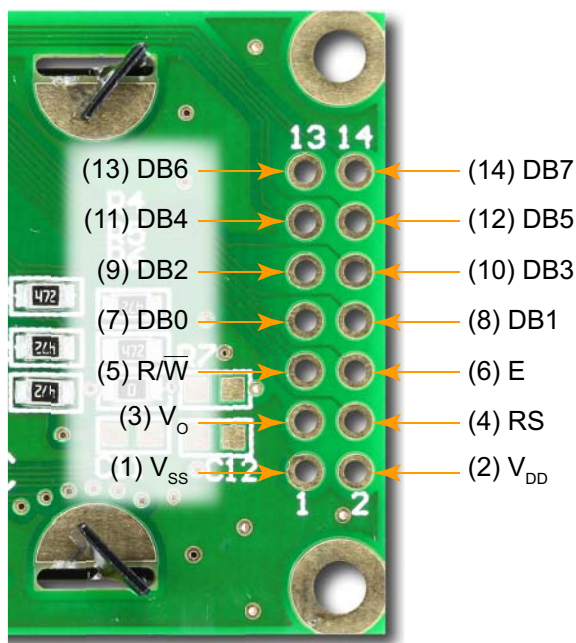


Figure 3. Back View of Pins (Labeled)

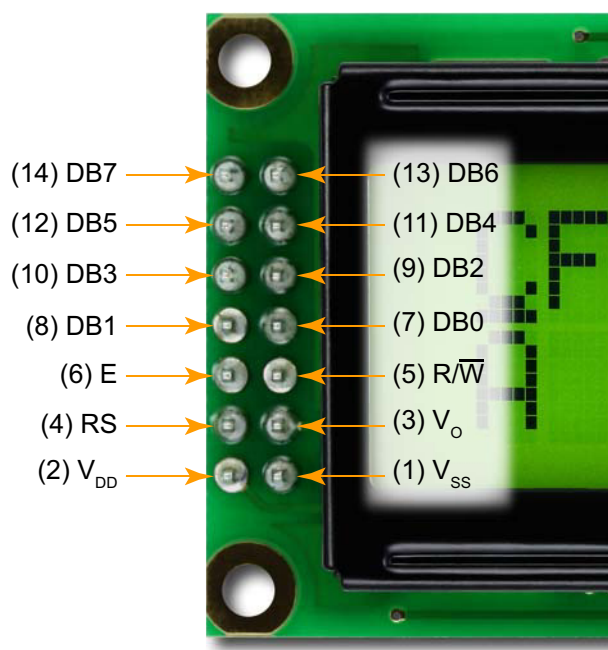


Figure 4. Front View of Pins (Labeled)



TYPICAL V_O CONNECTIONS FOR DISPLAY CONTRAST

Adjust V_O to +1v ($V_{LCD} = +4v$) as an initial setting. When the module is operational, readjust V_O for optimal display appearance.

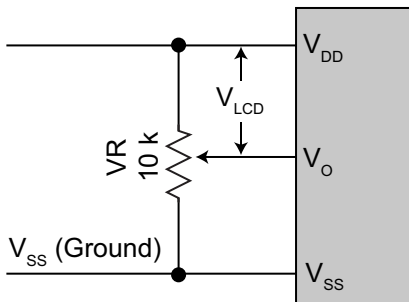


Figure 5. Typical V_O Connections

We recommend allowing field adjustment of V_O for all designs. The optimal value for V_O will change with temperature, variations in V_{DD} , and viewing angle. V_O will also vary module-to-module and batch-to-batch due to normal manufacturing variations.

Ideally, adjustments to V_O should be available to the end user so each user can adjust the display to the optimal contrast for their required viewing conditions. At a minimum, your design should allow V_O to be adjusted as part of your product's final test.

Although a potentiometer is shown as a typical connection, V_O can be driven by your microcontroller, either by using a DAC or a filtered PWM. Displays that require V_O to be negative may need a level-shifting circuit. Please do not hesitate to contact CrystalFontz application support for design assistance on your application.

ESD (ELECTRO-STATIC DISCHARGE) SPECIFICATIONS

This circuitry is industry standard CMOS logic and is susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. For more information, see [CARE AND HANDLING PRECAUTIONS \(Pg. 23\)](#).



OPTICAL SPECIFICATIONS

OPTICAL CHARACTERISTICS

| ITEM | SYMBOL | CONDITION | MINIMUM | TYPICAL | MAXIMUM |
|--|--------------|-------------|---------|---------|---------|
| Viewing Angle (6 o'clock) (Vertical, Horizontal) | (V) θ | CR \geq 2 | 10° | | 40° |
| | (H) ϕ | CR \geq 2 | -40° | | 40° |
| Contrast Ratio | CR | | | 3 | |
| LCD Response Time* | T rise | Ta = 25°C | | 150 ms | 200 ms |
| | T fall | Ta = 25°C | | 150 ms | 200 ms |
| *Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again. | | | | | |

OPTICAL DEFINITIONS

- Operating Voltage (V_{LCD}): V_{OP}
- Viewing Angle
 - Vertical (V) θ : 0°
 - Horizontal (H) ϕ : 0°
- Frame Frequency: 64 Hz
- Driving Waveform: 1/16 Duty, 1/5 Bias
- Ambient Temperature (Ta): 25°C



Definition of Operation Voltage (Vop)

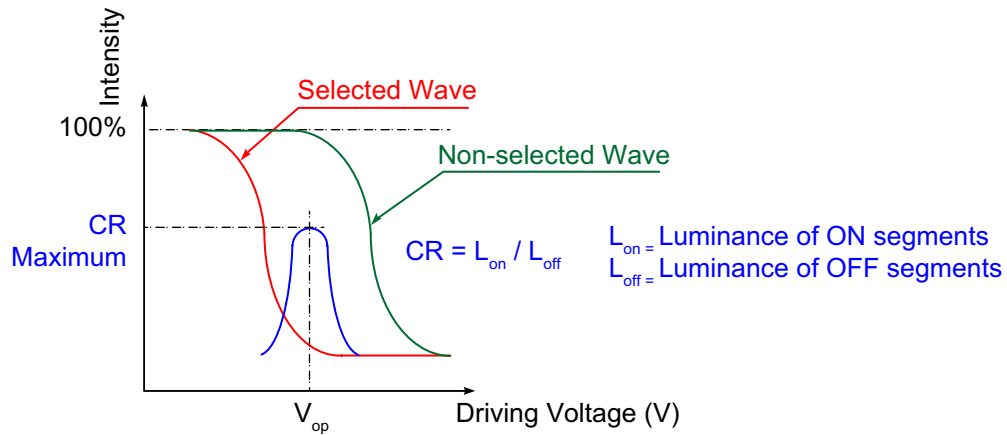


Figure 6. Definition of Operation Voltage (V_{OP}) (Positive)

Definition of Response Time (T_r , T_f)

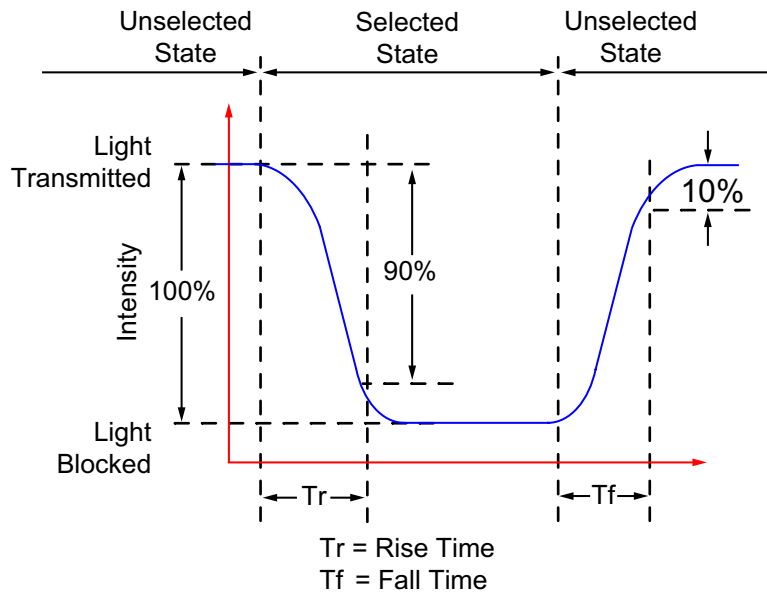


Figure 7. Definition of Response Time (T_r , T_f) (Positive)



Definition of Vertical and Horizontal Viewing Angles ($CR \geq 2$)

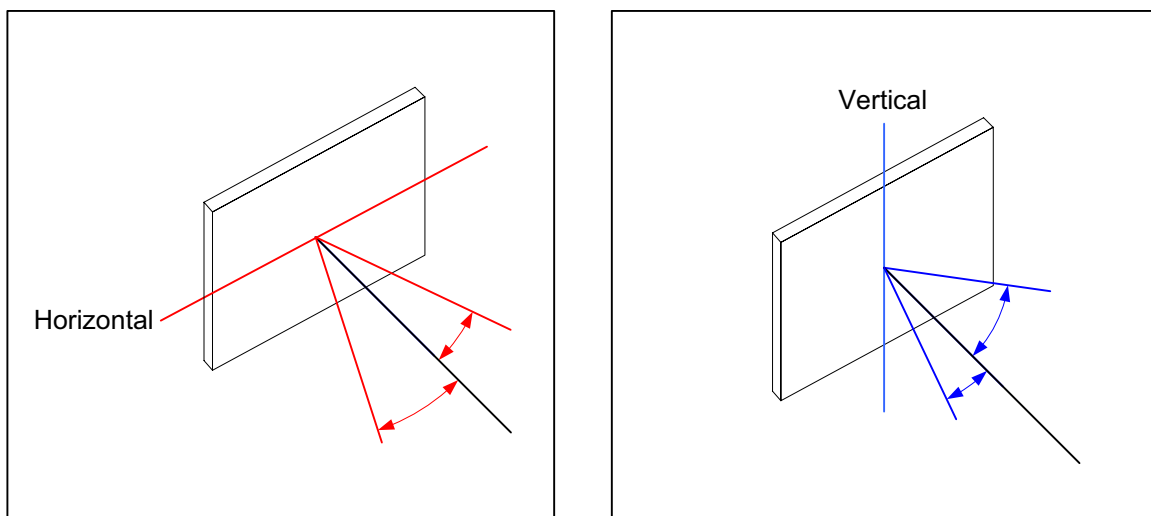


Figure 8. Definition of Horizontal and Vertical Viewing Angles ($CR \geq 2$)

Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles

This module has a 6:00 o'clock viewing angle. A 6:00 o'clock viewing angle is a bottom viewing angle like what you would see when you look at a cell phone or calculator. A 12:00 o'clock viewing angle is a top viewing angle like what you would see when you look at the gauges in a golf cart or airplane.

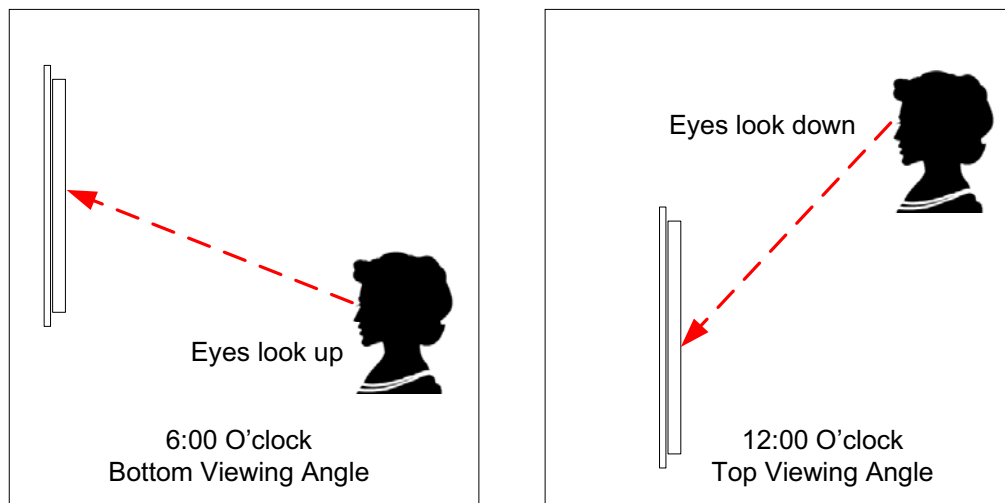


Figure 9. Definition of 6:00 O'Clock and 12:00 O'Clock Viewing Angles



LED BACKLIGHT CHARACTERISTICS

The CFAH0802A-GYH-JT uses an LED backlight. LED backlights are easy to use, but they are also easily damaged by abuse.

NOTE

Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

LEDs are “current” devices. The important aspect of driving an LED is the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor in line from a voltage source will work well in most applications and is much less complex than a current source.

You need to know what the forward voltage of the LEDs is so you can calculate the current limiting resistor (R_{LIMIT}). The forward voltage will vary slightly from display to display.

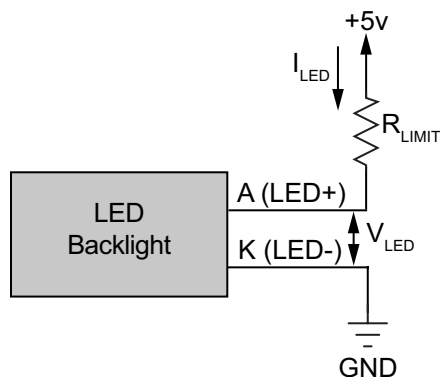


Figure 10. Typical LED Backlight Connections for “Always On”

The equation to calculate R_{LIMIT} is:

$$R_{LIMIT} \text{ (minimum)} = \frac{V_{DD} \text{ (Supply Voltage)} - V_{LED} \text{ (Typical LED Forward Voltage)}}{I_{LED} \text{ (Typical LED Forward Current)}}$$

The specific R_{LIMIT} calculation for the CFAH0802A-GYH-JT at $V_{DD} = +5v$ is:

$$R_{LIMIT} = \frac{5v - 4.2v}{0.07 \text{ A}} = 11.43\Omega \text{ (minimum)}$$



The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

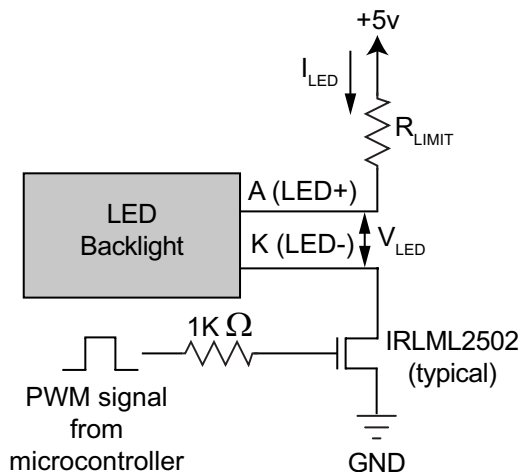


Figure 11. Example of LED Backlight Connections for PWM Dimming

| Backlight Characteristics <i>Dark dots on green background</i> | | | |
|---|----------------------|---------|---------|
| PARAMETER | MINIMUM | TYPICAL | MAXIMUM |
| Forward Current (I_{LED}) $V = 4.2v$ | | 70 mA | 140 mA |
| Forward Voltage (V_{LED}) | | +4.2v | +4.6v |
| Reverse Voltage (V_R) | | | +8v |
| Luminous Intensity* (I_V) $I_{LED} = 70 \text{ mA}$ | 10 cd/m ² | | |
| Wavelength* (λ) $I_{LED} = 70 \text{ mA}$ | | 570 nm | |
| *Direct measurement of backlight—the backlight is not measured through the LCD. | | | |



LCD CONTROLLER INTERFACE

This module uses a Sitronix ST7066U controller. The Sitronix ST7066U is compatible with the industry standard Hitachi HD44780 controller. Software written for modules that use the HD44780 should work without modification.

For your reference, we added [APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET \(Pg. 30\)](#) to this Data Sheet.

DISPLAY POSITION DDRAM ADDRESS

The following table shows the relationship between the controller's addresses and the corresponding character location on the module.

| | | COLUMN | | | | | | | |
|-----|---|--------|------|------|------|------|------|------|------|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| ROW | 0 | 0x00 | 0x01 | 0x02 | 0x03 | 0x04 | 0x05 | 0x06 | 0x07 |
| | 1 | 0x40 | 0x41 | 0x42 | 0x43 | 0x44 | 0x45 | 0x46 | 0x47 |



CHARACTER GENERATOR ROM (CGROM)

To find the code for a given character, add the two numbers that are shown in bold for its row and column. For example, the lowercase “h” is in the column labeled “96₁₀” and in the row labeled “8₁₀”. So you would add 96 + 8 to get 104. When you send a byte with the value of 104 to the display, then a lowercase “h” will be shown. (See [APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET \(Pg. 30\)](#)).

| <div>upper lower 4 bits 4 bits</div> | 0 ₁₀ 0000 ₂ | 16 ₁₀ 0001 ₂ | 32 ₁₀ 0010 ₂ | 48 ₁₀ 0011 ₂ | 64 ₁₀ 0100 ₂ | 80 ₁₀ 0101 ₂ | 96 ₁₀ 0110 ₂ | 112 ₁₀ 0111 ₂ | 128 ₁₀ 1000 ₂ | 144 ₁₀ 1001 ₂ | 160 ₁₀ 1010 ₂ | 176 ₁₀ 1011 ₂ | 192 ₁₀ 1100 ₂ | 208 ₁₀ 1101 ₂ | 224 ₁₀ 1110 ₂ | 240 ₁₀ 1111 ₂ |
|--|--------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|--|--|--|--|--|--|--|--|--|
| 0 ₁₀ 0000 ₂ | CGRAM [0] | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |
| 1 ₁₀ 0001 ₂ | CGRAM [1] | | ! | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E |
| 2 ₁₀ 0010 ₂ | CGRAM [2] | | " | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E |
| 3 ₁₀ 0011 ₂ | CGRAM [3] | | # | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 4 ₁₀ 0100 ₂ | CGRAM [4] | | \$ | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | G |
| 5 ₁₀ 0101 ₂ | CGRAM [5] | | % | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | G | H |
| 6 ₁₀ 0110 ₂ | CGRAM [6] | | & | 6 | 7 | 8 | 9 | A | B | C | D | E | F | G | H | I |
| 7 ₁₀ 0111 ₂ | CGRAM [7] | | ' | 7 | 8 | 9 | A | B | C | D | E | F | G | H | I | J |
| 8 ₁₀ 1000 ₂ | | | (| 8 | 9 | A | B | C | D | E | F | G | H | I | J | K |
| 9 ₁₀ 1001 ₂ | | |) | 9 | A | B | C | D | E | F | G | H | I | J | K | L |
| 10 ₁₀ 1010 ₂ | | | * | A | B | C | D | E | F | G | H | I | J | K | L | M |
| 11 ₁₀ 1011 ₂ | | | + | B | C | D | E | F | G | H | I | J | K | L | M | N |
| 12 ₁₀ 1100 ₂ | | | , | C | D | E | F | G | H | I | J | K | L | M | N | O |
| 13 ₁₀ 1101 ₂ | | | - | D | E | F | G | H | I | J | K | L | M | N | O | P |
| 14 ₁₀ 1110 ₂ | | | . | E | F | G | H | I | J | K | L | M | N | O | P | Q |
| 15 ₁₀ 1111 ₂ | | | / | F | G | H | I | J | K | L | M | N | O | P | Q | R |

Figure 12. Character Generator ROM (CGROM)



MODULE RELIABILITY AND LONGEVITY

MODULE RELIABILITY

| ITEM | SPECIFICATION |
|-----------------------------------|-----------------------------------|
| LCD including green LED backlight | 50,000 to 100,000 hours (typical) |

MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

Crystalfontz is committed to making all of our LCD modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module it replaces. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *LCD fluid, polarizers, or the LCD manufacturing process.* These items may change the appearance of the display, requiring an adjustment to V_O (See [Typical \$V_O\$ Connections for Display Contrast \(Pg. 14\)](#)).
- *Backlight LEDs.* Brightness may be affected (perhaps the new LEDs have better efficiency) or the current they draw may change (new LEDs may have a different VF).
- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's webpage as soon as possible. If interested, you can subscribe to future part change notifications.



CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- The exposed surface of the LCD “glass” is actually a polarizer laminated on top of the glass. To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the tab of the metal holder or make connections to it.
- Solder only to the I/O terminals. Use care when removing solder—it is possible to damage the PCB.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.

AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, and tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

IF LCD PANEL BREAKS

- If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or eyes.
- If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Do not eat the LCD panel.

CLEANING

The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.

- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.



OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product." This module is not "user friendly" and connecting them to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at <http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257>.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
 - At lower temperatures of this range, response time is delayed.
 - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING



- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated CrystalFontz LCD modules at an approved facility.



APPENDIX A: QUALITY ASSURANCE STANDARDS

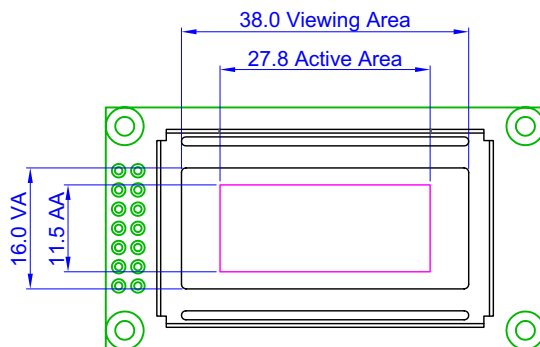
INSPECTION CONDITIONS

- Environment
 - Temperature: $25 \pm 5^{\circ}\text{C}$
 - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
 - Source lighting: two 20-Watt or one 40-Watt fluorescent light
 - Display adjusted for best contrast
 - Viewing distance: 30 ± 5 cm (about 12 inches)
 - Viewing angle: inspect at 45° angle of vertical line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our LCD modules as accurately as possible. For the photos, we adjust the backlight (if any) and contrast for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

DEFINITION OF ACTIVE AREA AND VIEWING AREA



ACCEPTANCE SAMPLING

| DEFECT TYPE | AQL* |
|---|--------------|
| Major | $\leq .65\%$ |
| Minor | $< 1.0\%$ |
| * Acceptable Quality Level: maximum allowable error rate or variation from standard | |

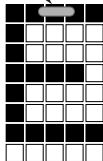
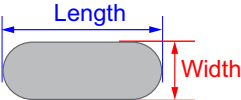
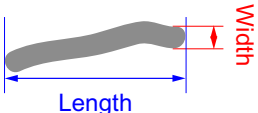


DEFECTS CLASSIFICATION

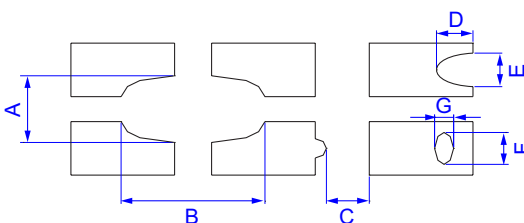
Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

ACCEPTANCE STANDARDS

| # | DEFECT TYPE | CRITERIA | | | MAJOR / MINOR |
|---|--|---|---------------------------------------|----------------|---------------|
| 1 | Electrical defects | 1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications. | | | Major |
| 2 | Viewing area defect | Viewing area does not meet specifications. | | | Major |
| 3 | Contrast adjustment defect | Contrast adjustment fails or malfunctions. | | | Major |
| 4 | Blemishes or foreign matter on display segments |  | Defect Size | Acceptable Qty | Minor |
| | | | ≤0.30 mm | 3 | |
| | | | ≤2 defects within 10 mm of each other | | |
| 5 | Blemishes or foreign matter outside of display segments | Defect Size = (Width + Length)/2  | Defect Size | Acceptable Qty | Minor |
| | | | ≤0.15 mm | Ignore | |
| | | | 0.15 to 0.20 mm | 3 | |
| | | | 0.20 to 0.25 mm | 2 | |
| | | | > 0.30 mm | 1 | |
| 6 | Dark lines or scratches in display area  | Defect Width | Defect Length | Acceptable Qty | Minor |
| | | ≤0.03 mm | ≤3.0 mm | 3 | |
| | | 0.03 to 0.05 | ≤2.0 mm | 2 | |
| | | 0.05 to 0.08 | ≤2.0 mm | 1 | |
| | | 0.08 to 0.10 | ≤3.0 mm | 0 | |
| | | ≥0.10 | >3.0 mm | 0 | |



| # | DEFECT TYPE | CRITERIA | | MAJOR / MINOR |
|----|--|---|---|---------------|
| 7 | Bubbles between polarizer film and glass | Defect Size | Acceptable Qty | Minor |
| | | ≤0.20 mm | Ignore | |
| | | 0.20 to 0.40 mm | 3 | |
| | | 0.40 to 0.60 mm | 2 | |
| | | ≥0.60 mm | 0 | |
| 8 | Display pattern defect |  | | Minor |
| | | Dot Size | Acceptable Qty | |
| | | $((A+B)/2) \leq 0.20 \text{ mm}$ | ≤ 3 total defects ≤ 2 pinholes per digit | |
| | | $C > 0 \text{ mm}$ | | |
| | | $((D+E)/2) \leq 0.25 \text{ mm}$ | | |
| | | $((F+G)/2) \leq 0.25 \text{ mm}$ | | |
| 9 | Backlight defects | 1. Light fails or flickers. (Major) 2. Color and luminance do not correspond to specifications. (Major) 3. Exceeds standards for display's blemishes, foreign matter, dark lines or scratches. (Minor) | | See list ← |
| 10 | PCB defects | 1. Oxidation or contamination on connectors.* 2. Wrong parts, missing parts, or parts not in specification.* 3. Jumpers set incorrectly. (Minor) 4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. (Minor) *Minor if display functions correctly. Major if the display fails. | | See list ← |
| 11 | Soldering defects | 1. Unmelted solder paste. 2. Cold solder joints, missing solder connections, or oxidation.* 3. Solder bridges causing short circuits.* 4. Residue or solder balls. 5. Solder flux is black or brown. *Minor if display functions correctly. Major if the display fails. | | Minor |



APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION

This module can be used with a 3.3v power supply. In order to meet the requirements of V_{LCD} , you must provide a negative voltage source for V_O (pin 3, see [Details of Interface Pin Functions \(Pg. 12\)](#)). You need to drive V_O to below ground (typically -1v or -2v) until the V_{LCD} is met, making display contrast acceptable.

You can supply the negative voltage by one of the following methods:

1. Use an available source for the negative voltage.

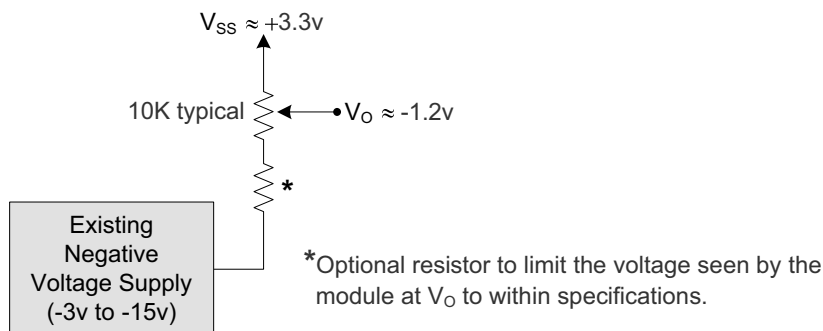


Figure 1. Use Existing Negative Voltage Supply

2. Use a "7660" CMOS switched-capacitor voltage converter or one of the many other available solutions for creating a negative voltage from a positive supply.

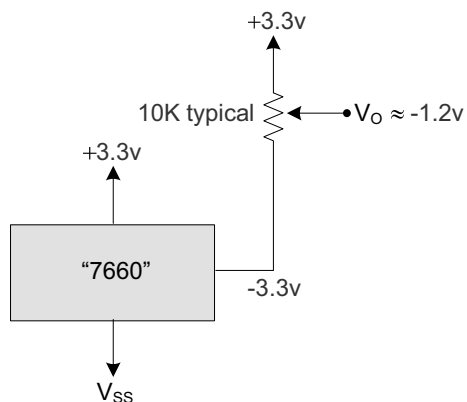


Figure 2. "7660" Switched-Capacitor Voltage Converter



3. Use the circuit in the figure below to create the voltage for V_O by using a PWM (Pulse Width Modulation) output of your microcontroller. This circuit allows the contrast to be adjusted under software control.

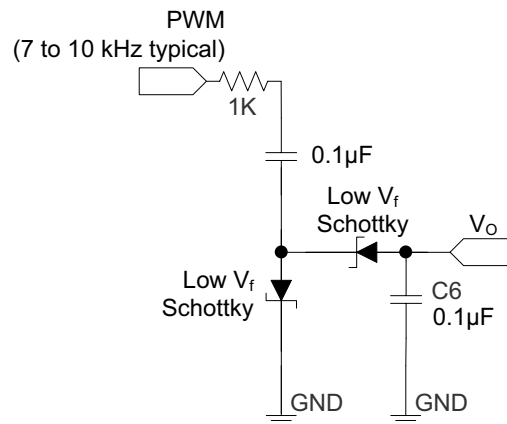


Figure 3. V_O Driving Circuit

Since V_O is pulled up internally by the LCD controller, this circuit will produce positive ($\approx +1\text{v}$) V_{LCD} (V_{LCD} = small, contrast is light) for low ($\approx 10\%$) or high (90%) duty cycles. For duty cycles near 50% , this circuit will produce negative ($\approx -2\text{v}$) levels of V_O (V_{LCD} = big, contrast is dark).

4. Replace this module with the module in this series that has an on-board negative voltage generator. (The part number has a "V" at the end of it.)

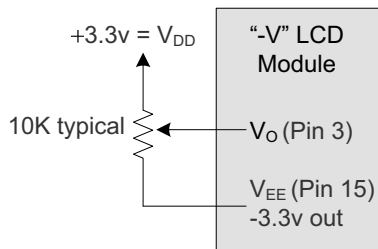


Figure 4. On-Board Negative Voltage Generator



APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET

The complete *Sitronix ST7066U Dot Matrix LCD Controller/Driver* specifications (42 pages) follows.

■ Features

- **5 x 8 and 5 x 11 dot matrix possible**
- **Low power operation support:**
 - 2.7 to 5.5V
- **Wide range of LCD driver power**
 - 3.0 to 10V
- **Correspond to high speed MPU bus interface**
 - 2 MHz (when $V_{cc} = 5V$)
- **4-bit or 8-bit MPU interface enabled**
- **80 x 8-bit display RAM (80 characters max.)**
- **13,200-bit character generator ROM for a total of 240 character fonts(5 x 8 dot or 5 x 11 dot)**
- **64 x 8-bit character generator RAM**
 - 8 character fonts (5 x 8 dot)
 - 4 character fonts (5 x 11 dot)
- **16-common x 40-segment liquid crystal display driver**
- **Programmable duty cycles**
 - 1/8 for one line of 5 x 8 dots with cursor
 - 1/11 for one line of 5 x 11 dots & cursor
 - 1/16 for two lines of 5 x 8 dots & cursor
- **Wide range of instruction functions:**
 - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- **Automatic reset circuit that initializes the controller/driver after power on**
- **Internal oscillator with external resistors**
- **Low power consumption**
- **QFP80 and Bare Chip available**

■ Description

The ST7066U dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

The ST7066U character generator ROM is extended to generate 240 5x8(5x11) dot character fonts for a

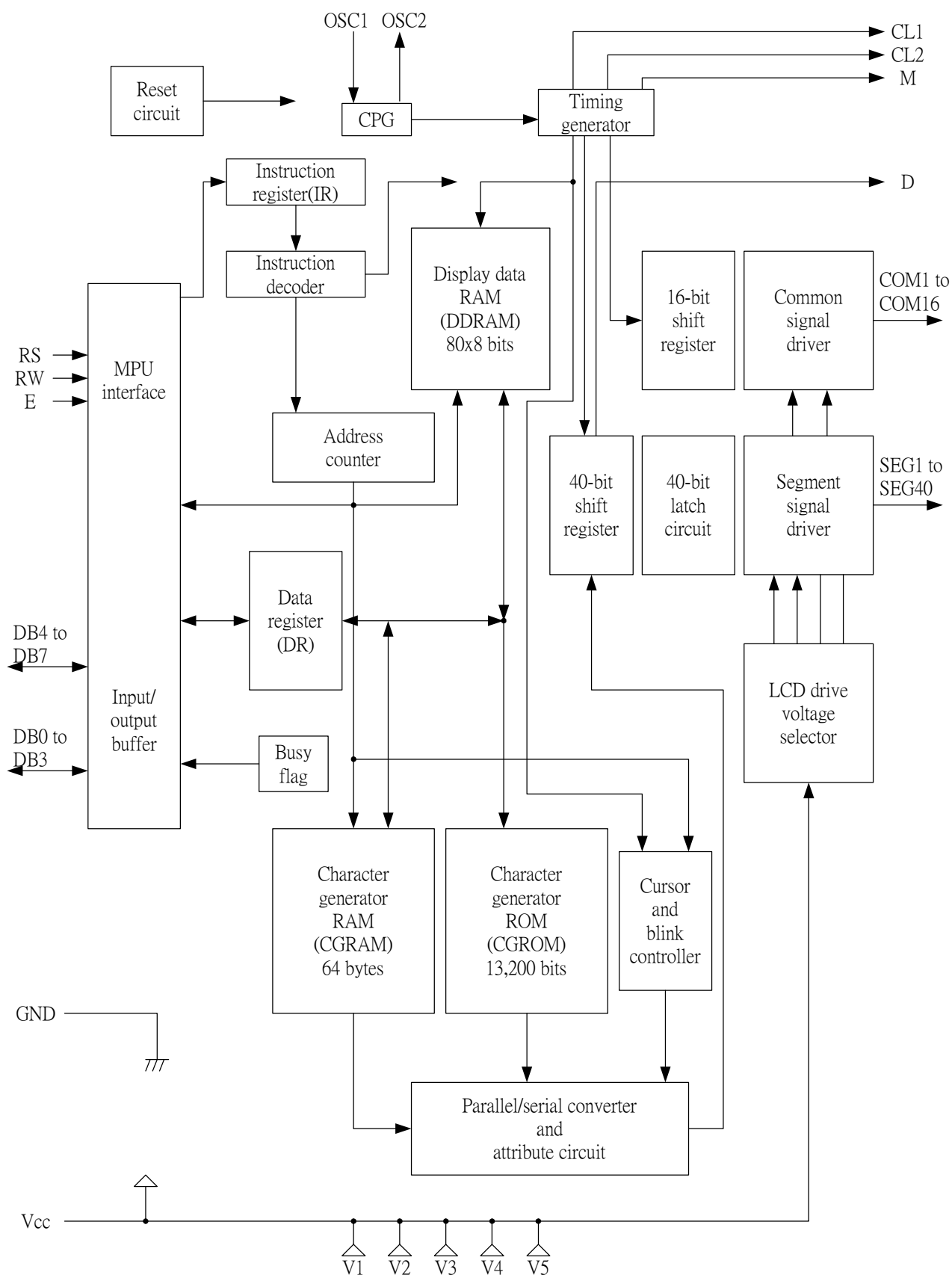
total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the ST7066U is suitable for any portable battery-driven product requiring low power dissipation.

The ST7066U LCD driver consists of 16 common signal drivers and 40 segment signal drivers which can extend display size by cascading segment driver ST7065 or ST7063. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7066U can display up to one 8-character line or two 8-character lines.

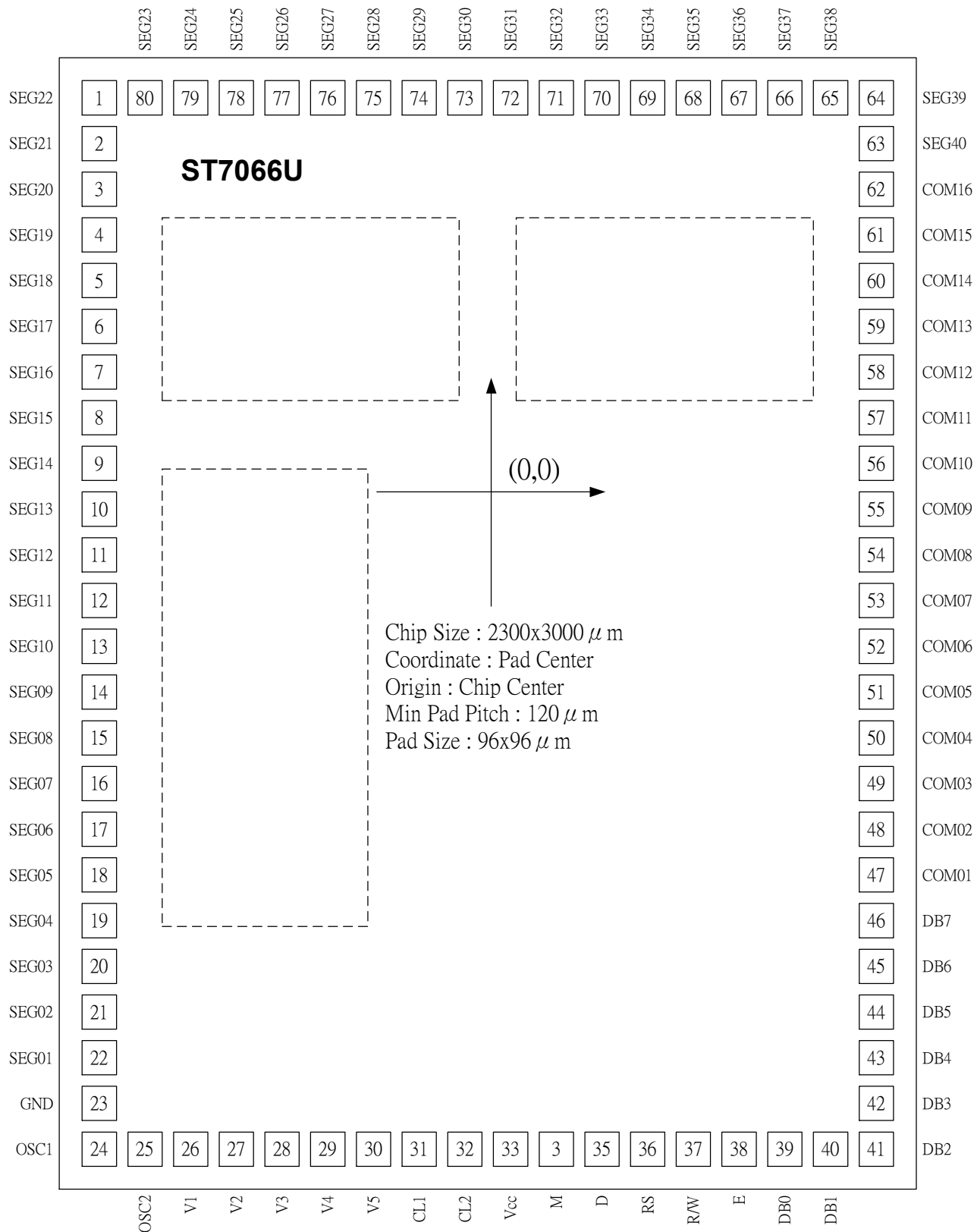
| Product Name | Support Character |
|--------------|--------------------|
| ST7066U-0A | English / Japan |
| ST7066U-0B | English / European |
| ST7066U-0E | English / European |

| ST7066 Serial Specification Revision History | | |
|--|------------|---|
| Version | Date | Description |
| 1.7 | 2000/10/31 | 1. Added 8051 Example Program Code(Page 21,23) 2. Added Annotated Flow Chart : “BF cannot be checked before this instruction” 3. Changed Maximum Ratings Power Supply Voltage:+5.5V →+7.0V(Page 28) |
| 1.8 | 2000/11/14 | Added QFP Pad Configuration(Page 5) |
| 1.8a | 2000/11/30 | 1. Moved QFP Package Dimensions(Page 39) to Page 5 2. Changed DC Characteristics Ratings(Page 32,33) |
| 2.0 | 2001/03/01 | Transition to ST7066U |
| 2.1 | 2006/04/10 | 1. Add Power Supply Conditions (Page 31); 2. Modify reset description on Page 22. |
| 2.2 | 2006/05/11 | Emphasis checking BF procedure (Page 9, 27, 28). |
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■ Block Diagram



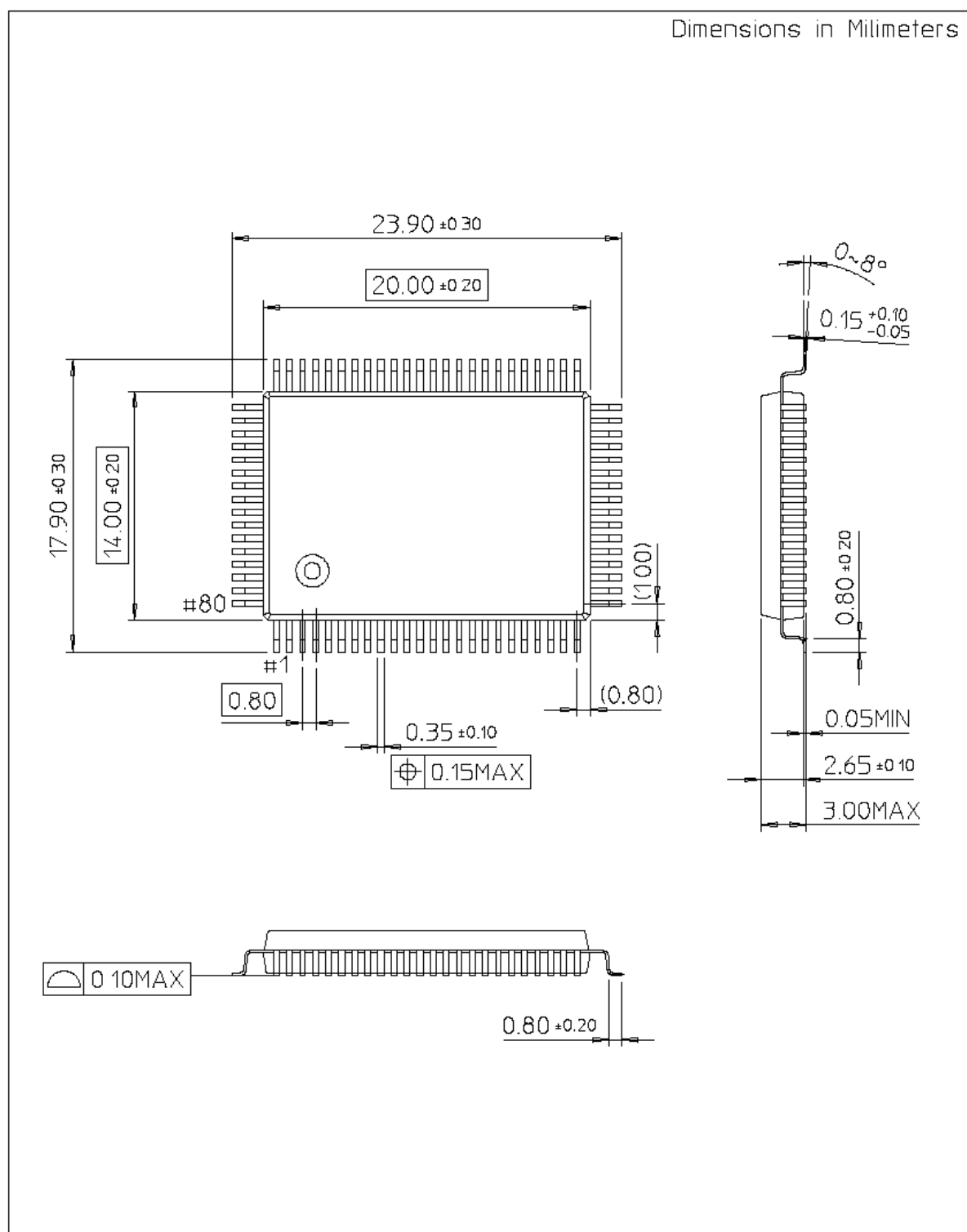
■ Pad Arrangement



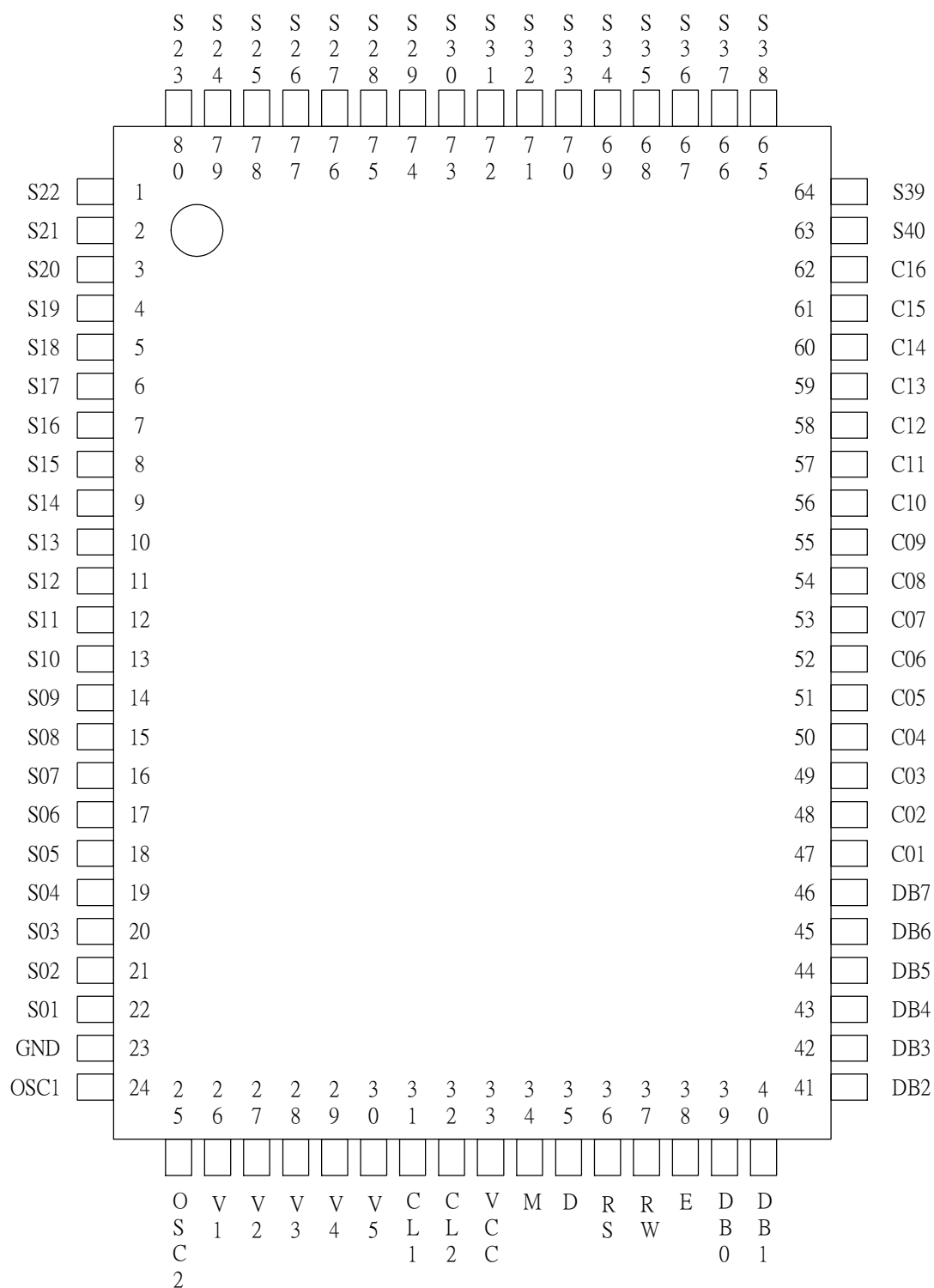
Substrate Connect to VDD.

■ Package Dimensions

80-QFP-1420C



■ Pad Configuration(80 QFP)



■ Pad Location Coordinates

| Pad No. | Function | X | Y |
|---------|----------|-------|-------|
| 1 | SEG22 | -1040 | 1400 |
| 2 | SEG21 | -1040 | 1270 |
| 3 | SEG20 | -1040 | 1140 |
| 4 | SEG19 | -1040 | 1020 |
| 5 | SEG18 | -1040 | 900 |
| 6 | SEG17 | -1040 | 780 |
| 7 | SEG16 | -1040 | 660 |
| 8 | SEG15 | -1040 | 540 |
| 9 | SEG14 | -1040 | 420 |
| 10 | SEG13 | -1040 | 300 |
| 11 | SEG12 | -1040 | 180 |
| 12 | SEG11 | -1040 | 60 |
| 13 | SEG10 | -1040 | -60 |
| 14 | SEG9 | -1040 | -180 |
| 15 | SEG8 | -1040 | -300 |
| 16 | SEG7 | -1040 | -420 |
| 17 | SEG6 | -1040 | -540 |
| 18 | SEG5 | -1040 | -660 |
| 19 | SEG4 | -1040 | -780 |
| 20 | SEG3 | -1040 | -900 |
| 21 | SEG2 | -1040 | -1020 |
| 22 | SEG1 | -1040 | -1140 |
| 23 | GND | -1040 | -1270 |
| 24 | OSC1 | -1040 | -1400 |
| 25 | OSC2 | -910 | -1400 |
| 26 | V1 | -780 | -1400 |
| 27 | V2 | -660 | -1400 |
| 28 | V3 | -540 | -1400 |
| 29 | V4 | -420 | -1400 |
| 30 | V5 | -300 | -1400 |
| 31 | CL1 | -180 | -1400 |
| 32 | CL2 | -60 | -1400 |
| 33 | Vcc | 60 | -1400 |
| 34 | M | 180 | -1400 |
| 35 | D | 300 | -1400 |
| 36 | RS | 420 | -1400 |
| 37 | RW | 540 | -1400 |
| 38 | E | 660 | -1400 |
| 39 | DB0 | 780 | -1400 |
| 40 | DB1 | 910 | -1400 |

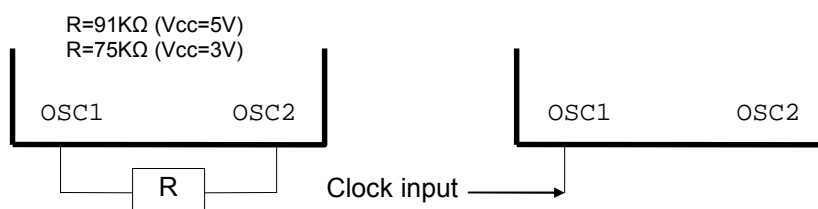
| Pad No. | Function | X | Y |
|---------|----------|------|-------|
| 41 | DB2 | 1040 | -1400 |
| 42 | DB3 | 1040 | -1270 |
| 43 | DB4 | 1040 | -1140 |
| 44 | DB5 | 1040 | -1020 |
| 45 | DB6 | 1040 | -900 |
| 46 | DB7 | 1040 | -780 |
| 47 | COM1 | 1040 | -660 |
| 48 | COM2 | 1040 | -540 |
| 49 | COM3 | 1040 | -420 |
| 50 | COM4 | 1040 | -300 |
| 51 | COM5 | 1040 | -180 |
| 52 | COM6 | 1040 | -60 |
| 53 | COM7 | 1040 | 60 |
| 54 | COM8 | 1040 | 180 |
| 55 | COM9 | 1040 | 300 |
| 56 | COM10 | 1040 | 420 |
| 57 | COM11 | 1040 | 540 |
| 58 | COM12 | 1040 | 660 |
| 59 | COM13 | 1040 | 780 |
| 60 | COM14 | 1040 | 900 |
| 61 | COM15 | 1040 | 1020 |
| 62 | COM16 | 1040 | 1140 |
| 63 | SEG40 | 1040 | 1270 |
| 64 | SEG39 | 1040 | 1400 |
| 65 | SEG38 | 910 | 1400 |
| 66 | SEG37 | 780 | 1400 |
| 67 | SEG36 | 660 | 1400 |
| 68 | SEG35 | 540 | 1400 |
| 69 | SEG34 | 420 | 1400 |
| 70 | SEG33 | 300 | 1400 |
| 71 | SEG32 | 180 | 1400 |
| 72 | SEG31 | 60 | 1400 |
| 73 | SEG30 | -60 | 1400 |
| 74 | SEG29 | -180 | 1400 |
| 75 | SEG28 | -300 | 1400 |
| 76 | SEG27 | -420 | 1400 |
| 77 | SEG26 | -540 | 1400 |
| 78 | SEG25 | -660 | 1400 |
| 79 | SEG24 | -780 | 1400 |
| 80 | SEG23 | -910 | 1400 |

■ Pin Function

| Name | Number | I/O | Interfaced with | Function |
|----------------|--------|-----|----------------------------|--|
| RS | 1 | I | MPU | Select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read) |
| R/W | 1 | I | MPU | Select read or write. 0: Write 1: Read |
| E | 1 | I | MPU | Starts data read/write. |
| DB4 to DB7 | 4 | I/O | MPU | Four high order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. DB7 can be used as a busy flag. |
| DB0 to DB3 | 4 | I/O | MPU | Four low order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. These pins are not used during 4-bit operation. |
| CL1 | 1 | O | Extension driver | Clock to latch serial data D sent to the extension driver |
| CL2 | 1 | O | Extension driver | Clock to shift serial data D |
| M | 1 | O | Extension driver | Switch signal for converting the liquid crystal drive waveform to AC |
| D | 1 | O | Extension driver | Character pattern data corresponding to each segment signal |
| COM1 to COM16 | 16 | O | LCD | Common signals that are not used are changed to non-selection waveform. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor. |
| SEG1 to SEG40 | 40 | O | LCD | Segment signals |
| V1 to V5 | 5 | - | Power supply | Power supply for LCD drive $V_{CC} - V5 = 10\text{ V (Max)}$ |
| V_{CC} , GND | 2 | - | Power supply | V_{CC} : 2.7V to 5.5V, GND: 0V |
| OSC1, OSC2 | 2 | | Oscillation resistor clock | When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1. |

Note:

1. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained
2. Two clock options:



■ Function Description

● System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

| RS | R/W | Operation |
|----|-----|---|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| L | H | Read Busy Flag(DB7) and address counter (DB0 ~ DB6) |
| H | L | Data Write operation (MPU writes data into DR) |
| H | H | Data Read operation (MPU reads data from DR) |

Table 1. Various kinds of operations according to RS and R/W bits.

● Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High. **Before checking BF, be sure to wait at least 80us. Please refer to Page 27 for the example. Do NOT keep "E" always "High" for checking BF.**

● Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

● Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

➤ 1-line display ($N = 0$) (Figure 2)

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the ST7066U, 8 characters are displayed. See Figure 3.

When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

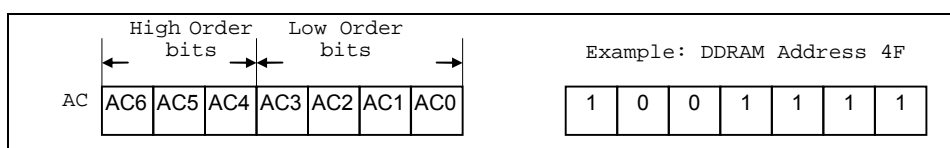


Figure 1 DDRAM Address

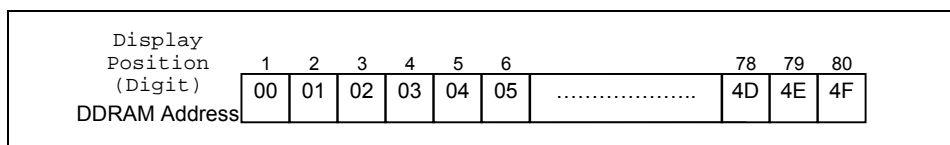


Figure 2 1-Line Display

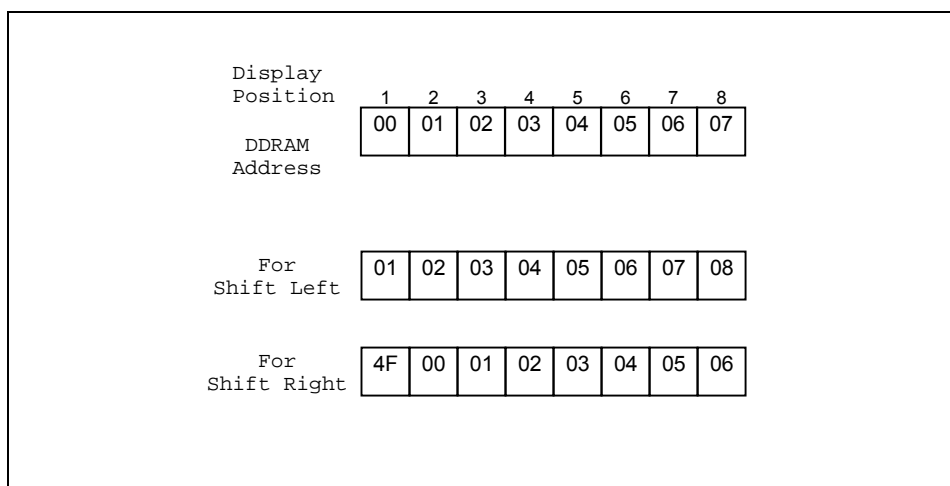


Figure 3 1-Line by 8-Character Display Example

➤ 2-line display ($N = 1$) (Figure 4)

Case 1: When the number of display characters is less than 40×2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the ST7066U is used, 8 characters \times 2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

| | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|-------|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | | 38 | 39 | 40 |
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | | 25 | 26 | 27 |
| | 40 | 41 | 42 | 43 | 44 | 45 | | 65 | 66 | 67 |

Figure 4 2-Line Display

| | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 |

Figure 5 2-Line by 8-Character Display Example

Case 2: For a 16-character × 2-line display, the ST7066U can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

| | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E |

Figure 6 2-Line by 16-Character Display Example

- **Character Generator ROM (CGROM)**

The character generator ROM generates 5 x 8 dot or 5 x 11 dot character patterns from 8-bit character codes. It can generate 240 5 x 8 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

- **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 11 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

- **Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

- **LCD Driver Circuit**

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch. In case of 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have 1/11 duty, and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

- **Cursor/Blink Control Circuit**

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: 0A)

NO.7066-0A

| b7-b4 b3-b0 | | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM (1) | | | 0 | 8 | P | ˆ | P | | | | — | 9 | 3 | 8 | P | |
| 0001 | (2) | | ! | 1 | A | 0 | a | 9 | | | 6 | 7 | * | 4 | 8 | 9 | |
| 0010 | (3) | | " | 2 | B | R | b | r | | | 7 | 4 | 9 | × | p | 8 | |
| 0011 | (4) | | # | 3 | C | S | c | s | | | 8 | 5 | T | E | 8 | × | |
| 0100 | (5) | | \$ | 4 | D | T | d | t | | | 9 | I | t | † | μ | 8 | |
| 0101 | (6) | | % | 5 | E | U | e | u | | | * | † | † | 1 | 8 | 0 | |
| 0110 | (7) | | & | 6 | F | V | f | v | | | 9 | † | 2 | 3 | p | Σ | |
| 0111 | (8) | | ' | 7 | G | W | g | w | | | † | * | 3 | 9 | g | π | |
| 1000 | (1) | | < | 8 | H | X | h | x | | | 4 | 5 | * | 9 | † | Σ | |
| 1001 | (2) | | > | 9 | I | Y | i | y | | | 5 | † | 9 | μ | † | 9 | |
| 1010 | (3) | | * | : | J | Z | j | z | | | 6 | † | † | † | † | * | |
| 1011 | (4) | | + | ; | K | [| k | [| | | † | † | † | † | * | † | |
| 1100 | (5) | | , | < | L | * | l | l | | | † | † | † | † | † | † | |
| 1101 | (6) | | — | = | N |] | n | > | | | † | † | † | † | † | † | |
| 1110 | (7) | | . | > | N | ^ | n | ~ | | | † | † | † | † | † | † | |
| 1111 | (8) | | / | ? | 0 | _ | o | ~ | | | † | † | † | † | † | † | |

Table 4(Cont.) (ROM Code: 0B)

NO.7066-0B

| b7-b4 b3-b0 | | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM (1) | ± | | 0 | 0 | P | ° | P | 9 | é | à | | í | À | ß | ç | |
| 0001 | (2) | ≡ | ! | 1 | A | 0 | a | 9 | 0 | * | í | | ¡ | † | ý | ú | |
| 0010 | (3) | 7 | " | 2 | B | R | b | r | é | É | ó | | ° | ó | è | è | ¿ |
| 0011 | (4) | ¿ | # | 3 | C | 8 | c | é | à | ó | ú | | ¿ | ¶ | ¶ | é | ¶ |
| 0100 | (5) | ¡ | \$ | 4 | D | T | d | t | à | ó | ¢ | | ¡ | ¶ | ¿ | ¿ | ó |
| 0101 | (6) | ¡ | % | 5 | E | U | e | u | à | ó | E | | ¡ | † | ¿ | ¶ | ¶ |
| 0110 | (7) | ¡ | & | 6 | F | V | f | v | à | ó | ¥ | | ¡ | ↓ | 0 | 0 | ¶ |
| 0111 | (8) | ¡ | ' | 7 | G | W | g | w | ó | ó | ¥ | | ¡ | × | × | À | ¶ |
| 1000 | (1) | ¡ | (| 8 | H | X | h | x | é | 9 | ¢ | | ¡ | ÷ | ÷ | E | K |
| 1001 | (2) | ¡ |) | 9 | I | Y | i | y | é | 0 | ¡ | | ¡ | ∏ | ∏ | À | ¶ |
| 1010 | (3) | × | * | : | J | Z | j | z | é | 0 | à | | ¡ | ∏ | ∏ | μ | ¶ |
| 1011 | (4) | ¡ | + | ; | K | L | k | l | í | À | à | | ¡ | ∏ | ∏ | ú | ¶ |
| 1100 | (5) | = | , | < | L | \ | l | l | í | À | 8 | | ¡ | ∏ | ∏ | ¿ | 0 |
| 1101 | (6) | ó | - | = | M | J | m | j | í | à | 8 | | ¡ | * | * | ¶ | ¶ |
| 1110 | (7) | ¶ | . | > | N | ^ | n | ~ | À | 9 | 8 | | ¡ | 0 | 0 | p | ¶ |
| 1111 | (8) | ¶ | / | ? | O | _ | o | à | À | ¿ | 8 | | ¡ | 0 | 0 | 0 | ¶ |

Table 4(Cont.) (ROM Code: 0E)

NO.7066-0E

| b7-b4 b3-b0 | | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM (1) | | | | 0 | a | P | > | P | 0 | e | a | s | s | | a | p |
| 0001 | (2) | | | ! | 1 | A | Q | a | 9 | 0 | e | 1 | ± | L | | 3 | 9 |
| 0010 | (3) | | | " | 2 | B | R | b | r | 0 | e | 1 | 0 | B | | 2 | e |
| 0011 | (4) | | | # | 3 | C | S | c | s | 0 | e | 1 | ↑ | B | | 4 | * |
| 0100 | (5) | | | \$ | 4 | D | T | d | t | 0 | e | 1 | ↓ | G | | 5 | a |
| 0101 | (6) | | | % | 5 | E | U | e | u | 0 | e | 1 | ← | B | | 6 | P |
| 0110 | (7) | | | & | 6 | F | V | f | v | 0 | e | 1 | → | B | | 7 | Σ |
| 0111 | (8) | | | ' | 7 | G | W | g | w | 0 | e | 1 | ↖ | C | | 8 | γ |
| 1000 | (1) | | | (| 8 | H | X | h | x | 0 | a | 1 | * | P | | 9 | 0 |
| 1001 | (2) | | |) | 9 | I | Y | i | y | 0 | a | 2 | + | B | | 1 | 9 |
| 1010 | (3) | | | * | : | J | Z | j | z | 0 | a | 3 | + | G | | 2 | B |
| 1011 | (4) | | | + | ; | K | L | k | l | 0 | a | 4 | ± | A | | 3 | 1 |
| 1100 | (5) | | | , | < | L | * | l | l | 0 | a | 5 | ¶ | C | | 4 | A |
| 1101 | (6) | | | - | = | M | I | m | i | 0 | a | 6 | 4 | B | | 5 | U |
| 1110 | (7) | | | . | > | N | ^ | n | ~ | 0 | a | 7 | 5 | B | | 6 | 1 |
| 1111 | (8) | | | / | ? | O | _ | o | * | 0 | a | 8 | 4 | B | | 7 | ■ |

| Character Code (DDRAM Data) | | | | | | | | CGRAM Address | | | | | | Character Patterns (CGRAM Data) | | | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|------------------------------------|----|----|----|----|----|----|----|--|--|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | b5 | b4 | b3 | b2 | b1 | b0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | | |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 1 | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 1 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 1 | 0 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 1 | 1 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 0 | | | | 1 | 0 | 0 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 0 | | | | 1 | 0 | 1 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 0 | | | | 1 | 1 | 0 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 0 | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | | | | |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 0 | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 1 | | | | 0 | 1 | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 1 | 0 | | | | 0 | 1 | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 1 | 1 | | | | 1 | 0 | | | | | |
| | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 1 | | | | 1 | 0 | 1 | | | | 0 | 0 | | | | | |
| | | | | | 0 | 0 | 1 | | | | 1 | 1 | 0 | | | | 0 | 1 | | | | | |
| | | | | | 0 | 0 | 1 | | | | 1 | 1 | 1 | | | | 0 | 0 | | | | | |

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.

“-”: Indicates no effect.

■ Instructions

There are four categories of instructions that:

- Designate ST7066U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Others

Instruction Table:

| Instruction | Instruction Code | | | | | | | | | | Description | Description Time (270KHz) |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|------------------------------|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC | 1.52 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.52 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 37 us |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:entire display on C=1:cursor on B=1:cursor position on | 37 us |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x | Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 37 us |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x | DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8 | 37 us |
| Set CGRAM address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter | 37 us |
| Set DDRAM address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter | 37 us |
| Read Busy flag and address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 us |
| Write data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM) | 37 us |
| Read data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM) | 37 us |

Note:

Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

■ Instruction Description

● Clear Display

| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

● Return Home

| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

● Entry Mode Set

| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

- **I/D : Increment / decrement of DDRAM address (cursor or blink)**
 When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
 When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
 * CGRAM operates the same as DDRAM, when read from or write to CGRAM.
- **S: Shift of entire display**
 When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

| S | I/D | Description |
|---|-----|--------------------------------|
| H | H | Shift the display to the left |
| H | L | Shift the display to the right |

● Display ON/OFF

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

● Cursor or Display Shift

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x |

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

| S/C | R/L | Description | AC Value |
|-----|-----|--|----------|
| L | L | Shift cursor to the left | AC=AC-1 |
| L | H | Shift cursor to the right | AC=AC+1 |
| H | L | Shift display to the left. Cursor follows the display shift | AC=AC |
| H | H | Shift display to the right. Cursor follows the display shift | AC=AC |

● Function Set

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x |

- **DL : Interface data length control bit**
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.
- **N : Display line number control bit**
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
- **F : Display font type control bit**
When F = "Low", it means 5 x 8 dots format display mode
When F = "High", 5 x 11 dots format display mode.

| N | F | No. of Display Lines | Character Font | Duty Factor |
|---|---|----------------------|----------------|-------------|
| L | L | 1 | 5x8 | 1/8 |
| L | H | 1 | 5x11 | 1/11 |
| H | x | 2 | 5x8 | 1/16 |

● Set CGRAM Address

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

● Set DDRAM Address

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

● Read Busy Flag and Address

| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

When BF = "High", indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

● Write Data to CGRAM or DDRAM

| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

● Read Data from CGRAM or DDRAM

| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

■ Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the ST7066U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

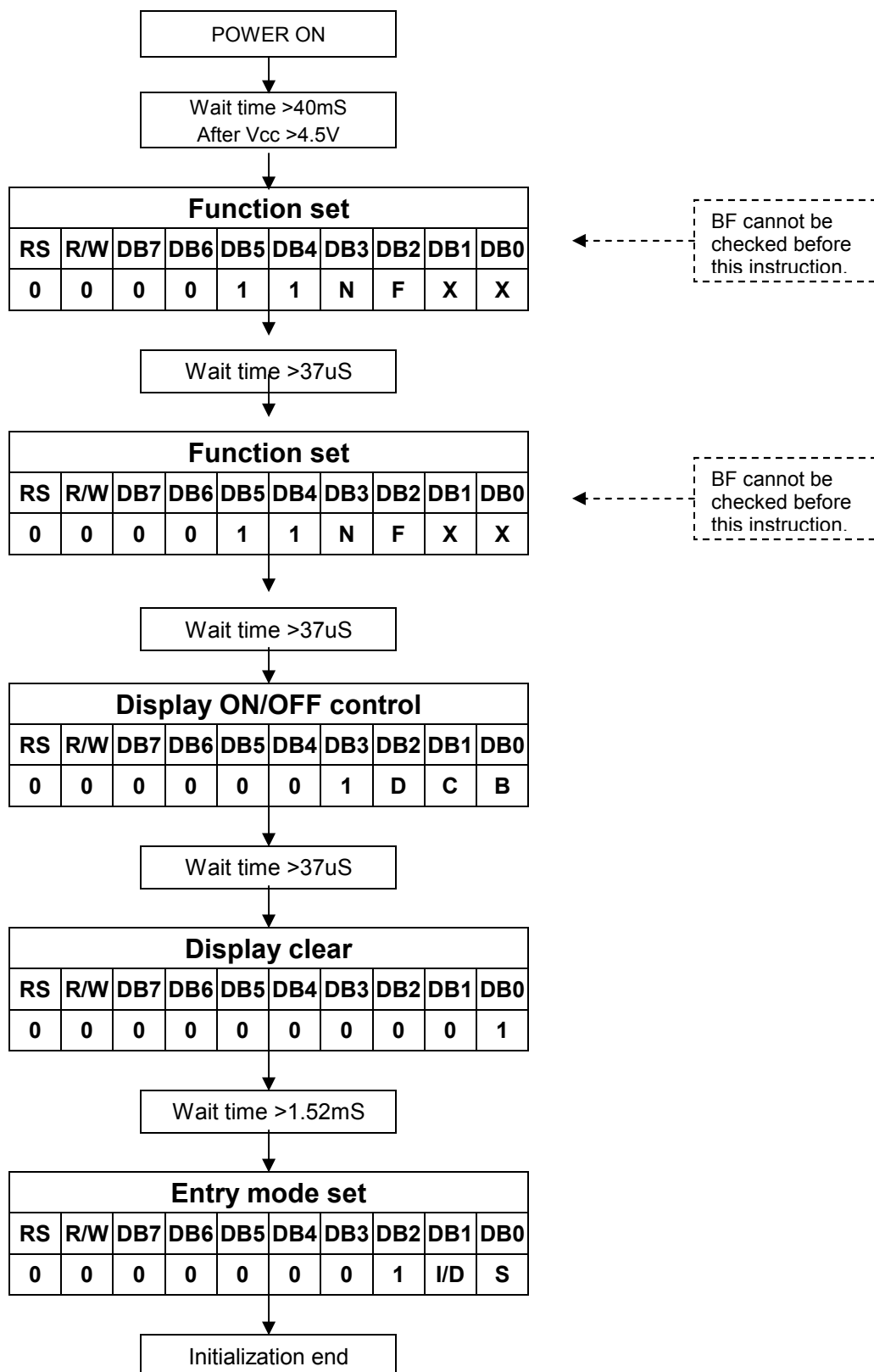
1. Display clear
2. Function set:
 - DL = 1; 8-bit interface data
 - N = 0; 1-line display
 - F = 0; 5x8 dot character font
3. Display on/off control:
 - D = 0; Display off
 - C = 0; Cursor off
 - B = 0; Blinking off
4. Entry mode set:
 - I/D = 1; Increment by 1
 - S = 0; No shift

Note:

If the electrical characteristics conditions listed in the table Power Supply Conditions (Page 31) are not met, the internal reset circuit will not operate normally and will fail to initialize the ST7066U. For such a case, initialization must be performed by the MPU as explain by the following figures.

■ Initializing by Instruction

- 8-bit Interface (fosc=270KHz)



➤ Initial Program Code Example For 8051 MPU(8 Bit Interface):

INITIAL_START:

```
CALL    DELAY40mS

MOV     A,#38H           ;FUNCTION SET
CALL    WRINS_NOCHK      ;8 bit,N=1,5*7dot
CALL    DELAY37uS

MOV     A,#38H           ;FUNCTION SET
CALL    WRINS_NOCHK      ;8 bit,N=1,5*7dot
CALL    DELAY37uS

MOV     A,#0FH           ;DISPLAY ON
CALL    WRINS_CHK
CALL    DELAY37uS

MOV     A,#01H           ;CLEAR DISPLAY
CALL    WRINS_CHK
CALL    DELAY1.52mS

MOV     A,#06H           ;ENTRY MODE SET
CALL    WRINS_CHK        ;CURSOR MOVES TO RIGHT
CALL    DELAY37uS
```

MAIN_START:

```
XXXX
XXXX
XXXX
XXXX
.
.
.
.
```

WRINS_CHK:

```
CALL    CHK_BUSY
```

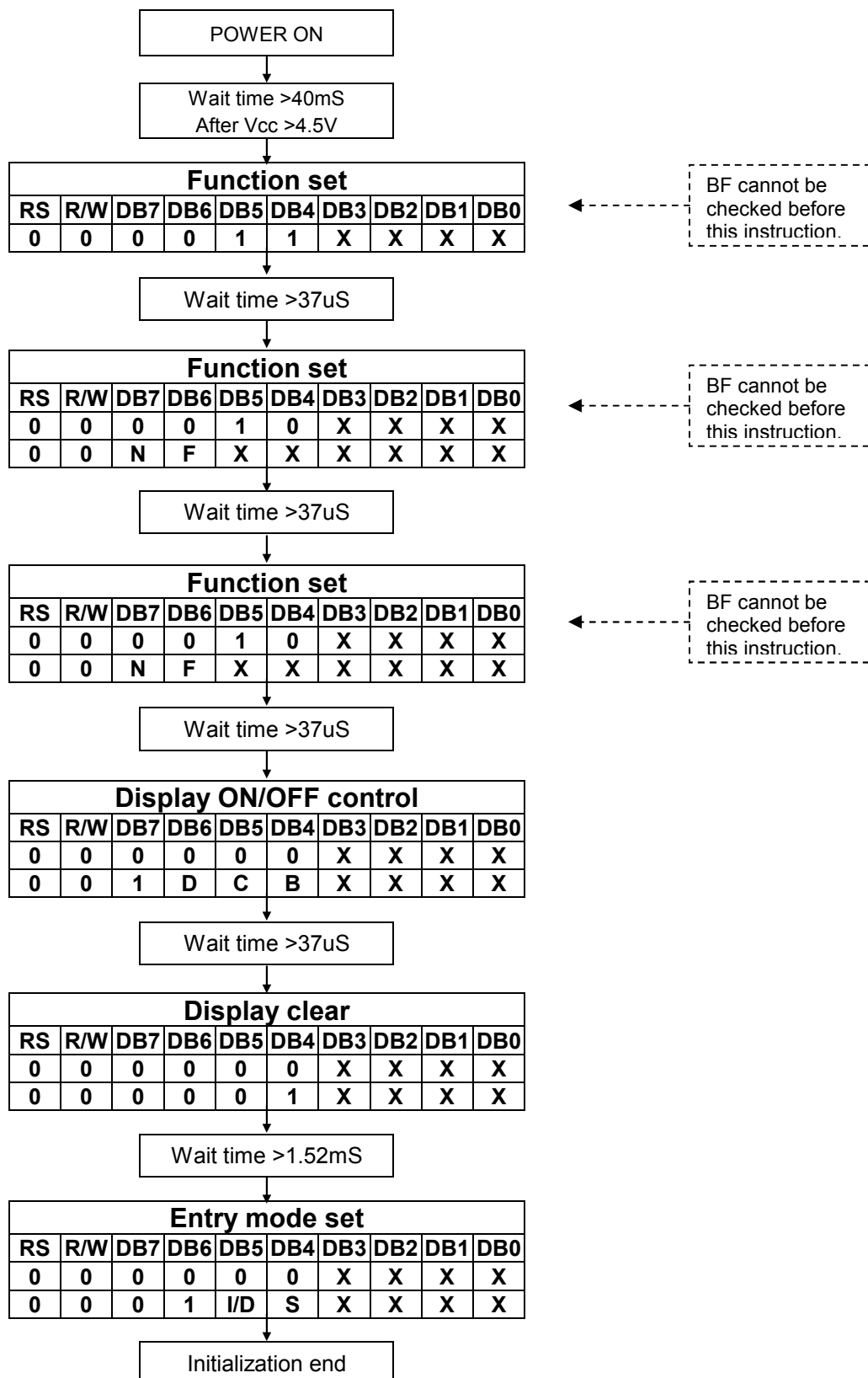
WRINS_NOCHK:

```
CLR     RS               ;EX:Port 3.0
CLR     RW               ;EX:Port 3.1
SETB    E                ;EX:Port 3.2
MOV     P1,A             ;EX:Port 1=Data Bus
CLR     E
MOV     P1,#FFH          ;For Check Busy Flag
RET
```

CHK_BUSY: ;Check Busy Flag

```
CLR     RS
SETB    RW
SETB    E
JB      P1.7,$
CLR     E
RET
```

● 4-bit Interface (fosc=270KHz)



➤ **Initial Program Code Example For 8051 MPU(4 Bit Interface):**

```

;-----
INITIAL_START:
    CALL    DELAY40mS

    MOV     A,#38H          ;FUNCTION SET
    CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
    CALL    DELAY37uS

    MOV     A,#28H          ;FUNCTION SET
    CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
    CALL    DELAY37uS

    MOV     A,#28H          ;FUNCTION SET
    CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
    CALL    DELAY37uS

    MOV     A,#0FH          ;DISPLAY ON
    CALL    WRINS_CHK
    CALL    DELAY37uS

    MOV     A,#01H          ;CLEAR DISPLAY
    CALL    WRINS_CHK
    CALL    DELAY1.52mS

    MOV     A,#06H          ;ENTRY MODE SET
    CALL    WRINS_CHK
    CALL    DELAY37uS

;-----
MAIN_START:
    XXXX
    XXXX
    XXXX
    XXXX
    .
    .
    .
    .
    .
    .
    .
    .
    .
    .

;-----
WRINS_CHK:
    CALL    CHK_BUSY

WRINS_NOCHK:
    PUSH    A
    ANL     A,#F0H
    CLR     RS              ;EX:Port 3.0
    CLR     RW              ;EX:Port 3.1
    SETB    E               ;EX:Port 3.2
    MOV     P1,A            ;EX:Port1=Data Bus
    CLR     E
    POP     A
    SWAP    A

WRINS_ONCE:
    ANL     A,#F0H
    CLR     RS
    CLR     RW
    SETB    E
    MOV     P1,A
    CLR     E
    MOV     P1,#FFH        ;For Check Bus Flag
    RET

;-----
CHK_BUSY:                                ;Check Busy Flag
    PUSH    A
    MOV     P1,#FFH

$1
    CLR     RS
    SETB    RW
    SETB    E
    MOV     A,P1
    CLR     E
    MOV     P1,#FFH
    CLR     RS
    SETB    RW
    SETB    E
    NOP
    CLR     E
    JB      A.7,$1
    POP     A
    RET

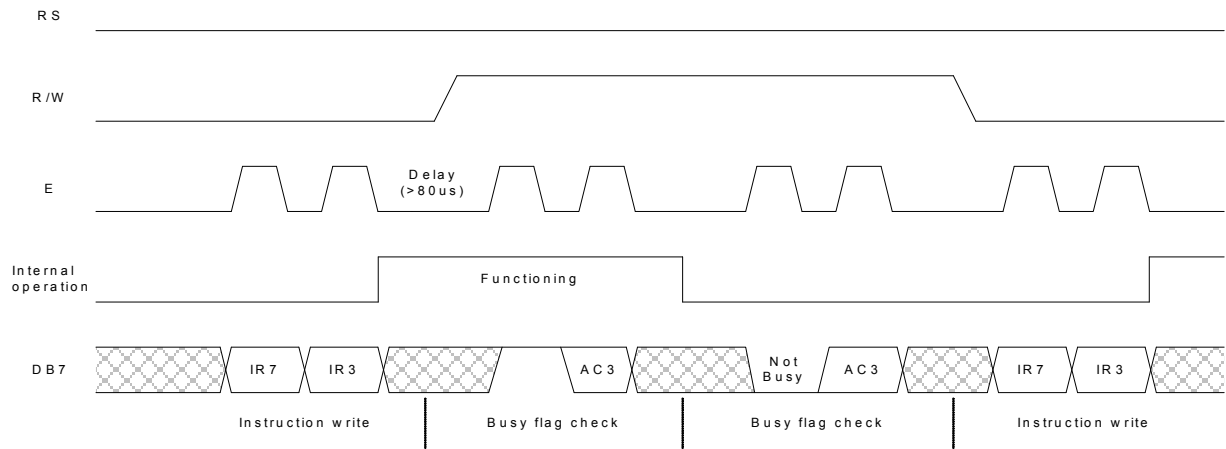
```


■ Interfacing to the MPU

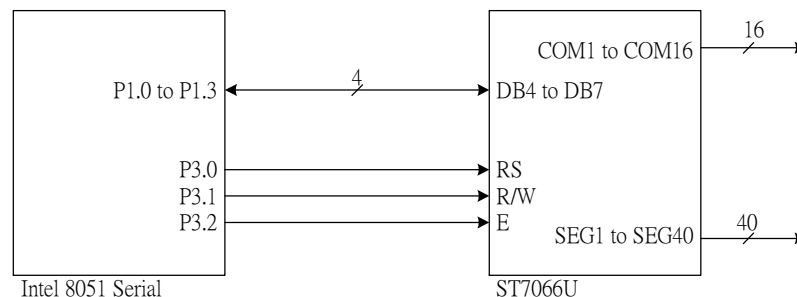
The ST7066U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPU.

- **For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.** Bus lines DB0 to DB3 are disabled. The data transfer between the ST7066U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

➤ Example of busy flag check timing sequence

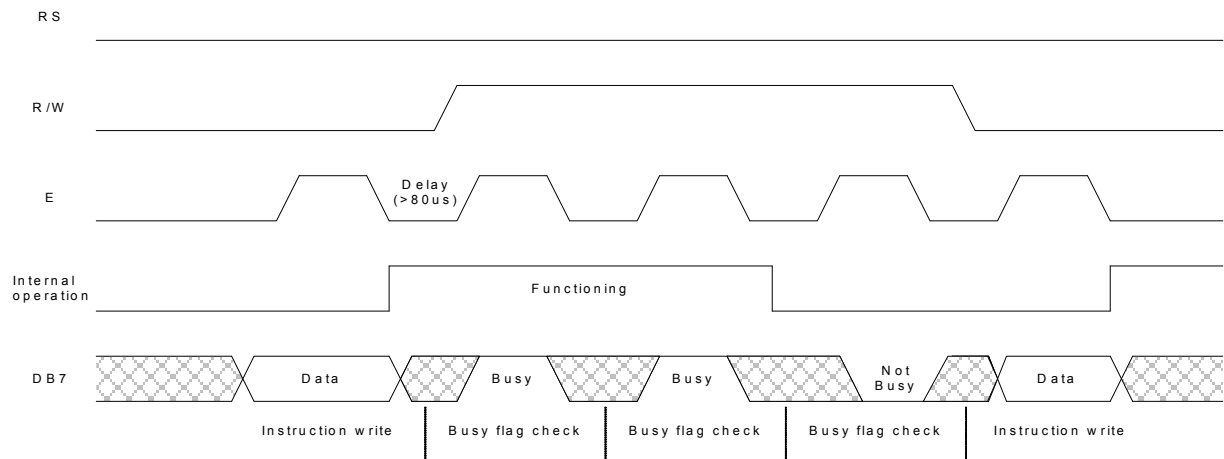


➤ Intel 8051 interface

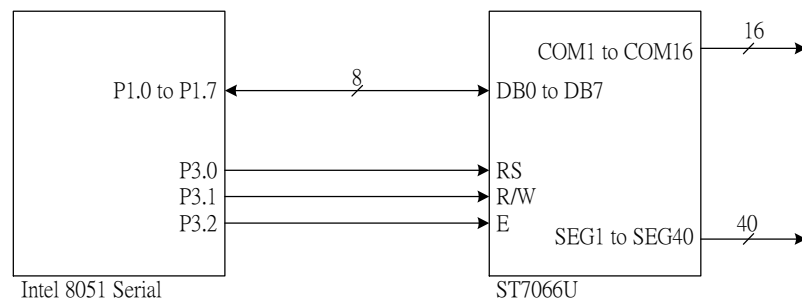


- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

➤ Example of busy flag check timing sequence



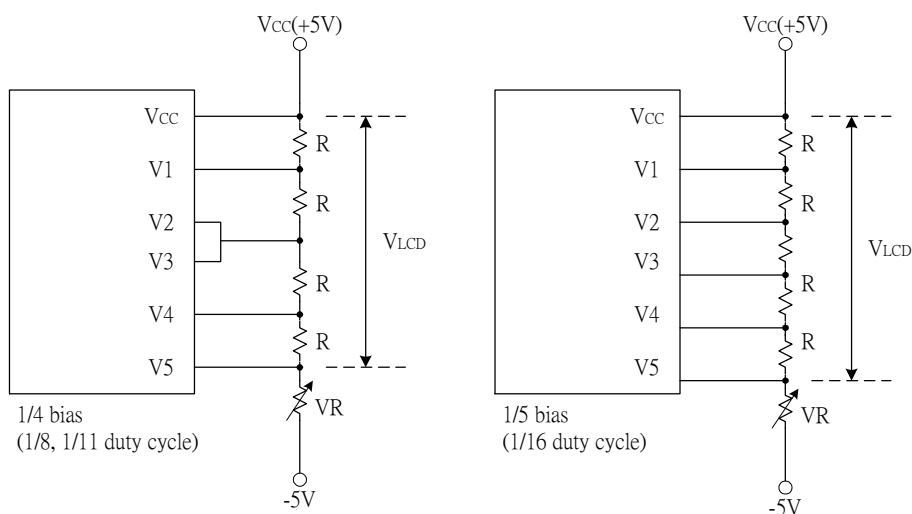
➤ Intel 8051 interface



■ Supply Voltage for LCD Drive

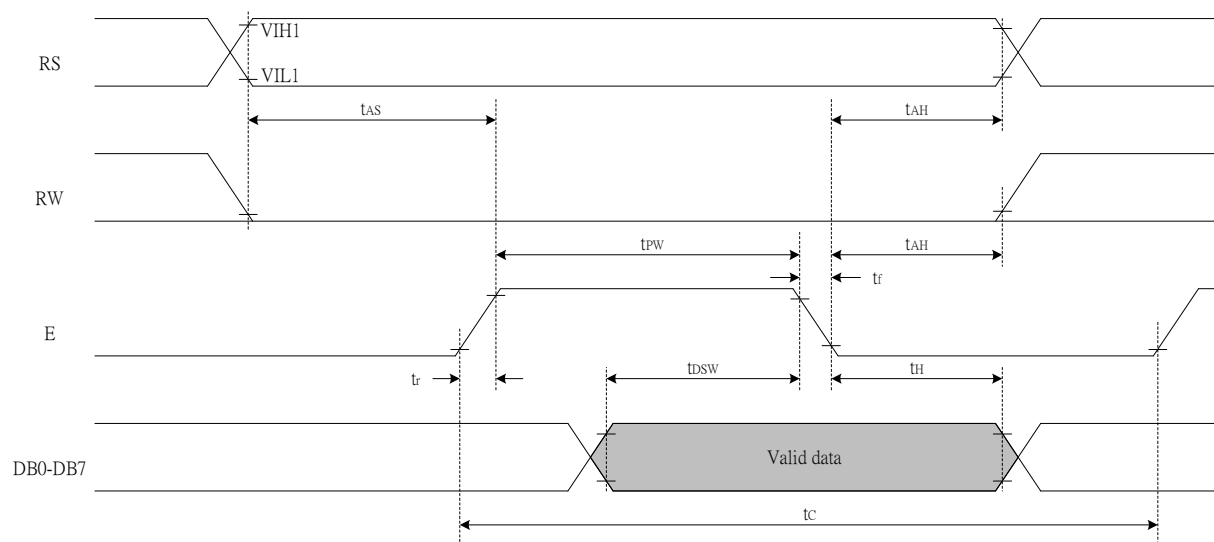
There are different voltages that supply to ST7066U's pin (V1 - V5) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

| | Duty Factor | |
|----------------|-----------------------|-----------------------|
| | 1/8, 1/11 | 1/16 |
| | Bias | |
| Supply Voltage | 1/4 | 1/5 |
| V1 | $V_{CC} - 1/4V_{LCD}$ | $V_{CC} - 1/5V_{LCD}$ |
| V2 | $V_{CC} - 1/2V_{LCD}$ | $V_{CC} - 2/5V_{LCD}$ |
| V3 | $V_{CC} - 1/2V_{LCD}$ | $V_{CC} - 3/5V_{LCD}$ |
| V4 | $V_{CC} - 3/4V_{LCD}$ | $V_{CC} - 4/5V_{LCD}$ |
| V5 | $V_{CC} - V_{LCD}$ | $V_{CC} - V_{LCD}$ |

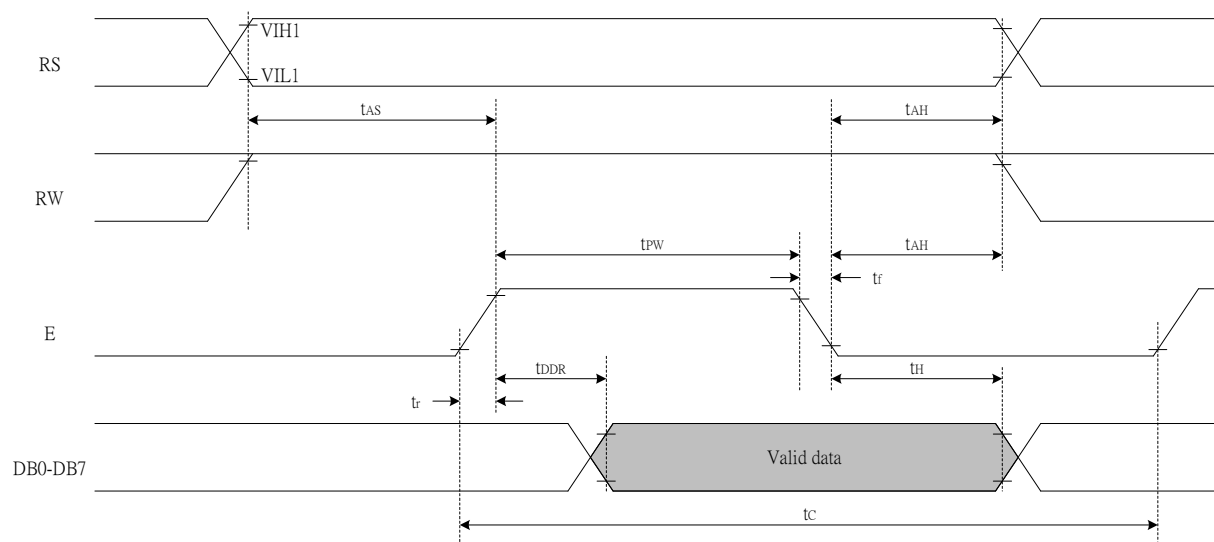


■ Timing Characteristics

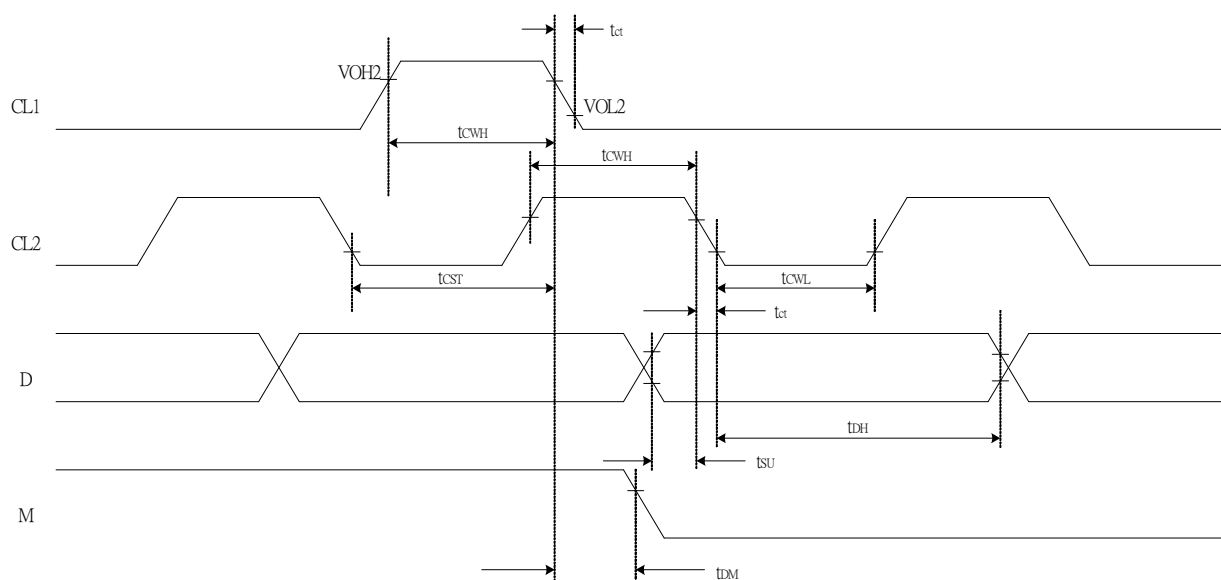
● Writing data from MPU to ST7066U



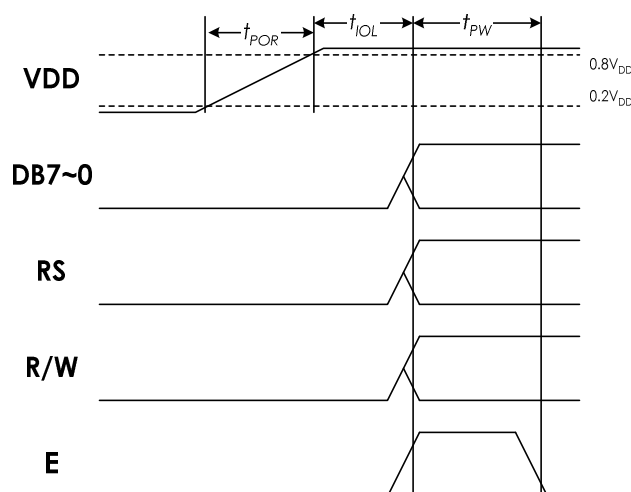
● Reading data from ST7066U to MPU



● Interface Timing with External Driver



■ Power Supply Conditions



| Symbol | Characteristics | Description | Min. | Typ. | Max. | Unit |
|-----------|--------------------|---|------|------|------|------|
| t_{POR} | Power rise time | Power rise time that will trigger internal power on reset circuit | 0.1 | | 100 | ms |
| t_{IOL} | I/O Low time | The period that I/O is kept low. | 40 | | | ms |
| t_{PW} | Enable pulse width | Please refer to the following tables. | | | | |

1. During t_{POR} , V_{DD} noise should be reduced (especially close to 2.0V). Otherwise the Power-ON-Reset function might be triggered several times and maybe cause unexpected result.
2. During t_{IOL} , the I/O ports of the interface (control and data signals) should be kept at "Low".

■ AC Characteristics

(TA = 25°C, VCC = 2.7V)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|--|-----------------------|-----------------|------|------|------|------|
| <i>Internal Clock Operation</i> | | | | | | |
| f _{OSC} | OSC Frequency | R = 75KΩ | 190 | 270 | 350 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f _{EX} | External Frequency | - | 125 | 270 | 410 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T _R , T _F | Rise/Fall Time | - | - | - | 0.2 | μs |
| <i>Write Mode (Writing data from MPU to ST7066U)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 460 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS, RW, E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS, RW, E | 10 | - | - | ns |
| T _{DSW} | Data Setup Time | Pins: DB0 - DB7 | 80 | - | - | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Read Mode (Reading Data from ST7066U to MPU)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 480 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS, RW, E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS, RW, E | 10 | - | - | ns |
| T _{DDR} | Data Setup Time | Pins: DB0 - DB7 | - | - | 320 | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Interface Mode with LCD Driver(ST7065)</i> | | | | | | |
| T _{CWH} | Clock Pulse with High | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CWL} | Clock Pulse with Low | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CST} | Clock Setup Time | Pins: CL1, CL2 | 500 | - | - | ns |
| T _{SU} | Data Setup Time | Pin: D | 300 | - | - | ns |
| T _{DH} | Data Hold Time | Pin: D | 300 | - | - | ns |
| T _{DM} | M Delay Time | Pin: M | 0 | - | 2000 | ns |

■ AC Characteristics

(TA = 25°C, VCC = 5V)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|--|-----------------------|-----------------|------|------|------|------|
| <i>Internal Clock Operation</i> | | | | | | |
| f _{OSC} | OSC Frequency | R = 91KΩ | 190 | 270 | 350 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f _{EX} | External Frequency | - | 125 | 270 | 410 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T _R , T _F | Rise/Fall Time | - | - | - | 0.2 | μs |
| <i>Write Mode (Writing data from MPU to ST7066U)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 140 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 10 | - | - | ns |
| T _{DSW} | Data Setup Time | Pins: DB0 - DB7 | 40 | - | - | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Read Mode (Reading Data from ST7066U to MPU)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 140 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 10 | - | - | ns |
| T _{DDR} | Data Setup Time | Pins: DB0 - DB7 | - | - | 100 | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Interface Mode with LCD Driver(ST7065)</i> | | | | | | |
| T _{CWH} | Clock Pulse with High | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CWL} | Clock Pulse with Low | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CST} | Clock Setup Time | Pins: CL1, CL2 | 500 | - | - | ns |
| T _{SU} | Data Setup Time | Pin: D | 300 | - | - | ns |
| T _{DH} | Data Hold Time | Pin: D | 300 | - | - | ns |
| T _{DM} | M Delay Time | Pin: M | 0 | - | 2000 | ns |

■ Absolute Maximum Ratings

| Characteristics | Symbol | Value |
|-----------------------|-----------|-------------------------------|
| Power Supply Voltage | V_{CC} | -0.3 to +7.0 |
| LCD Driver Voltage | V_{LCD} | $V_{CC}-10.0$ to $V_{CC}+0.3$ |
| Input Voltage | V_{IN} | -0.3 to $V_{CC}+0.3$ |
| Operating Temperature | T_A | -40°C to + 90°C |
| Storage Temperature | T_{STO} | -55°C to + 125°C |

■ DC Characteristics

($T_A = 25^\circ\text{C}$, $V_{CC} = 2.7\text{ V} - 4.5\text{ V}$)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|------------|---|---|--------------------|------|--------------------|---------------|
| V_{CC} | Operating Voltage | - | 2.7 | - | 4.5 | V |
| V_{LCD} | LCD Voltage | $V_{CC}-V_5$ | 3.0 | - | 10.0 | V |
| I_{CC} | Power Supply Current | $f_{OSC} = 270\text{KHz}$ $V_{CC}=3.0\text{V}$ | - | 0.1 | 0.25 | mA |
| V_{IH1} | Input High Voltage (Except OSC1) | - | 0.7Vcc | - | V_{CC} | V |
| V_{IL1} | Input Low Voltage (Except OSC1) | - | - 0.3 | - | 0.6 | V |
| V_{IH2} | Input High Voltage (OSC1) | - | 0.7Vcc | - | V_{CC} | V |
| V_{IL2} | Input Low Voltage (OSC1) | - | - | - | 0.2Vcc | V |
| V_{OH1} | Output High Voltage (DB0 - DB7) | $I_{OH} = -0.1\text{mA}$ | 0.75 V_{CC} | - | - | V |
| V_{OL1} | Output Low Voltage (DB0 - DB7) | $I_{OL} = 0.1\text{mA}$ | - | - | 0.2Vcc | V |
| V_{OH2} | Output High Voltage (Except DB0 - DB7) | $I_{OH} = -0.04\text{mA}$ | 0.8V _{CC} | - | V_{CC} | V |
| V_{OL2} | Output Low Voltage (Except DB0 - DB7) | $I_{OL} = 0.04\text{mA}$ | - | - | 0.2V _{CC} | V |
| R_{COM} | Common Resistance | $V_{LCD} = 4\text{V}$, $I_d = 0.05\text{mA}$ | - | 2 | 20 | K Ω |
| R_{SEG} | Segment Resistance | $V_{LCD} = 4\text{V}$, $I_d = 0.05\text{mA}$ | - | 2 | 30 | K Ω |
| I_{LEAK} | Input Leakage Current | $V_{IN} = 0\text{V}$ to V_{CC} | -1 | - | 1 | μA |
| I_{PUP} | Pull Up MOS Current | $V_{CC} = 3\text{V}$ | -10 | -50 | -120 | μA |

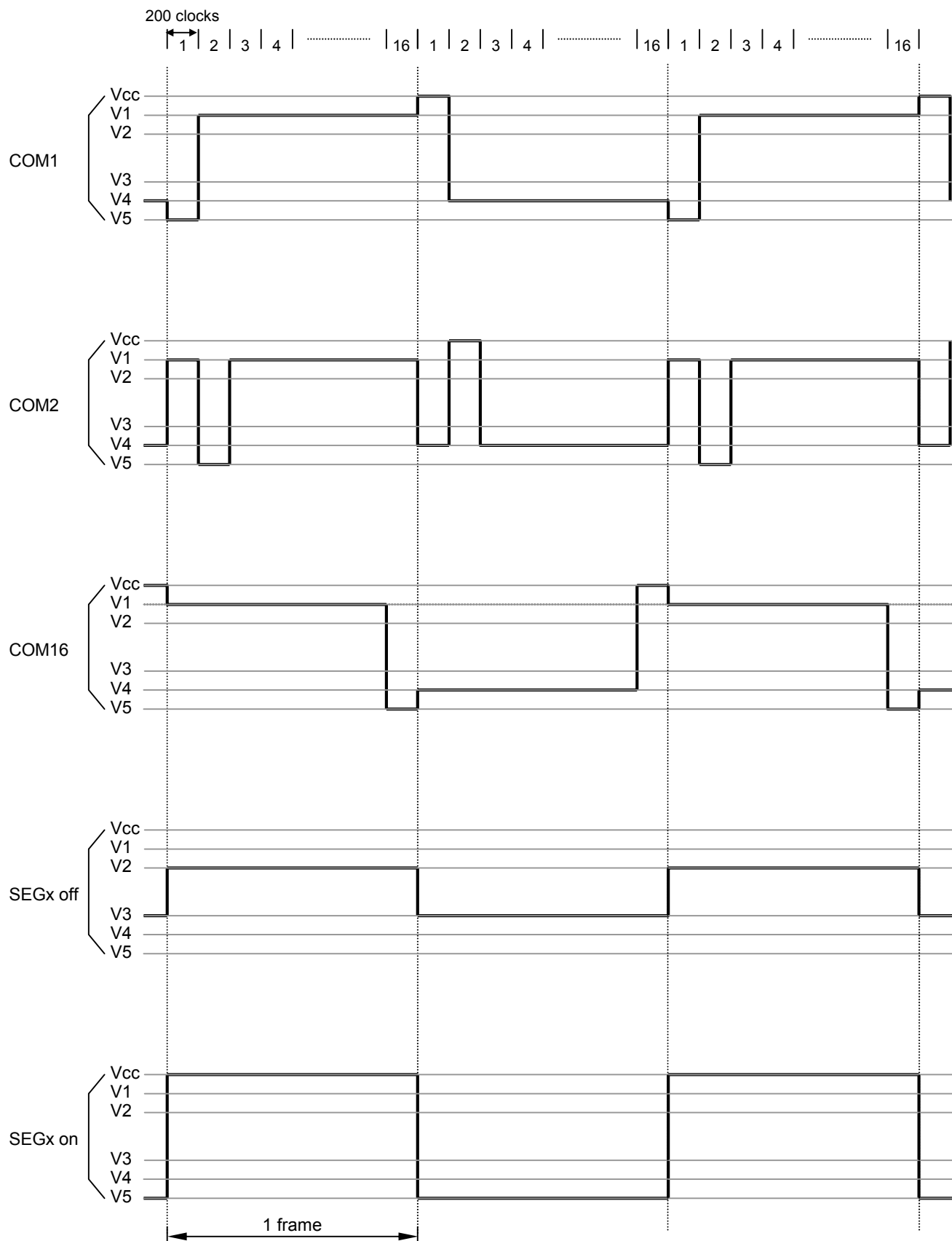
■ DC Characteristics

(TA = 25°C, V_{CC} = 4.5 V - 5.5 V)

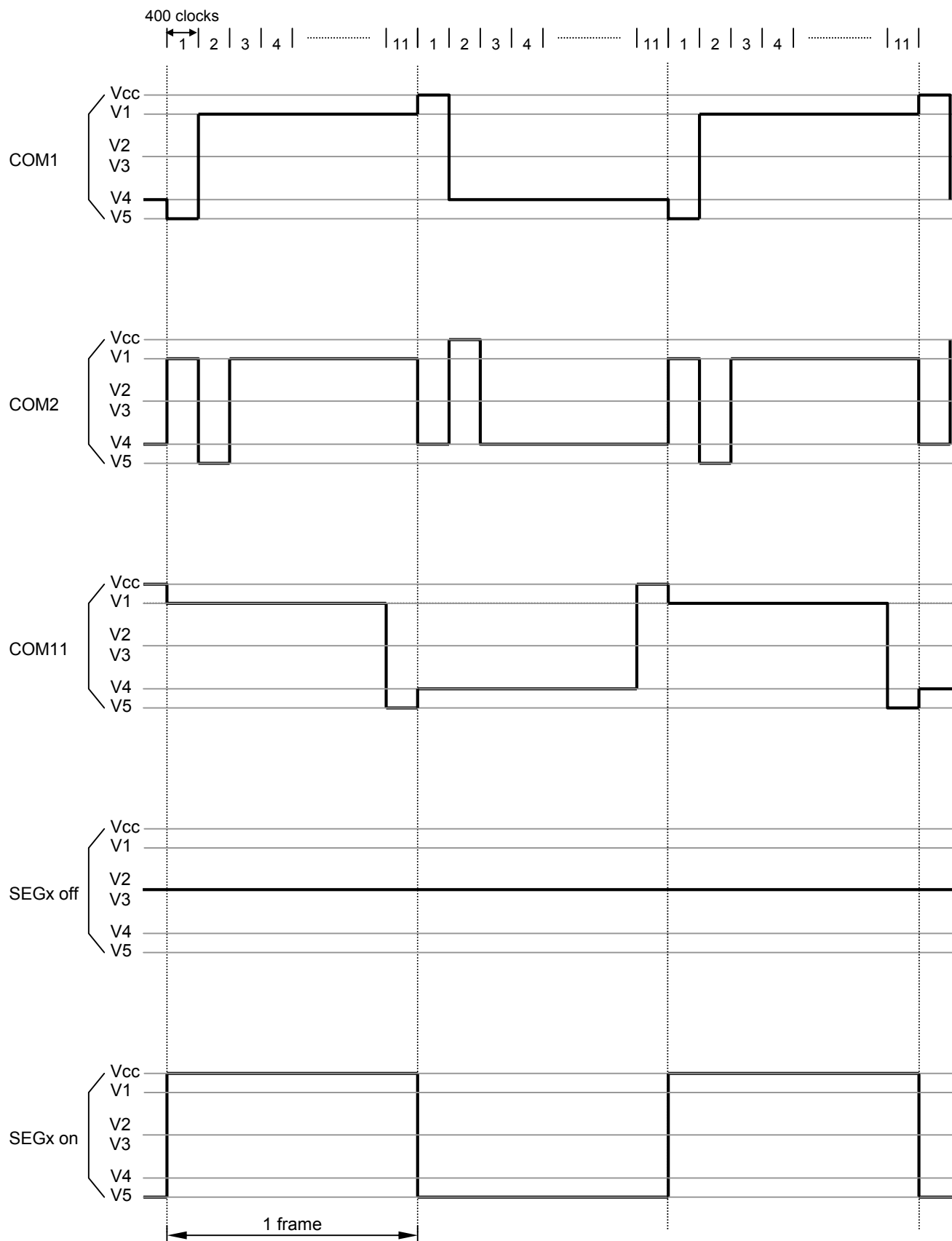
| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|-------------------|---|--|--------------------|------|--------------------|------|
| V _{CC} | Operating Voltage | - | 4.5 | - | 5.5 | V |
| V _{LCD} | LCD Voltage | V _{CC} -V5 | 3.0 | - | 10.0 | V |
| I _{CC} | Power Supply Current | f _{OSC} = 270KHz V _{CC} =5.0V | - | 0.2 | 0.5 | mA |
| V _{IH1} | Input High Voltage (Except OSC1) | - | 0.7V _{CC} | - | V _{CC} | V |
| V _{IL1} | Input Low Voltage (Except OSC1) | - | -0.3 | - | 0.6 | V |
| V _{IH2} | Input High Voltage (OSC1) | - | V _{CC} -1 | - | V _{CC} | V |
| V _{IL2} | Input Low Voltage (OSC1) | - | - | - | 1.0 | V |
| V _{OH1} | Output High Voltage (DB0 - DB7) | I _{OH} = -0.1mA | 3.9 | - | V _{CC} | V |
| V _{OL1} | Output Low Voltage (DB0 - DB7) | I _{OL} = 0.1mA | - | - | 0.4 | V |
| V _{OH2} | Output High Voltage (Except DB0 - DB7) | I _{OH} = -0.04mA | 0.9V _{CC} | - | V _{CC} | V |
| V _{OL2} | Output Low Voltage (Except DB0 - DB7) | I _{OL} = 0.04mA | - | - | 0.1V _{CC} | V |
| R _{COM} | Common Resistance | V _{LCD} = 4V, I _d = 0.05mA | - | 2 | 20 | KΩ |
| R _{SEG} | Segment Resistance | V _{LCD} = 4V, I _d = 0.05mA | - | 2 | 30 | KΩ |
| I _{LEAK} | Input Leakage Current | V _{IN} = 0V to V _{CC} | -1 | - | 1 | μA |
| I _{PUP} | Pull Up MOS Current | V _{CC} = 5V | -50 | -110 | -180 | μA |

■ LCD Frame Frequency

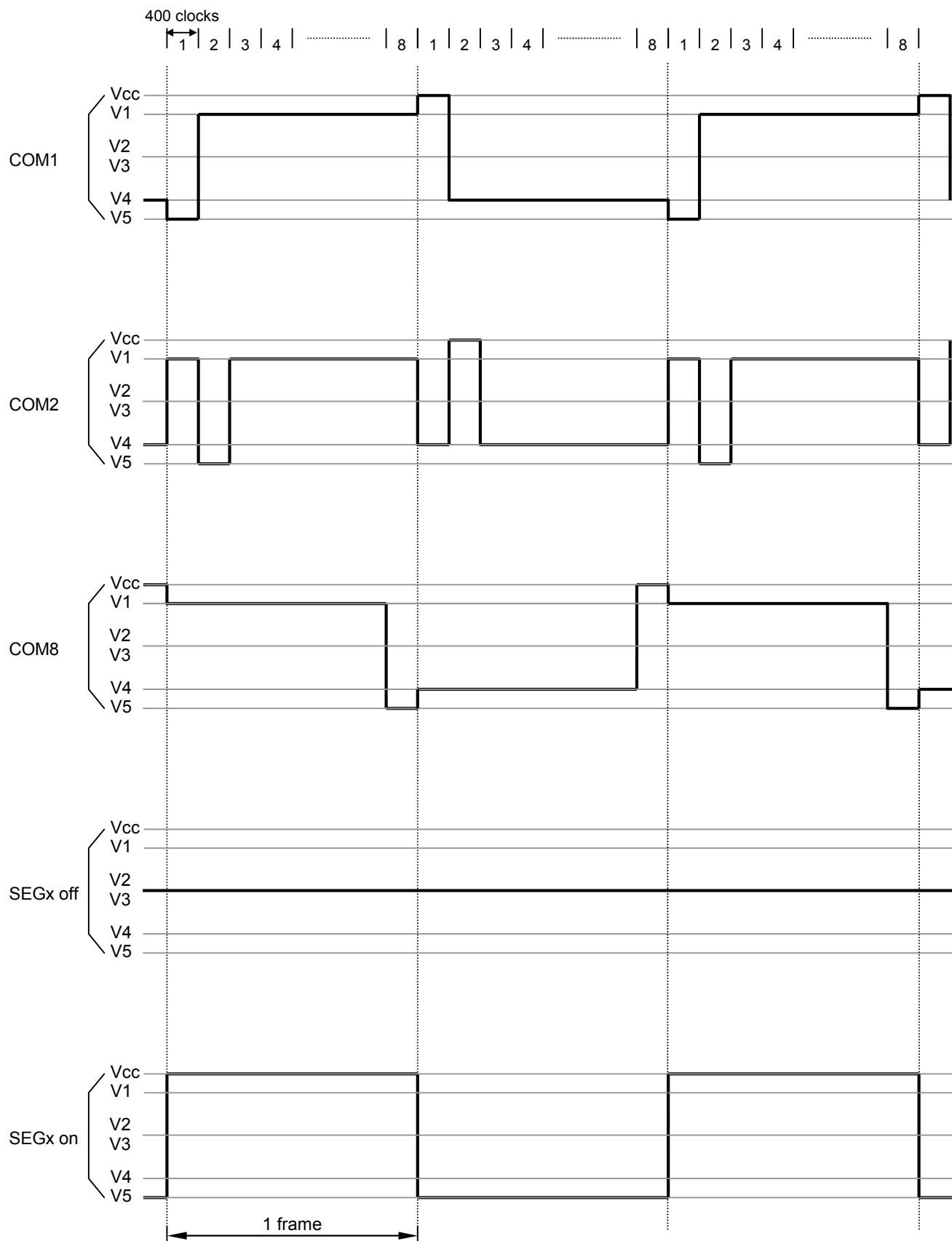
- Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/16 duty; 1/5 bias, 1 frame
 $= 3.7\mu s \times 200 \times 16 = 11840\mu s = 11.8ms (84.7Hz)$



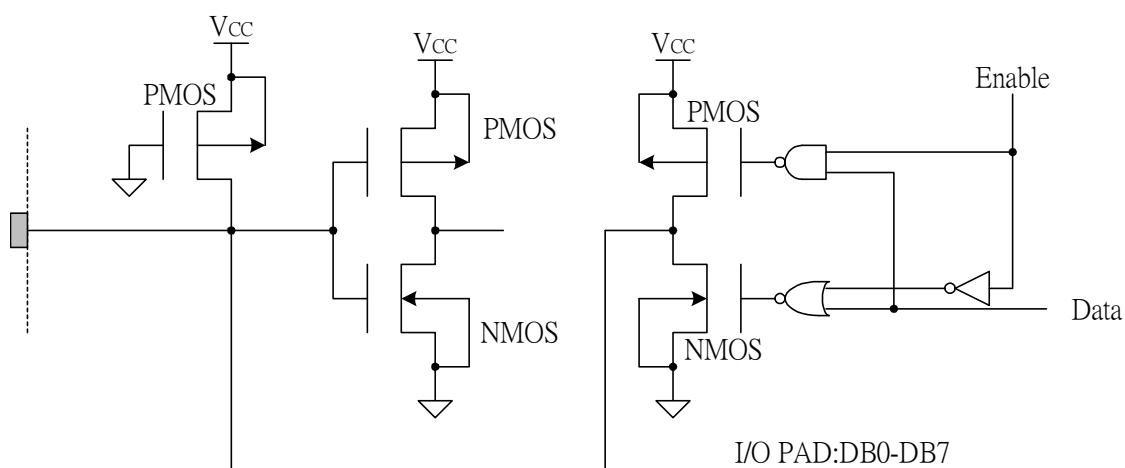
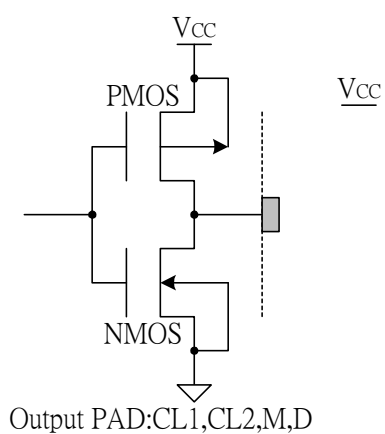
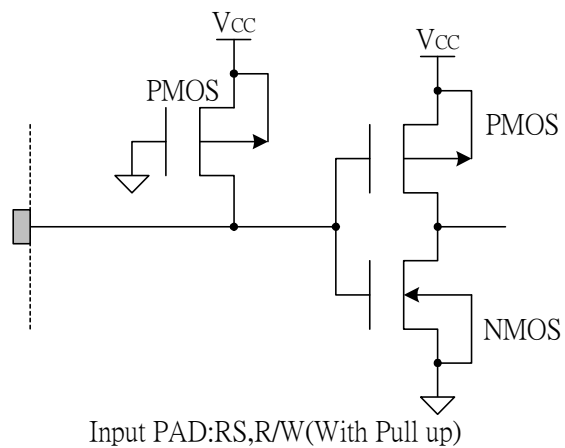
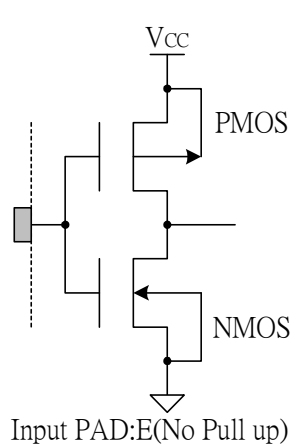
- Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/11 duty; 1/4 bias, 1 frame = 3.7us x 400 x 11 = 16280us=16.3ms (61.3Hz)



- Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/8 duty; 1/4 bias, 1 frame = 3.7us x 400 x 8 = 11840us=11.8ms (84.7Hz)

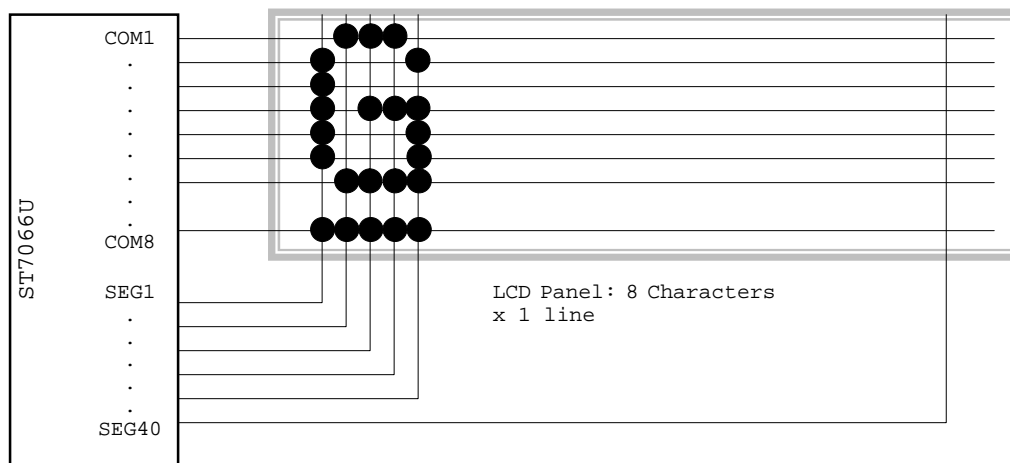


■ I/O Pad Configuration

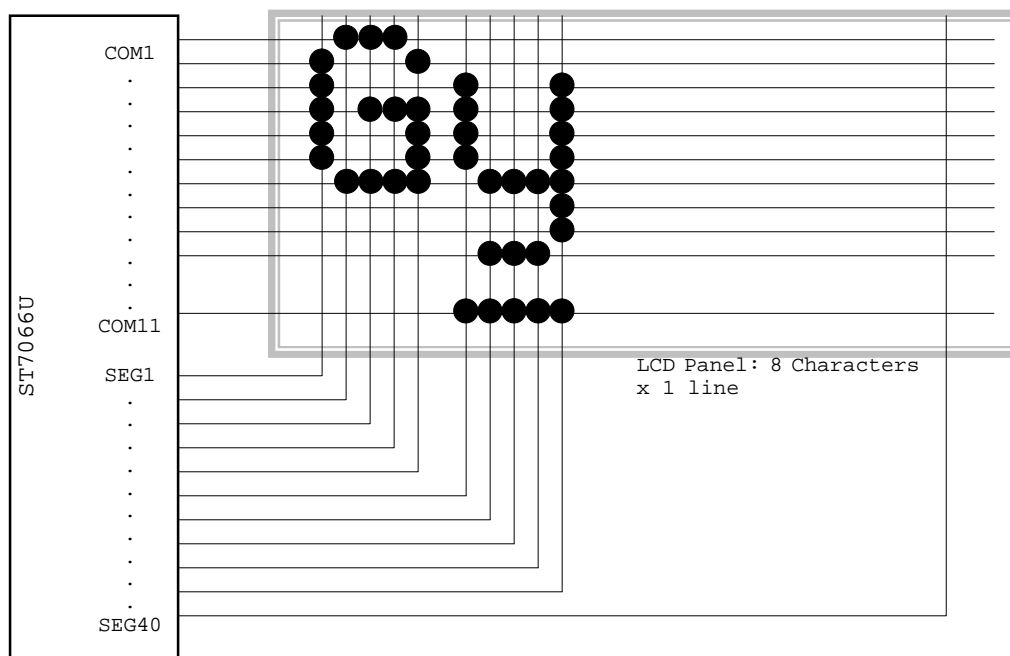


■ LCD and ST7066U Connection

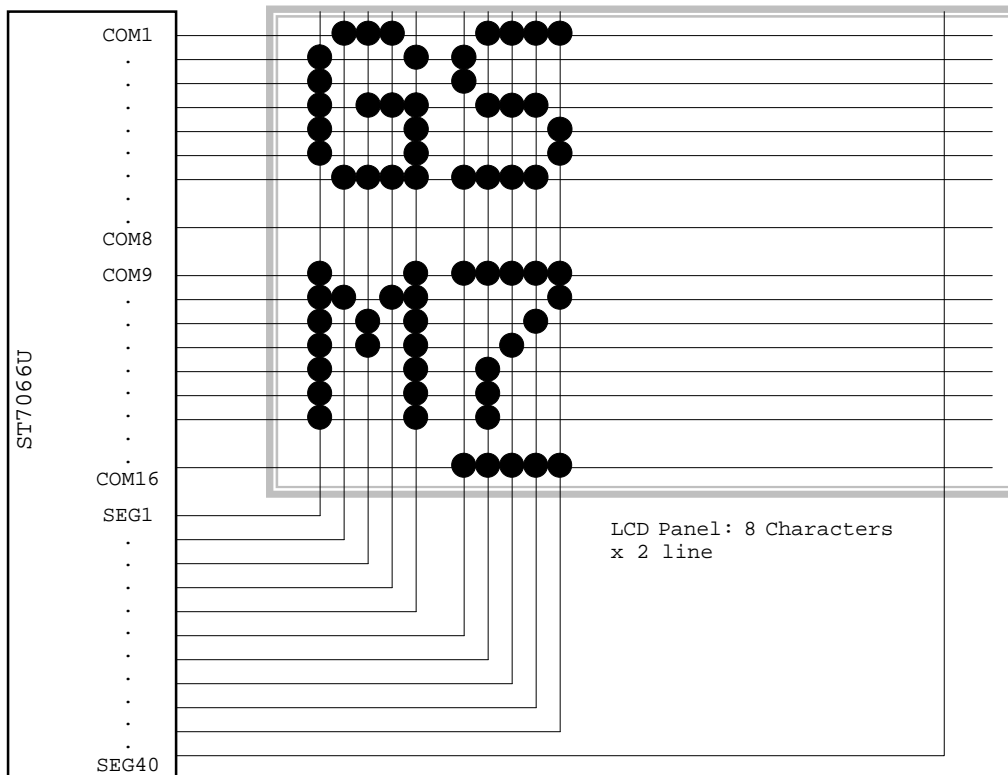
1. 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



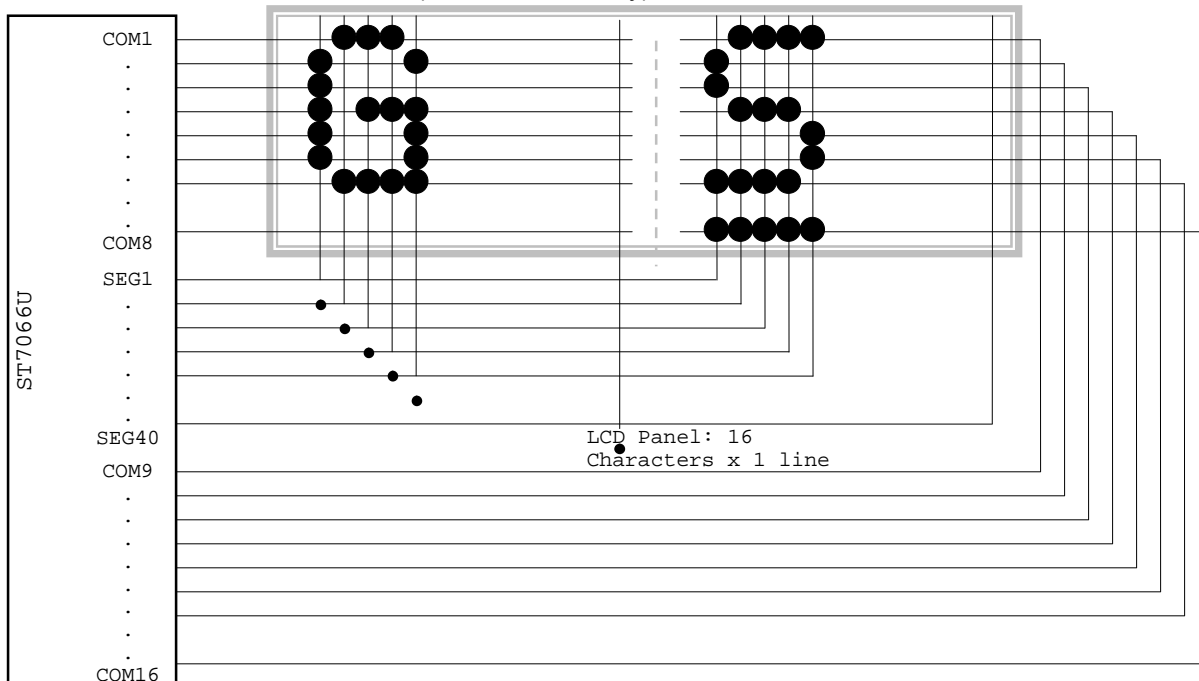
2. 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



3. 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



4. 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



■ Application Circuit

