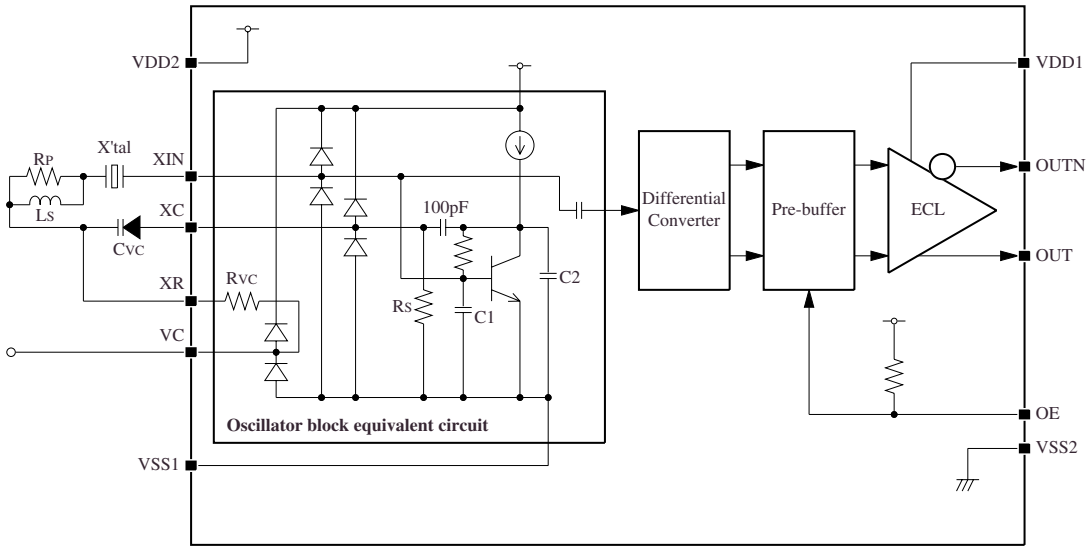
OVERVIEW

The CF5072BA is 155MHz VCXO IC. It incorporates a 155.52MHz fundamental frequency oscillator circuit and a differential LVPECL output circuit on a single chip. The oscillator circuit features characteristics optimized for VCXO operation, and includes a varicap connection pin. The CF5072BA can be configured with few external components, making them ideal as miniature VCXO modules.

FEATURES

- 3.0 to 3.6V operating supply voltage range
- 70MHz to 200MHz oscillator frequency range
- Differential LVPECL output
- 50 ± 5% output duty
  (measured at the output crossing point)
- Output enable function
  High impedance output when OE = LOW
  (oscillator continues running)
- –40 to 85°C operating temperature range
- Chip form (CF5072BA)

BLOCK DIAGRAM



ESD sensitive device:
The XR pin is not equipped with a protection circuit. Accordingly, its electrostatic withstand voltage is significantly lower than that of the other pins.
ESD breakdown prevention handling precautions are strongly recommended.

ORDERING INFORMATION

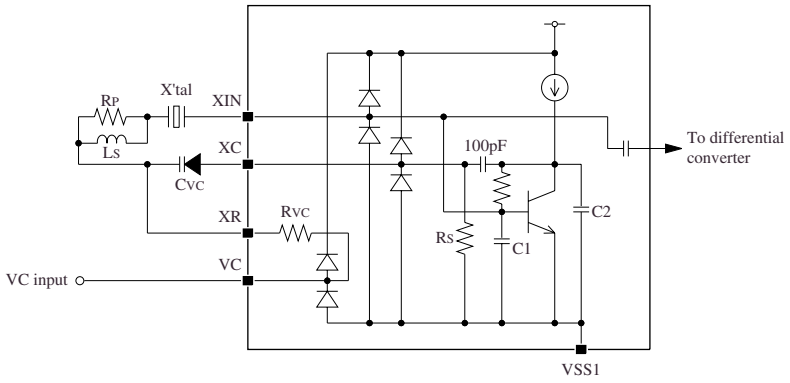
Device	Package
CF5072BA–1	Chip form

FUNCTIONAL DESCRIPTION

Oscillator Equivalent Circuit

The oscillator can be represented by the equivalent circuit shown below. The crystal unit is connected to XIN, and the other terminal is connected to the L_S and R_P network. A varicap is added with cathode connected to XR, and anode connected to XC.

The control voltage is applied to the VC pin, with high-resistance element connected between VC and XR built-in.



Note. R_P is a damping resistor to prevent parasitic oscillation due the combined effects of the external inductor (expander coil) and varicap capacitance/internal capacitance. It is recommended that R_P be connected in parallel with L_S.

Oscillator internal capacitors (design value)

Version	Internal capacitance [pF] (design value)	
	C1	C2
CF5072BA	11.2	14.4

Selecting external constants

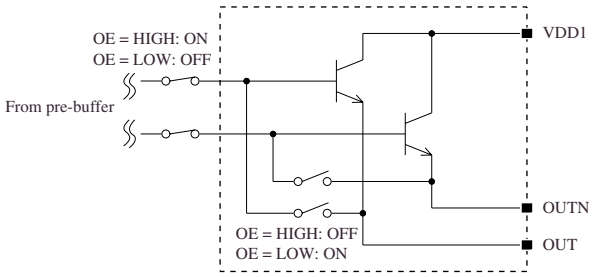
The L_S and R_P values should be selected such that both (a) the resonance point in the loop formed by L_S and C0, C_L, C_{VC} is higher than the crystal oscillator frequency, and (b) the resonance point does not satisfy the oscillation condition. (C0 is the crystal shunt capacitance, C_L is the oscillator equivalent circuit capacitance, and C_{VC} is the varicap capacitance.)

In the oscillator circuit, if the crystal capacitance C0 is 2.85pF, the varicap (C_{VC}) is a HVC350B (Renesas), and the oscillator frequency is 155.52MHz, then values in the order L_S = 220nH, R_P = 2.2kΩ or L_S = 180nH, R_P = 1.8kΩ will satisfy the conditions above. The optimal values for L_S and R_P will vary with crystal characteristics, oscillator frequency, and varicap diode, thus the values selected should be thoroughly evaluated.

Output Circuit

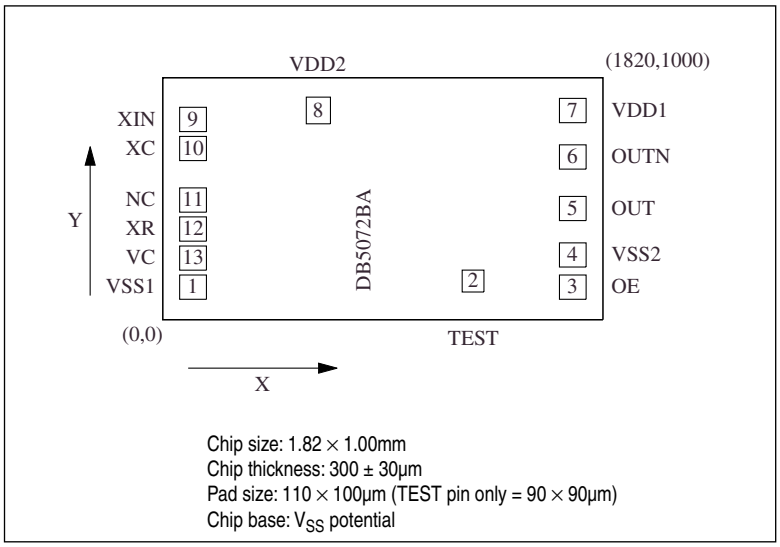
The output is enabled/disabled using the OE pin. Outputs are high impedance when disabled. The OE pin logic is shown in the following table.

OE	OUT	OUTN
HIGH or open	CLK output	CLK output
LOW	High impedance	High impedance



PAD LAYOUT

(Unit: µm)



Chip size: 1.82 × 1.00mm
Chip thickness: 300 ± 30µm
Pad size: 110 × 100µm (TEST pin only = 90 × 90µm)
Chip base: V_{SS} potential

PAD DESCRIPTION AND DIMENSIONS

Pad No.	Name	I/O	Function	Pad dimensions [µm]		Pad size [µm]	
				X	Y	X	Y
1	VSS1	–	Oscillator ground	125	135	110	100
2	TEST	I	IC test pin (leave open circuit for normal operation)	1283	160	90	90
3	OE	I	Output enable, with pull-up resistor built-in	1695	135	110	100
4	VSS2	–	Ground	1695	268	110	100
5	OUT	O	Differential PECL non-inverting output (true)	1695	460	110	100
6	OUTN	O	Differential PECL inverting output (complementary)	1695	673	110	100
7	VDD1	–	ECL buffer supply	1695	865	110	100
8	VDD2	–	Supply	643	865	100	110
9	XIN	I	Crystal unit connection	125	828	110	100
10	XC	I	Varicap anode connection	125	708	110	100
11	NC	–	No connection	125	495	110	100
12	XR[1]	I	Varicap cathode connection and inductor connection	125	375	110	100
13	VC	I	Control voltage pin	125	255	110	100

1. The XR pin electrostatic withstand voltage is weaker than the other pins. The electrostatic withstand voltage of pins, excluding XR, is the same as that for existing NPC devices.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range	V_{DD}		V_{SS} – 0.5 to V_{SS} + 7.0	V
Input voltage range	V_{IN}		V_{SS} – 0.5 to V_{DD} + 0.5	V
Storage temperature range	T_{STG}		–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Supply voltage	V_{DD}		3.0	–	3.6	V
Operating temperature	T_{OPR}		–40	–	85	°C
Output load	R_L	Terminated to V_{DD} – 2V	–	50	–	Ω
Output frequency	f_{OUT}		70	–	200	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

Recommended operating conditions apply unless otherwise noted

Parameter	Symbol	Conditions		Rating			Unit
				Min	Typ	Max	
Current consumption	I_{DD}	Measurement circuit 1, output terminated to V_{DD} – 2V, OE = OPEN		–	50	88	mA
OUT/OUTN HIGH-level output voltage	V_{OH}	Measurement circuit 2, V_{DD} = 3.3V, OE = OPEN	Ta = 0 to 85°C	2.275	2.350	2.420	V
			Ta = –40°C	2.215	2.295	2.420	V
OUT/OUTN LOW-level output voltage	V_{OL}		Ta = 0 to 85°C	1.490	1.600	1.680	V
			Ta = –40°C	1.470	1.605	1.745	V
OE HIGH-level input voltage	V_{IH}	Measurement circuit 3		$0.7V_{CC}$	–	–	V
OE LOW-level input voltage	V_{IL}	Measurement circuit 3		–	–	$0.3V_{CC}$	V
OE LOW-level input current	I_{IL}	Measurement circuit 4, V_{IL} = 0V		–	–	–20	µA
Input impedance	Z_{IN}	Measurement circuit 5, measured between supply and VC		10	–	–	MΩ
VC resistance	R_{VC}	Measurement circuit 6, measured between VC and XR		100	150	200	kΩ
Pull-down resistance	R_S	Measurement circuit 7, measured between VSS and XC		10	20	40	kΩ

AC Characteristics

Recommended operating conditions apply unless otherwise noted

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Output duty cycle 1	Duty1	Measurement circuit 1, measured at output crossing point, Ta = 25°C, V_{DD} = 3.3V	45	50	55	%
Output duty cycle 2	Duty2	Measurement circuit 1, measured at 50% output swing, Ta = 25°C, V_{DD} = 3.3V	45	50	55	%
Output swing	V_{Opp}	Measurement circuit 1, peak-to-peak of output waveform	0.4	–	–	V
Output rise time	t_r	Measurement circuit 1, output swing 20% to 80%	–	0.5	1	ns
Output fall time	t_f	Measurement circuit 1, output swing 80% to 20%	–	0.5	1	ns
Output enable delay time	t_{OE}	Measurement circuit 3, Ta = 25°C	–	–	200	ns
Output disable delay time	t_{OD}	Measurement circuit 3, Ta = 25°C	–	–	200	ns

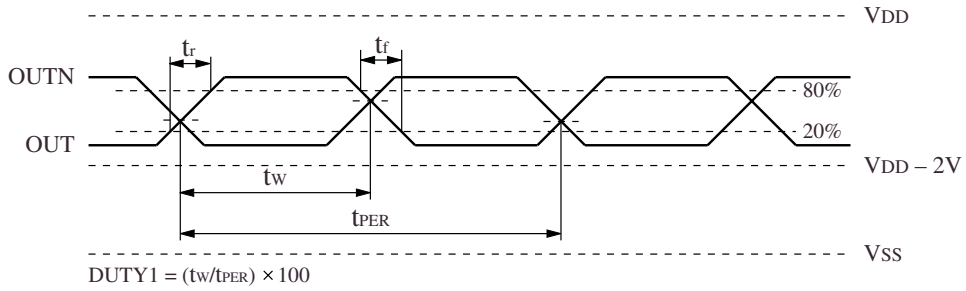


Figure 1. PECL output waveform

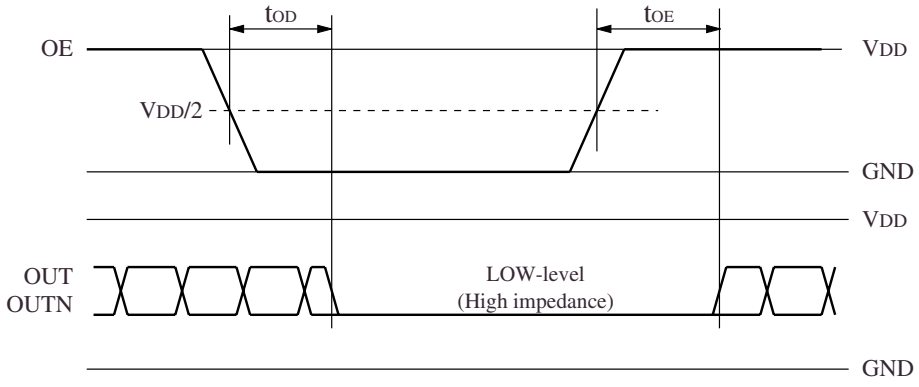
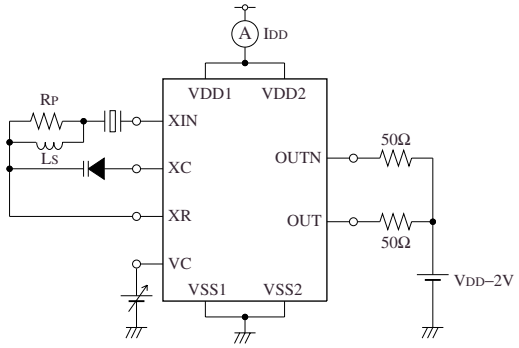


Figure 2. OE timing waveform (Differential LVPECL)

MEASUREMENT CIRCUITS

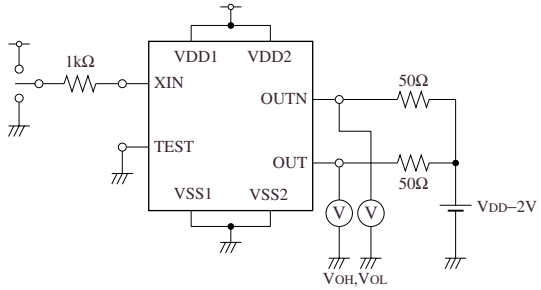
Measurement Circuit 1

Parameters: I_{DD}, Duty1, Duty2, V_{Opp}, t_r, t_f



Measurement Circuit 2

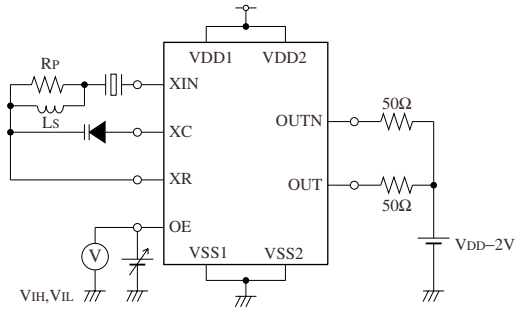
Parameters: V_{OH}, V_{OL}



When XIN = HIGH: OUT is tied LOW (V_{OL})
OUTN is tied HIGH (V_{OH})
When XOUT = LOW: OUT is tied HIGH (V_{OH})
OUTN is tied LOW (V_{OL})

Measurement Circuit 3

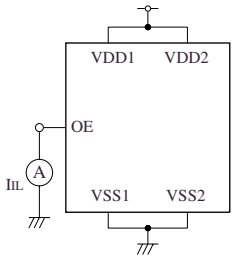
Parameters: V_{IH}, V_{IL}, t_{OE}, t_{OD}



V_{IH}: output state changes $V_{SS} \rightarrow V_{DD}$
V_{IL}: output state changes $V_{DD} \rightarrow V_{SS}$
OE: disable function

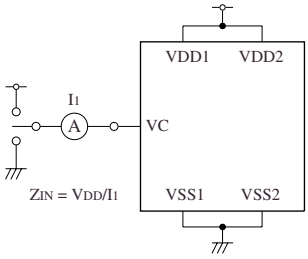
Measurement Circuit 4

Parameter: I_{IL}



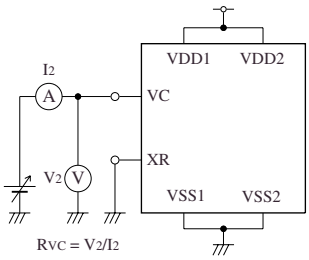
Measurement Circuit 5

Parameter: Z_{IN}



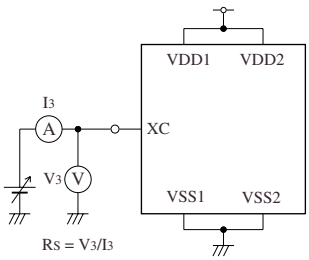
Measurement Circuit 6

Parameter: R_{VC}



Measurement Circuit 7

Parameter: R_S



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