

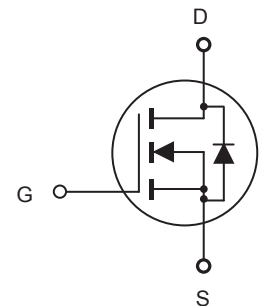


CED02N65G/CEU02N65G

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 650V, 1.8A, $R_{DS(ON)} = 5.5\Omega$ @ $V_{GS} = 10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	1.8	A
		1.1	A
Drain Current-Pulsed ^a	I_{DM}	7.2	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	48	W
		0.38	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^e	E_{AS}	11.25	mJ
Single Pulsed Avalanche Current ^e	I_{AS}	1.5	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.6	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$



CED02N65G/CEU02N65G

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 0.9A$		4.4	5.5	Ω
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		295		pF
Output Capacitance	C_{oss}			75		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 18\Omega$		19	38	ns
Turn-On Rise Time	t_r			11	22	ns
Turn-Off Delay Time	$t_{d(off)}$			29	58	ns
Turn-Off Fall Time	t_f			10	20	ns
Total Gate Charge	Q_g	$V_{DS} = 480V, I_D = 1A, V_{GS} = 10V$		6.7	8.9	nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			3		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S				1.8	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 1A$			1.5	V
Notes :□ a.Repetitive Rating : Pulse width limited by maximum junction temperature.□ b.Device Mounted on FR4 Board, $t < 10\text{ sec.}$□ c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.□ d.Guaranteed by design, not subject to production testing.□ e.L = 10mH, $I_{AS} = 1.5A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25\text{ C}$						



CED02N65G/CEU02N65G

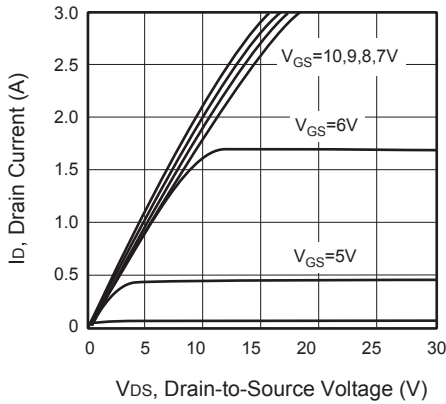


Figure 1. Output Characteristics

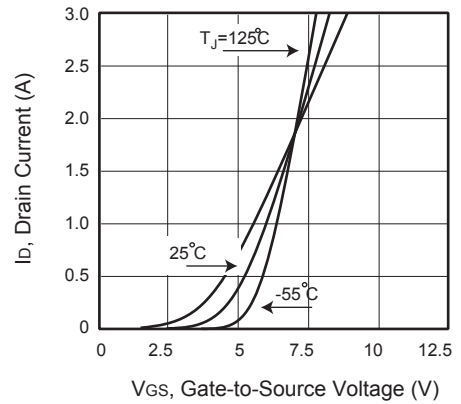


Figure 2. Transfer Characteristics

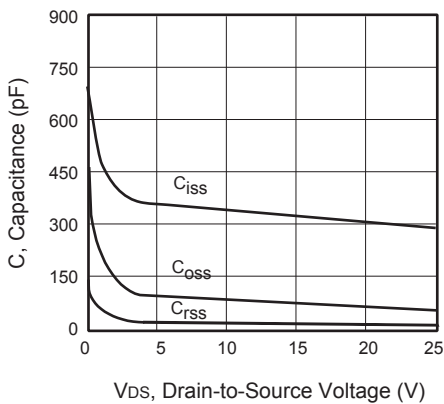


Figure 3. Capacitance

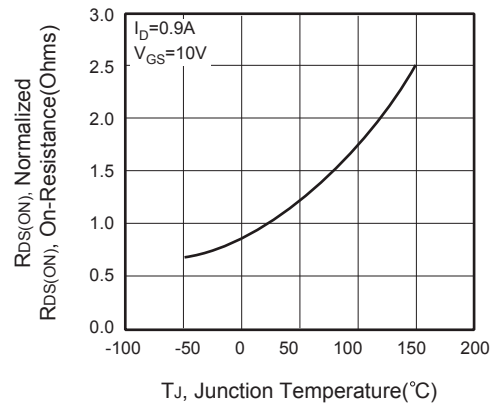


Figure 4. On-Resistance Variation with Temperature

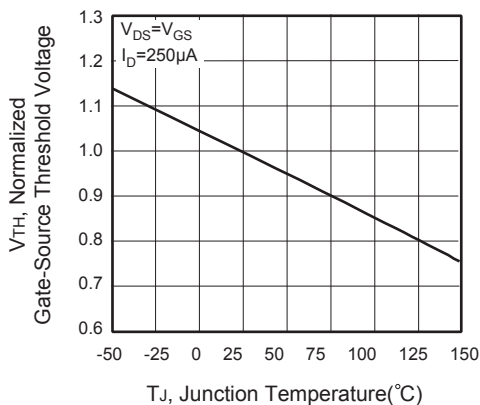


Figure 5. Gate Threshold Variation with Temperature

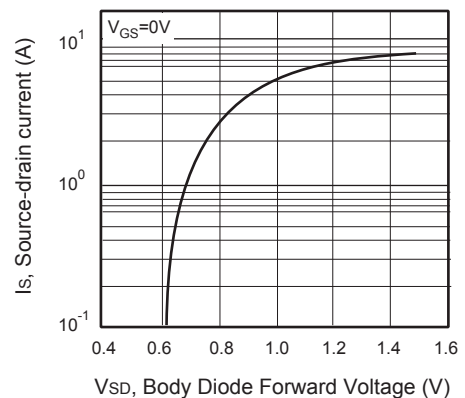


Figure 6. Body Diode Forward Voltage Variation with Source Current



CED02N65G/CEU02N65G

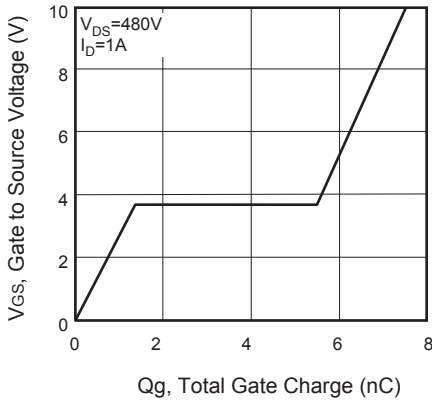


Figure 7. Gate Charge

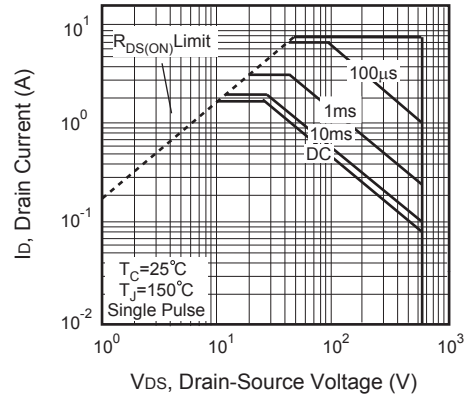


Figure 8. Maximum Safe Operating Area

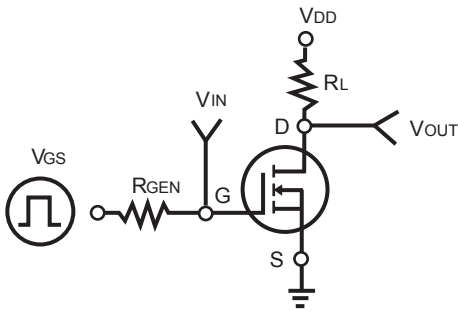


Figure 9. Switching Test Circuit

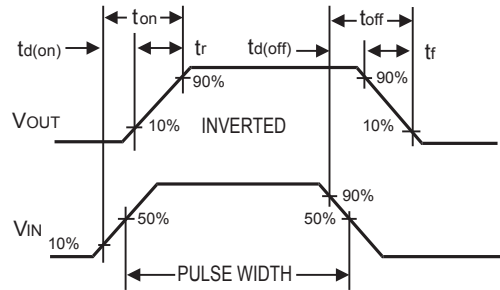


Figure 10. Switching Waveforms

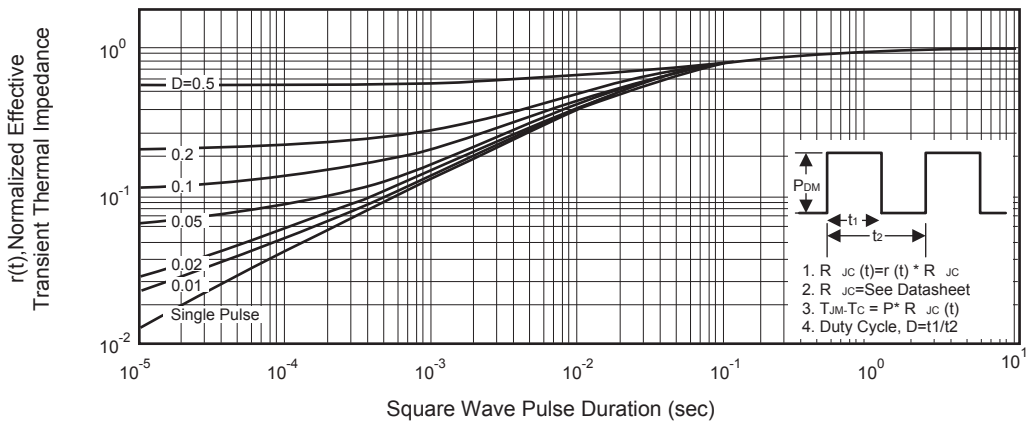


Figure 11. Normalized Thermal Transient Impedance Curve