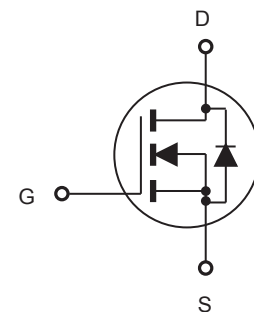
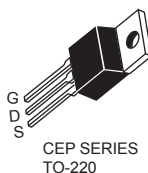


N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 40V, 180A, $R_{DS(ON)} = 5m\Omega$ @ $V_{GS} = 10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	$I_D @ T_C = 25^\circ\text{C}$	180	A
	$I_D @ T_C = 100^\circ\text{C}$	125	A
Drain Current-Pulsed ^a	I_{DM}	720	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	200	W
		1.3	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^d	E_{AS}	633	mJ
Single Pulsed Avalanche Current ^d	I_{AS}	65	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.75	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$			25	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 70A$		4.2	5	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 25V, I_D = 70A$		30		S
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		3390		pF
Output Capacitance	C_{oss}			1445		pF
Reverse Transfer Capacitance	C_{rss}			185		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 28V, I_D = 10A,$ $V_{GS} = 10V, R_{GEN} = 4.5\Omega$		32	64	ns
Turn-On Rise Time	t_r			20	40	ns
Turn-Off Delay Time	$t_{d(off)}$			82	164	ns
Turn-Off Fall Time	t_f			35	70	ns
Total Gate Charge	Q_g	$V_{DS} = 32V, I_D = 70A,$ $V_{GS} = 10V$		110	143	nC
Gate-Source Charge	Q_{gs}			14.4		nC
Gate-Drain Charge	Q_{gd}			44.4		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				180	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 70A$			1.3	V
Notes : ^a Repetitive Rating : Pulse width limited by maximum junction temperature ^b Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$ ^c Guaranteed by design, not subject to production testing. ^d L = 0.3mH, $I_{AS} = 65A$, $V_{DD} = 25V$, $R_G = 25\Omega$, Starting $T_j = 25\text{ C}$						

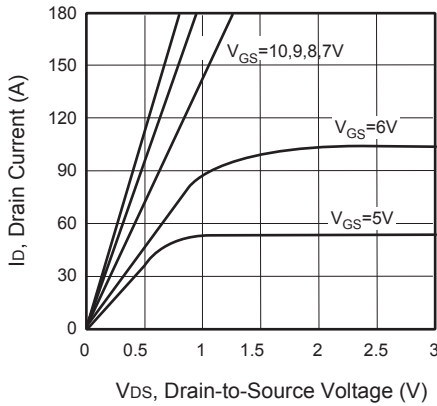


Figure 1. Output Characteristics

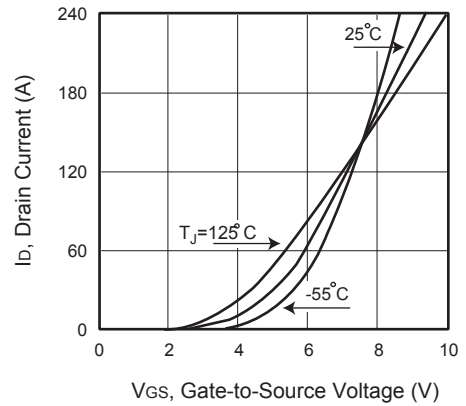


Figure 2. Transfer Characteristics

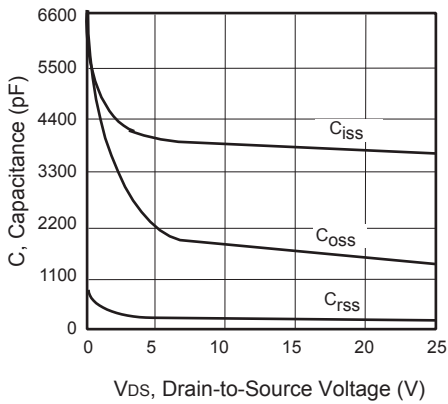


Figure 3. Capacitance

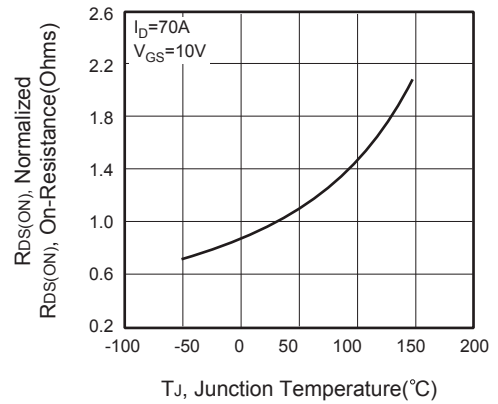


Figure 4. On-Resistance Variation with Temperature

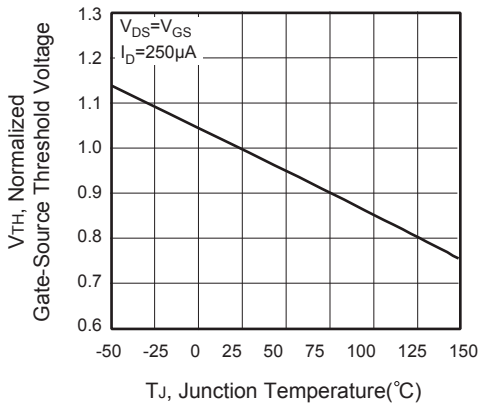


Figure 5. Gate Threshold Variation with Temperature

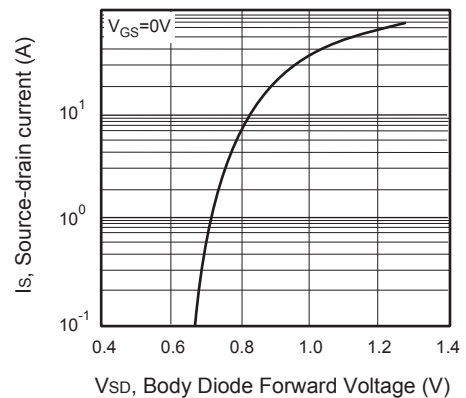


Figure 6. Body Diode Forward Voltage Variation with Source Current



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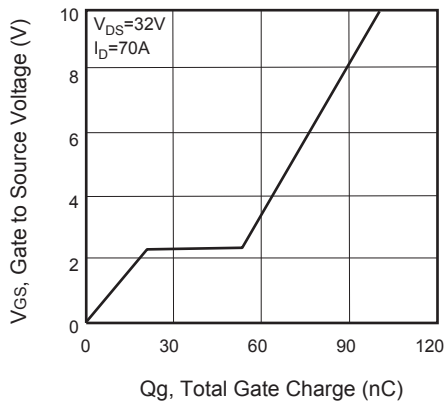


Figure 7. Gate Charge

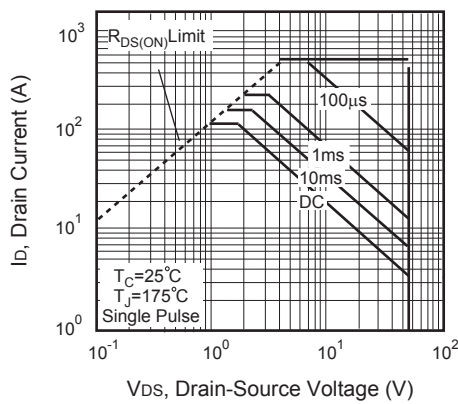


Figure 8. Maximum Safe Operating Area

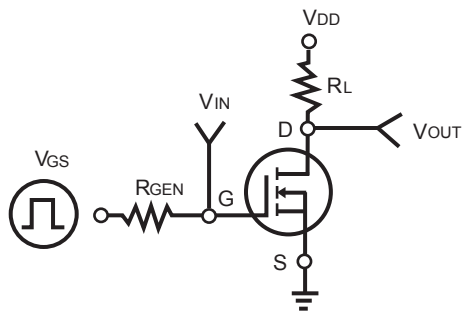


Figure 9. Switching Test Circuit

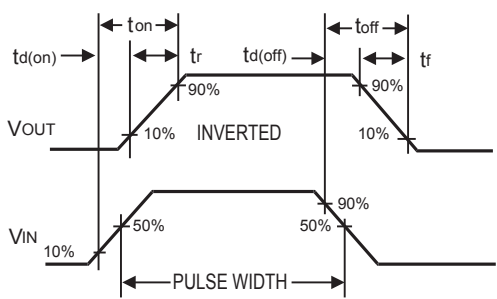


Figure 10. Switching Waveforms

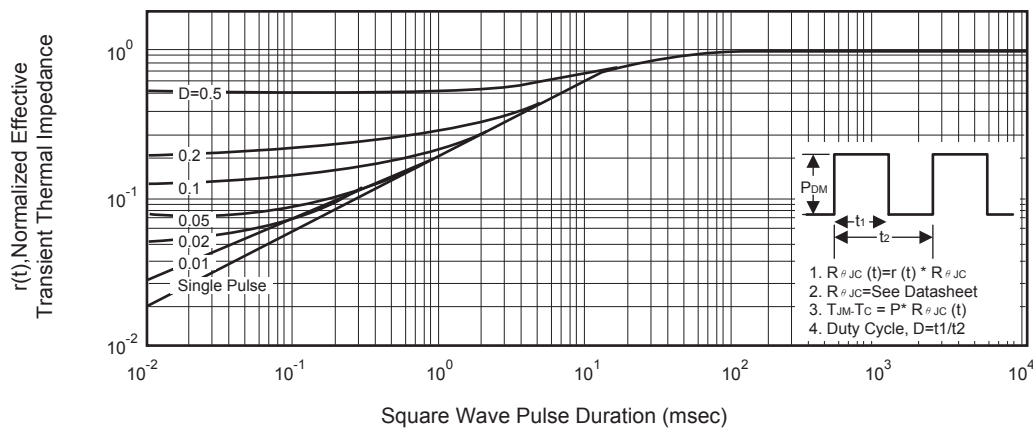


Figure 11. Normalized Thermal Transient Impedance Curve