

CET

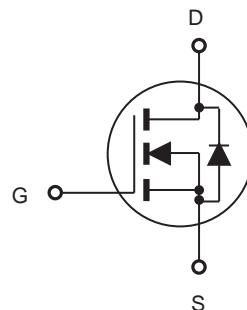
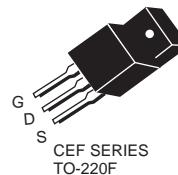
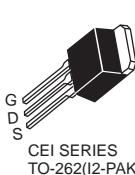
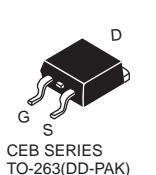
CEPF634/CEBF634 CEIF634/CEFF634

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEPF634	250V	0.45Ω	8.1A	10V
CEBF634	250V	0.45Ω	8.1A	10V
CEIF634	250V	0.45Ω	8.1A	10V
CEFF634	250V	0.45Ω	8.1A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handing capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V _{DS}	250		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current-Continuous	I _D	8.1	8.1 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	32	32 ^d	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P _D	74 0.59	38 0.3	W W/°C
Operating and Store Temperature Range	T _{J,Tstg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	1.7	3.3	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	250			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 250\text{V}, V_{\text{GS}} = 0\text{V}$			25	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{\text{GS}} = 30\text{V}, V_{\text{DS}} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	2		4	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 5.1\text{A}$			0.45	Ω
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 50\text{V}, I_D = 5.1\text{A}$		4.4		S
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		630		pF
Output Capacitance	C_{oss}			100		pF
Reverse Transfer Capacitance	C_{rss}			40		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 125\text{V}, I_D = 5.6\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 12\Omega$		19	40	ns
Turn-On Rise Time	t_r			11	30	ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			46	90	ns
Turn-Off Fall Time	t_f			10	30	ns
Total Gate Charge	Q_g	$V_{\text{DS}} = 200\text{V}, I_D = 5.6\text{A}, V_{\text{GS}} = 10\text{V}$		26	33	nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			11		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S ^f				8.1	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_S = 8.1\text{A}$		0.9	1.5	V

Notes :

- a.Repetitive Rating : Pulse width limited by maximum junction temperature .
- b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- c.Guaranteed by design, not subject to production testing.
- d.Limited only by maximum temperature allowed .
- e .Pulse width limited by safe operating area .
- f.Full package $I_{\text{S}(\text{max})} = 6\text{A}$.

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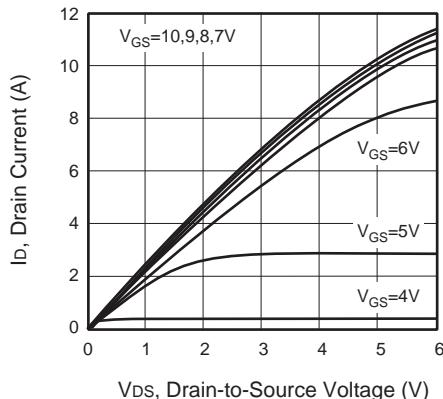


Figure 1. Output Characteristics

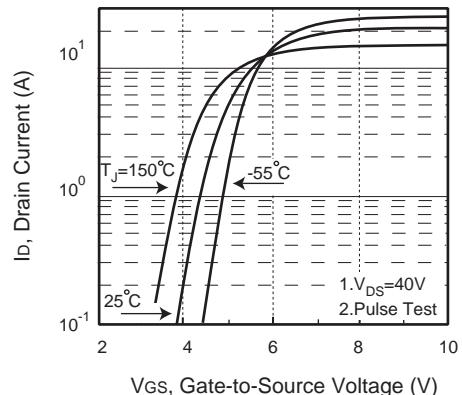


Figure 2. Transfer Characteristics

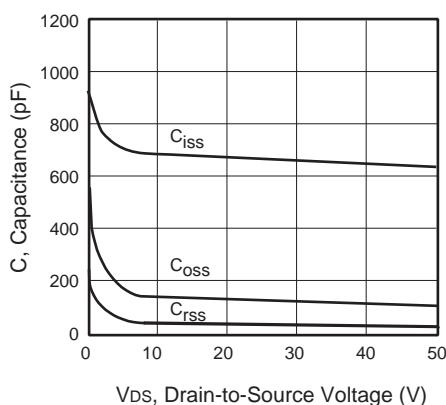


Figure 3. Capacitance

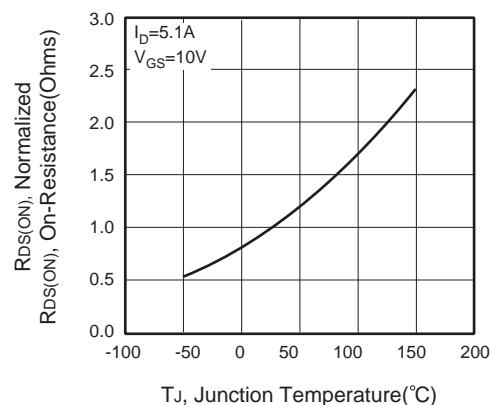


Figure 4. On-Resistance Variation with Temperature

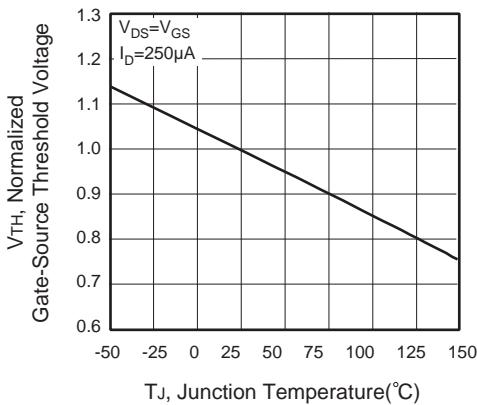


Figure 5. Gate Threshold Variation with Temperature

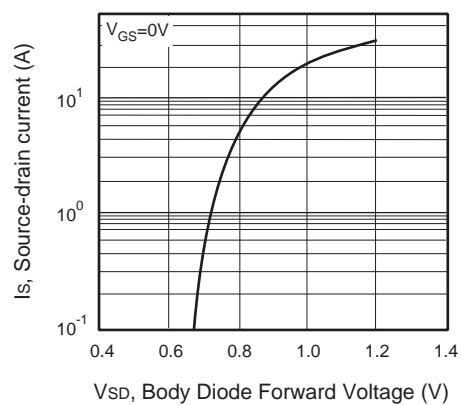


Figure 6. Body Diode Forward Voltage Variation with Source Current

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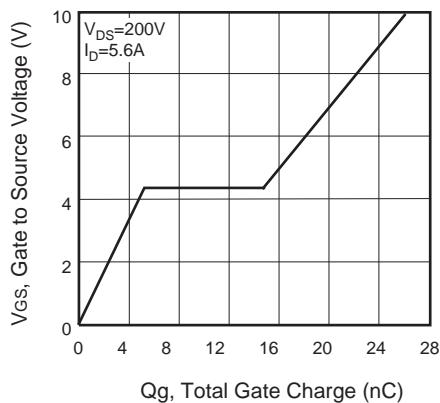


Figure 7. Gate Charge

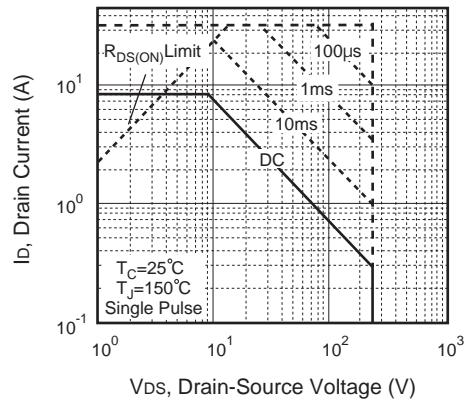


Figure 8. Maximum Safe Operating Area

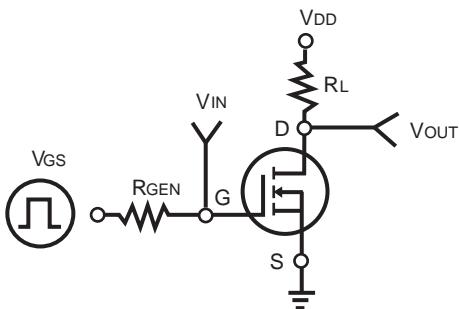


Figure 9. Switching Test Circuit

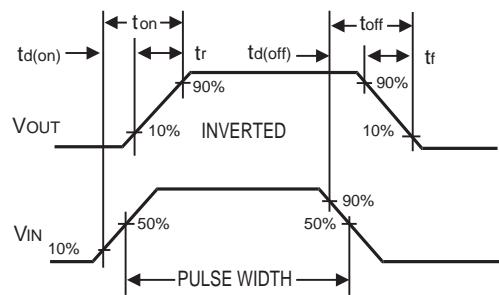


Figure 10. Switching Waveforms

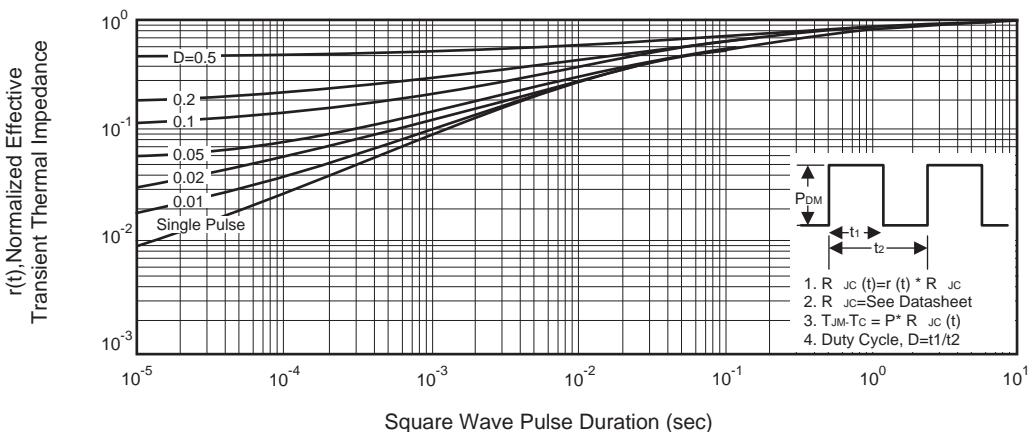


Figure 11. Normalized Thermal Transient Impedance Curve