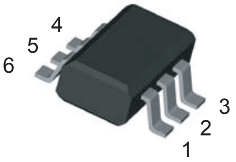
CEH2608

Dual Enhancement Mode Field Effect Transistor (N Channel)

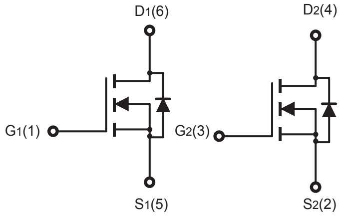
PRELIMINARY

FEATURES

- 20V, 3.8A, $R_{DS(ON)}$ = 50mΩ @V_{GS} = 4.5V.
  $R_{DS(ON)}$ = 70mΩ @V_{GS} = 2.5V.
  $R_{DS(ON)}$ = 100mΩ @V_{GS} = 1.8V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead-free plating ; RoHS compliant.
- Surface mount Package.



TSOP-6



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	3.8	A
Drain Current-Pulsed [a]	I_{DM}	15.2	A
Maximum Power Dissipation	P_D	1.14	W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	110	°C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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N-Channel Electrical Characteristics $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	µA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250µA	0.4		1.2	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 3.8A		30	50	mΩ
		V_{GS} = 2.5V, I_D = 3.0A		40	70	mΩ
		V_{GS} = 1.8V, I_D = 2.0A		60	100	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V, f = 1.0 MHz		330		pF
Output Capacitance	C_{oss}			90		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 3.5A, V_{GS} = 4.5V, R_{GEN} = 6Ω		10	20	ns
Turn-On Rise Time	t_r			6	12	ns
Turn-Off Delay Time	$t_{d(off)}$			28	56	ns
Turn-Off Fall Time	t_f			15	30	ns
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 3.5A, V_{GS} = 4.5V		5		nC
Gate-Source Charge	Q_{gs}			1.0		nC
Gate-Drain Charge	Q_{gd}			1.5		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1A			1.1	V

Notes :

a.Repetitive Rating : Pulse width limited by maximum junction temperature.

b.Surface Mounted on FR4 Board, t ≤ 10 sec.

c.Pulse Test : Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

d.Guaranteed by design, not subject to production testing.

N-CHANNEL

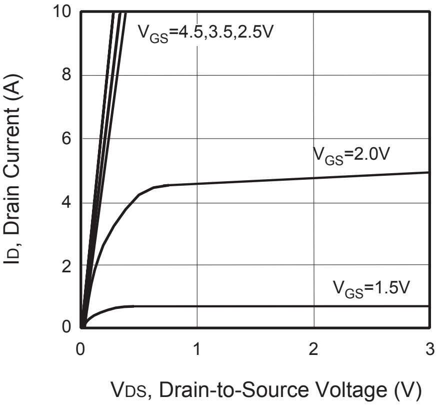


Figure 1. Output Characteristics

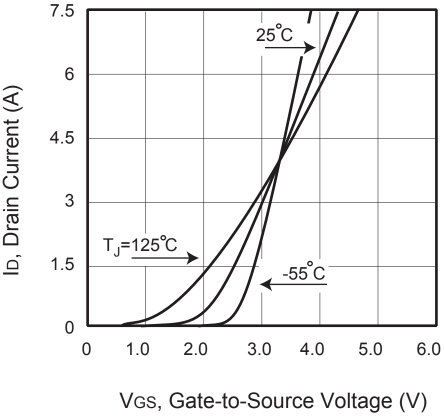


Figure 2. Transfer Characteristics

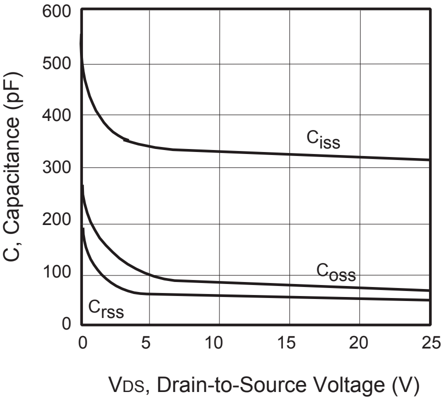


Figure 3. Capacitance

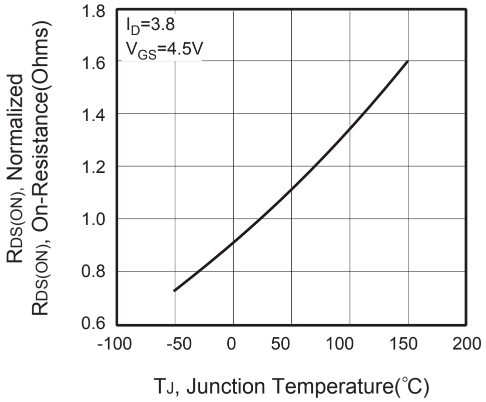


Figure 4. On-Resistance Variation with Temperature

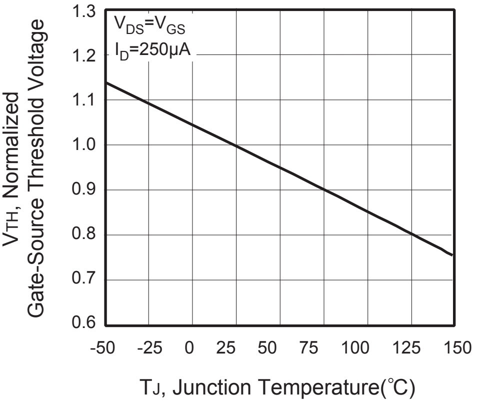


Figure 5. Gate Threshold Variation with Temperature

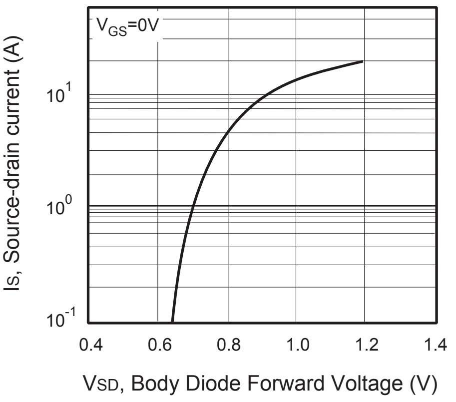


Figure 6. Body Diode Forward Voltage Variation with Source Current

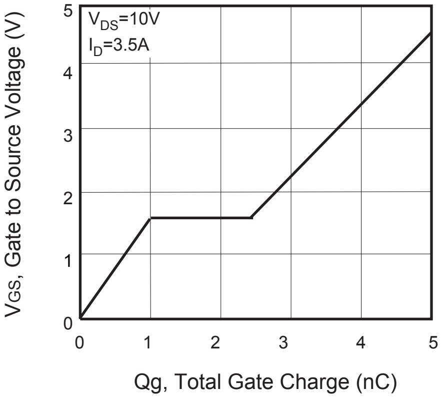


Figure 7. Gate Charge

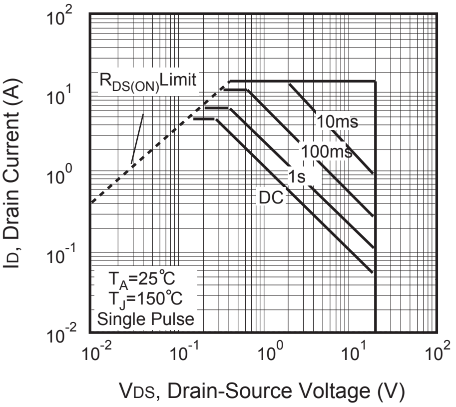


Figure 8. Maximum Safe Operating Area

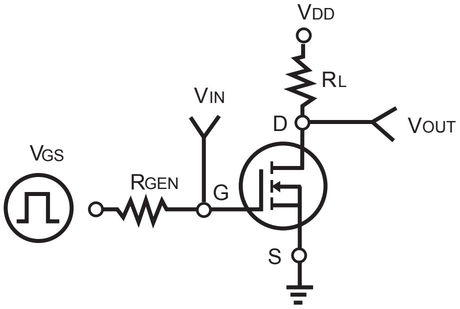


Figure 9. Switching Test Circuit

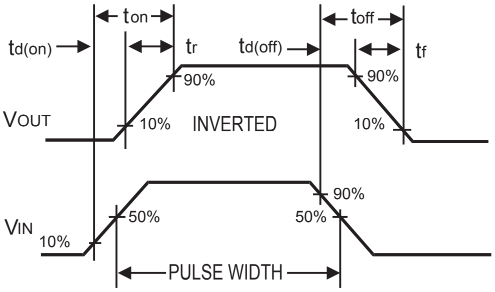
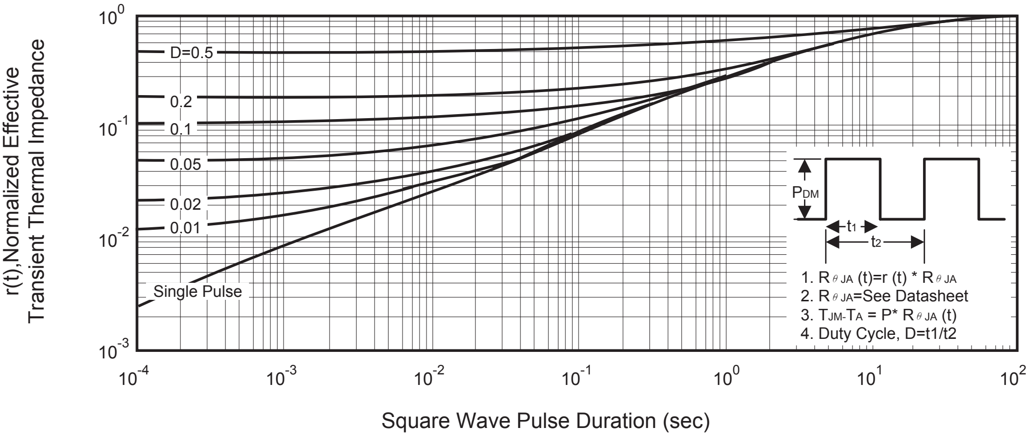


Figure 10. Switching Waveforms



1. $R_{\theta JA}(t) = r(t) * R_{\theta JA}$
2. $R_{\theta JA}$=See Datasheet
3. $T_{JM}-T_A = P^* R_{\theta JA}(t)$
4. Duty Cycle, D=t1/t2

Figure 11. Normalized Thermal Transient Impedance Curve