



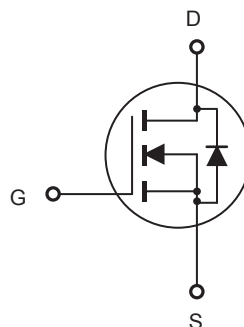
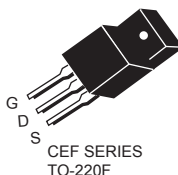
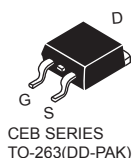
CEP1710/CEB1710 CEF1710

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP1710	100V	85mΩ	19A	10V
CEB1710	100V	85mΩ	19A	10V
CEF1710	100V	85mΩ	19A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- Lead free product is acquired.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	100		V
Gate-Source Voltage	V _{GS}	±20		V
Drain Current-Continuous	I _D	19	19 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	76	76 ^d	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P _D	62.5	32	W
		0.5	0.26	W/°C
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	2	3.9	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W



CEP1710/CEB1710

CEF1710

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 15A$		65	85	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 2.5V, I_D = 15A$		9		S
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		702		pF
Output Capacitance	C_{oss}			200		pF
Reverse Transfer Capacitance	C_{rss}			88		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 19A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$		17	34	ns
Turn-On Rise Time	t_r			51	100	ns
Turn-Off Delay Time	$t_{d(off)}$			16	32	ns
Turn-Off Fall Time	t_f			71	140	ns
Total Gate Charge	Q_g	$V_{DS} = 80V, I_D = 19A,$ $V_{GS} = 10V$		26	34	nC
Gate-Source Charge	Q_{gs}			3.3		nC
Gate-Drain Charge	Q_{gd}			16.2		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				19	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 15A^g$			1.5	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. c.Guaranteed by design, not subject to production testing. d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 13A$. g.Full package V_{SD} test condition $I_S = 13A$.						

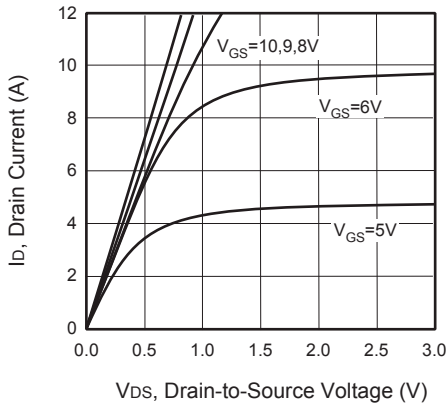


Figure 1. Output Characteristics

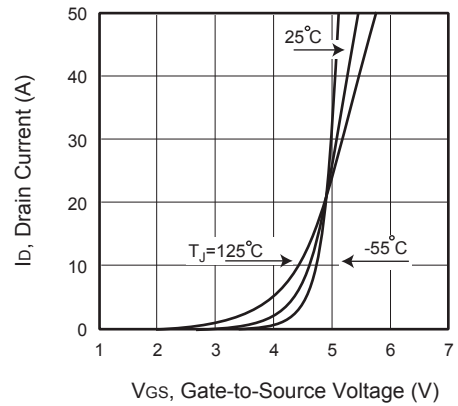


Figure 2. Transfer Characteristics

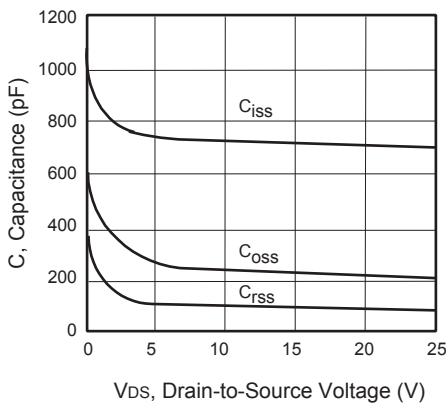


Figure 3. Capacitance

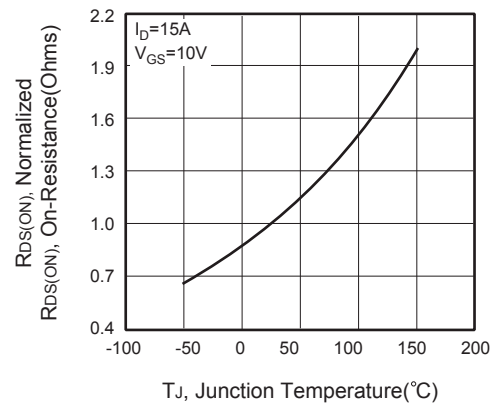


Figure 4. On-Resistance Variation with Temperature

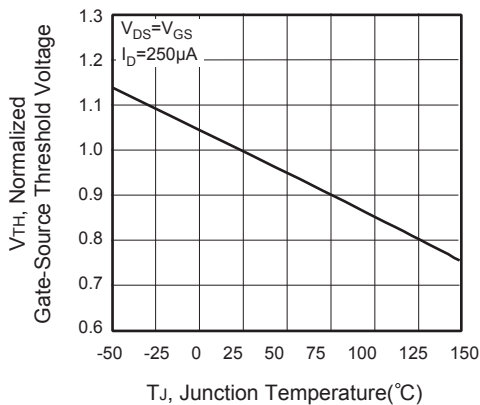


Figure 5. Gate Threshold Variation with Temperature

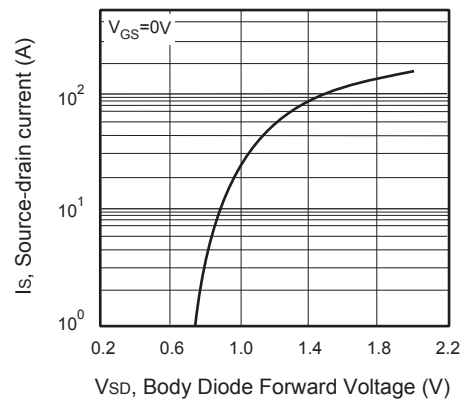
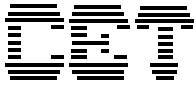


Figure 6. Body Diode Forward Voltage Variation with Source Current



CEP1710/CEB1710 CEF1710

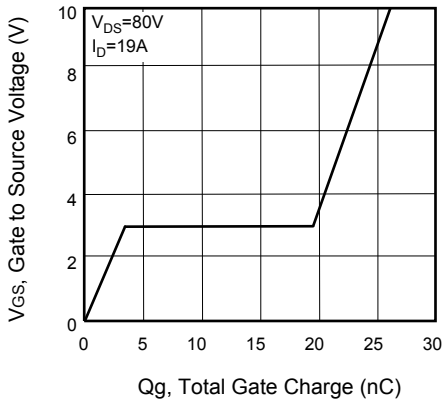


Figure 7. Gate Charge

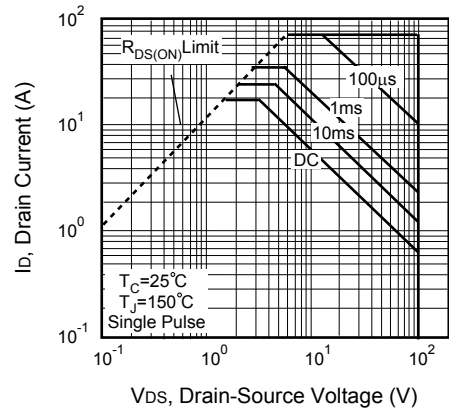


Figure 8. Maximum Safe Operating Area

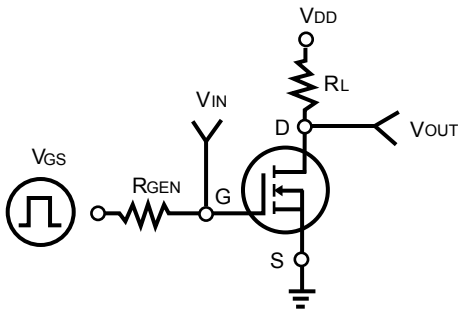


Figure 9. Switching Test Circuit

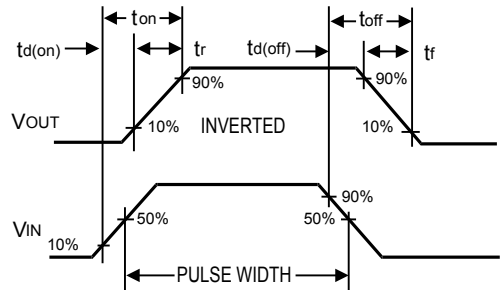


Figure 10. Switching Waveforms

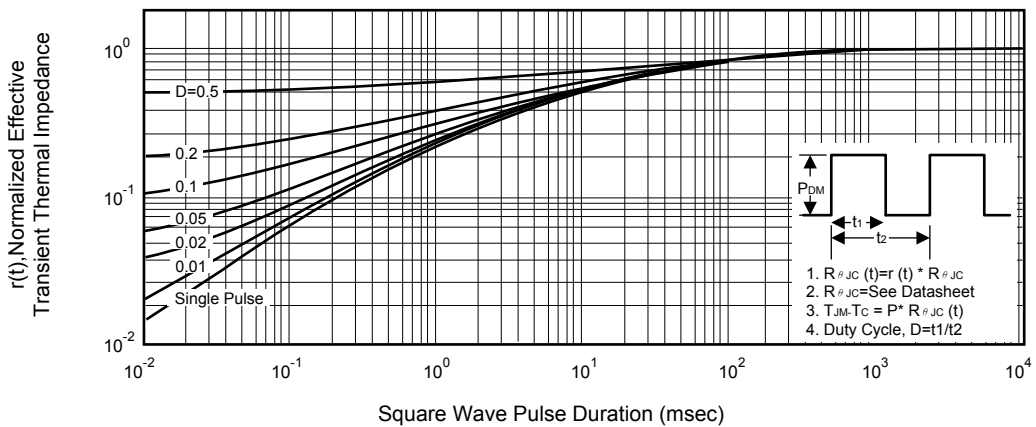


Figure 11. Normalized Thermal Transient Impedance Curve