



CED6086L/CEU6086L

N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

■ 60V, 50.5A, $R_{DS(ON)} = 10m\Omega$ @ $V_{GS} = 10V$.

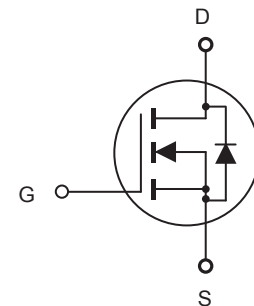
$R_{DS(ON)} = 13.5m\Omega$ @ $V_{GS} = 4.5V$.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handling capability.

■ Lead free product is acquired.

■ TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	I_D	50.5	A
		36	A
Drain Current-Pulsed ^a	I_{DM}	202	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	65	W
		0.43	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^e	E_{AS}	132	mJ
Single Pulsed Avalanche Current ^e	I_{AS}	23	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.3	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$		8	10	m Ω
On-Resistance		$V_{GS} = 4.5V, I_D = 15A$		10	13.5	m Ω
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		2815		pF
Output Capacitance	C_{oss}			235		pF
Reverse Transfer Capacitance	C_{rss}			165		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30V, I_D = 20A,$ $V_{GS} = 10V, R_{GEN} = 4.7\Omega$		19	38	ns
Turn-On Rise Time	t_r			10	20	ns
Turn-Off Delay Time	$t_{d(off)}$			75	150	ns
Turn-Off Fall Time	t_f			12	24	ns
Total Gate Charge	Q_g	$V_{DS} = 48V, I_D = 20A,$ $V_{GS} = 4.5V$		32	42	nC
Gate-Source Charge	Q_{gs}			7		nC
Gate-Drain Charge	Q_{gd}			18		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current ^b	I_S				50.5	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 20A$			1.2	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec.}$ c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing. e.L = 0.5mH, $I_{AS} = 23A, V_{DD} = 24V, R_G = 25\Omega$, Starting $T_J = 25\text{ C}$						

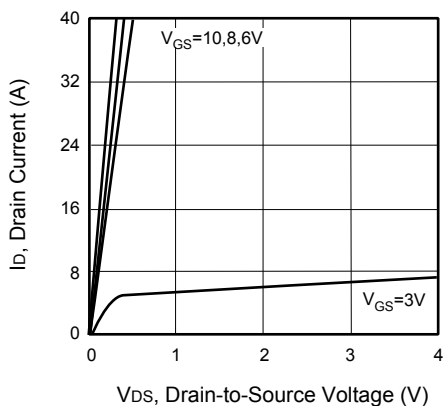


Figure 1. Output Characteristics

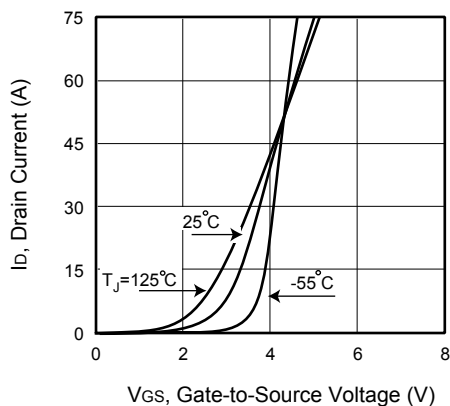


Figure 2. Transfer Characteristics

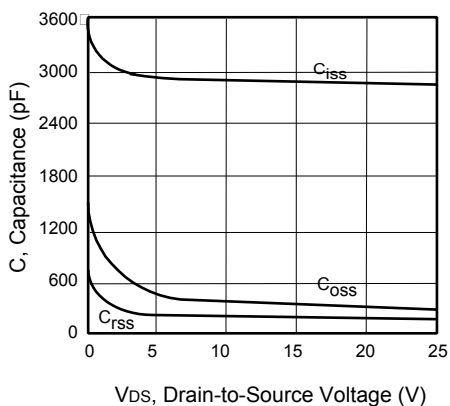


Figure 3. Capacitance

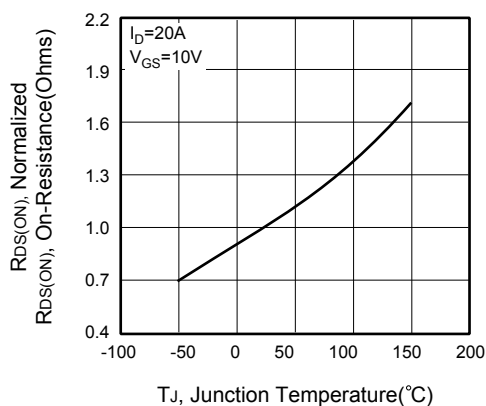


Figure 4. On-Resistance Variation with Temperature

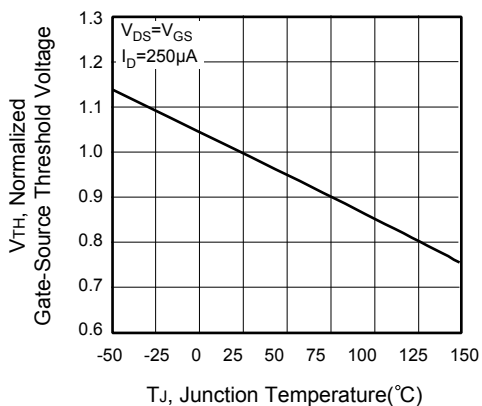


Figure 5. Gate Threshold Variation with Temperature

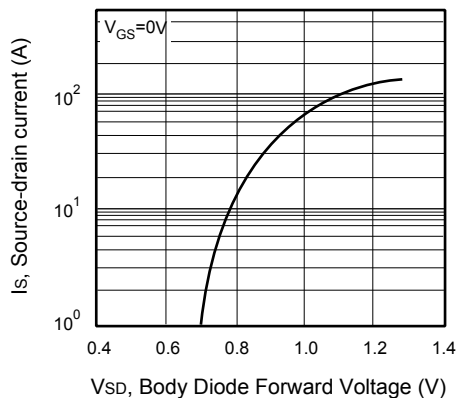


Figure 6. Body Diode Forward Voltage Variation with Source Current



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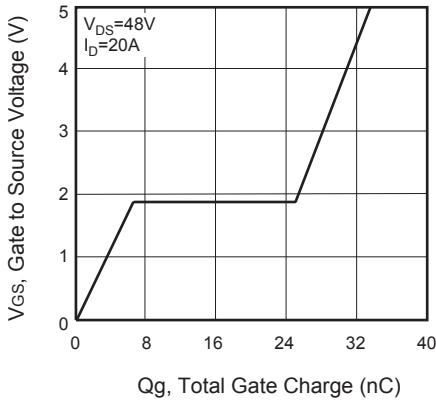


Figure 7. Gate Charge

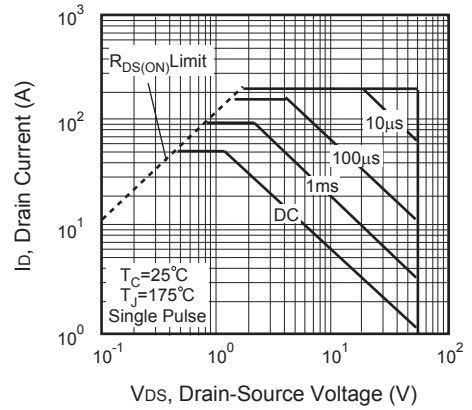


Figure 8. Maximum Safe Operating Area

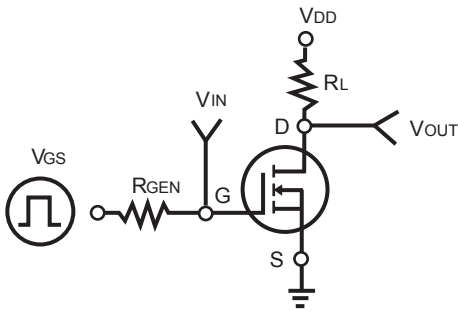


Figure 9. Switching Test Circuit

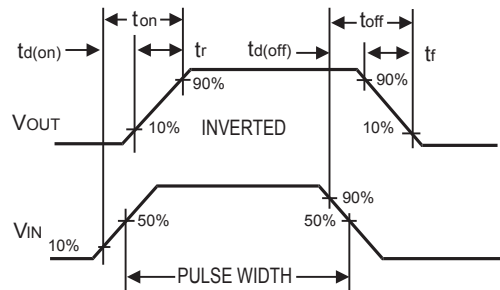


Figure 10. Switching Waveforms

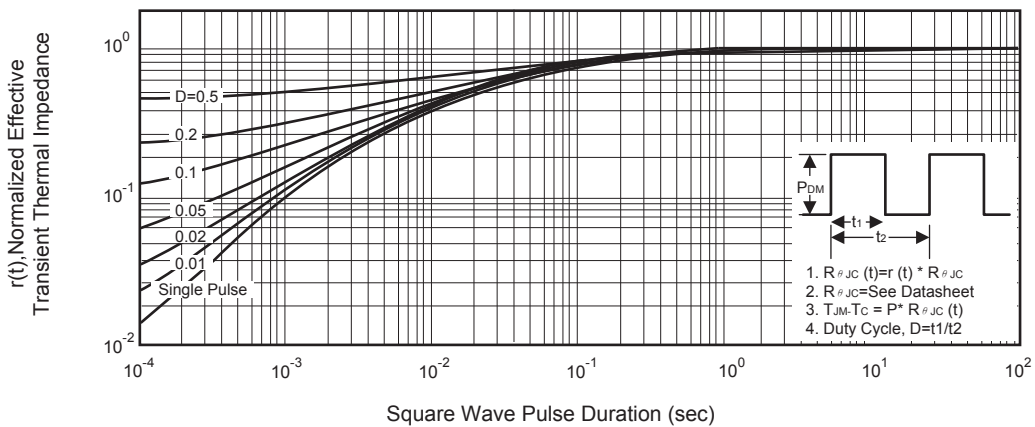


Figure 11. Normalized Thermal Transient Impedance Curve