



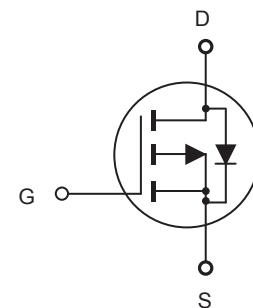
CED12P15/CEU12P15

P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- -150V, -12A, $R_{DS(ON)} = 0.24\Omega$ @ $V_{GS} = -10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage(Typ)	V_{DS}	-150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-12	A
Drain Current-Pulsed ^a	I_{DM}	-48	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	60 0.48	W W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy ^e	E_{AS}	250	mJ
Single Pulsed Avalanche Current ^e	I_{AS}	10	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

This is preliminary information on a new product in development now .
Details are subject to change without notice

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<http://www.cetsemi.com>



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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$		-150		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -135V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-2		-4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -7.5A$		0.2	0.24	Ω
Gate input resistance	R_g	f=1MHz,open Drain		5.3		Ω
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = -25V, V_{GS} = 0V,$ f = 1.0 MHz		1245		pF
Output Capacitance	C_{oss}			175		pF
Reverse Transfer Capacitance	C_{rss}			35		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -75V, I_D = -7.5A,$ $V_{GS} = -10V, R_{GEN} = 10\Omega$		18		ns
Turn-On Rise Time	t_r			8		ns
Turn-Off Delay Time	$t_{d(off)}$			63		ns
Turn-Off Fall Time	t_f			14		ns
Total Gate Charge	Q_g	$V_{DS} = -120V, I_D = -7.5A,$ $V_{GS} = -10V$		31		nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			12		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current ^b	I_S				-12	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -12A$			-1.2	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, t ≤ 10 sec. c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%. d.Guaranteed by design, not subject to production testing. e.L = 5mH, I _{AS} = 10A, V _{DD} = 25V, R _G = 25Ω, Starting T _J = 25 C						

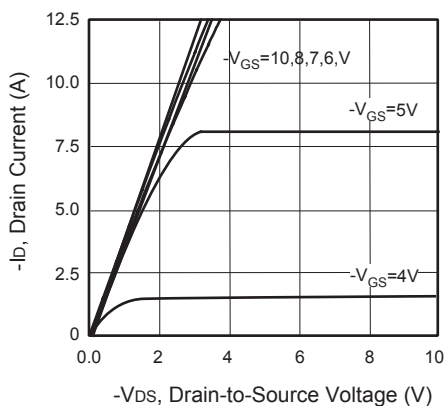


Figure 1. Output Characteristics

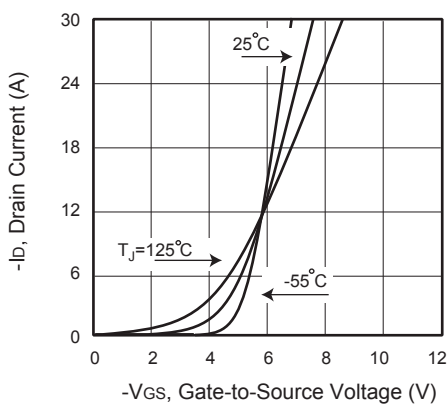


Figure 2. Transfer Characteristics

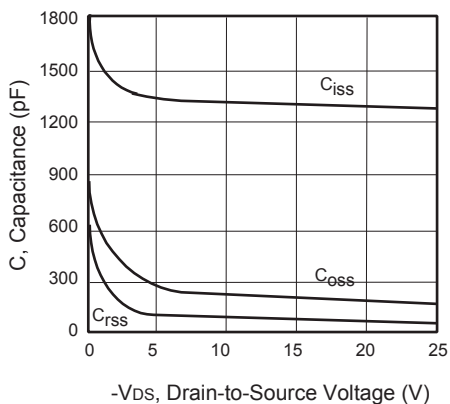


Figure 3. Capacitance

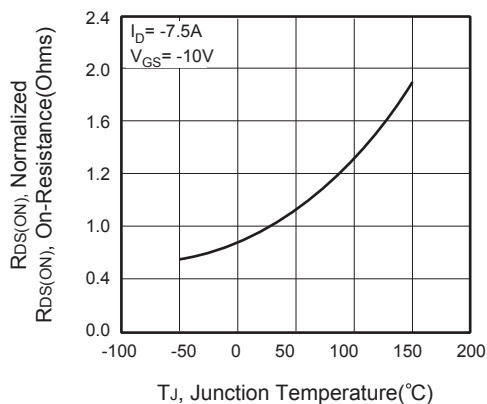


Figure 4. On-Resistance Variation with Temperature

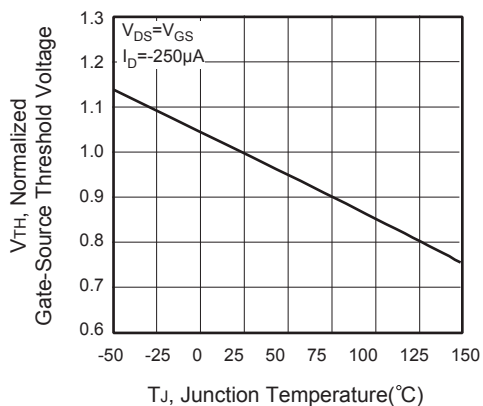


Figure 5. Gate Threshold Variation with Temperature

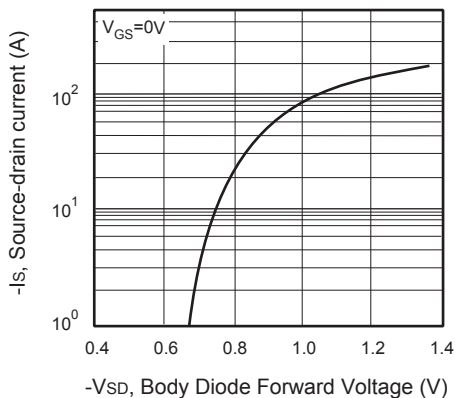


Figure 6. Body Diode Forward Voltage Variation with Source Current



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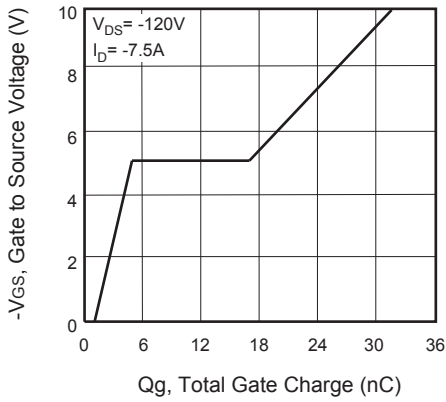


Figure 7. Gate Charge

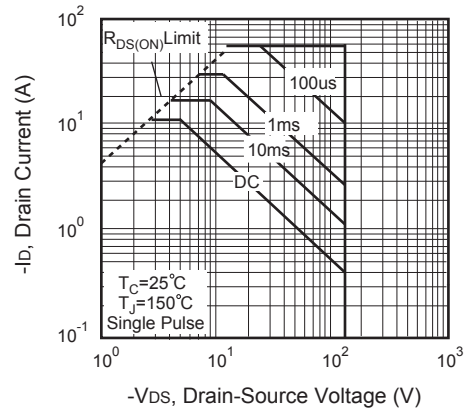


Figure 8. Maximum Safe Operating Area

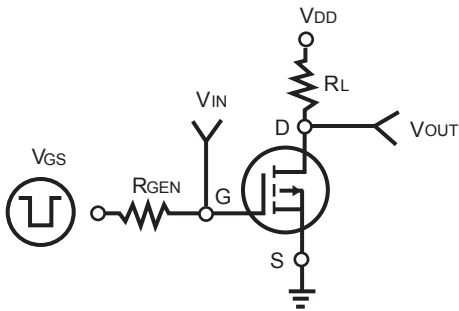


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

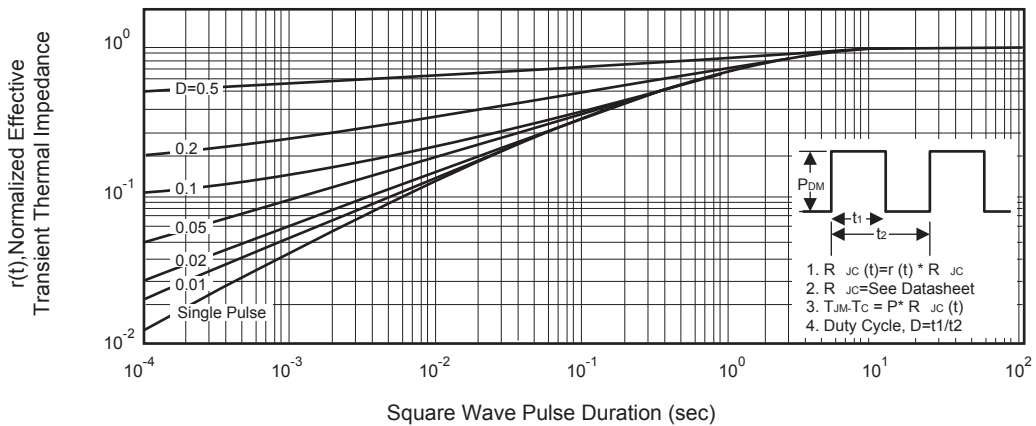


Figure 11. Normalized Thermal Transient Impedance Curve