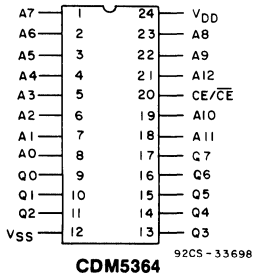
CDM5364, CDM5364A



CDM5364
TERMINAL ASSIGNMENT

CMOS 8192-Word by 8-Bit LSI Static ROMS

Features:

- *Asynchronous operation*
- *Fast access time - 250 ns max.*
- *Low standby and operating power:*
  I_{SBY2} = 2 μA typical (CDM5364)
  I_{DDS} = 2 μA typical (CDM5364A)
  I_{OPER2} = 10 mA max. at t_{cyc} = 1 μs
  = 30 mA max. at t_{cyc} = 250 ns
- *Automatic power down*
- *TTL input and output compatible*
- *24-pin JEDEC standard pin out: Pin compatible with Motorola MCM68764 and MCM68766 EPROMs*
- *Choice of pin 20 function: Mask-programmable CE (CDM5364) Mask-programmable CS (CDM5364A)*

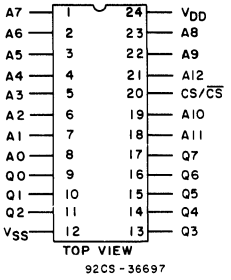
The RCA CDM5364 and CDM5364A are 65,536-bit mask-programmable CMOS Read Only Memories organized as 8192 eight-bit words. They are characterized by fast access time and low-power dissipation, and are designed to be used with a wide variety of general purpose microprocessor systems, including RCA-CDP1800-and CDP6805-series systems. The CDM5364 and CDM5364A differ in the function for pin 20.

The CDM5364 provides a chip enable input at pin 20, which gates the address buffers and output drivers, providing a low power standby mode.

The CDM5364A has a chip select input at pin 20. As a chip select input, pin 20 controls only the output drivers providing fast output enable time. The polarities of the chip enable and the chip select inputs are user mask-programmable.

Both the CDM5364 and CDM5364A provide automatic power-down and data hold while the address inputs are stable.

The CDM5364 and CDM5364A are supplied in 24-lead hermetic, dual-in-line side-brazed ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).



CDM5364A
TERMINAL ASSIGNMENT

6

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 8 mW/°C to 300 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C

File Number **1467**

CDM5364, CDM5364A

RECOMMENDED OPERATING CONDITIONS at T_A = -40 to +85°C
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS CDM5364, CDM5364A		UNITS
	Min.	Max.	
DC Operating Voltage Range	4	6	V
Input Voltage Range	V_{SS}	V_{DD}	

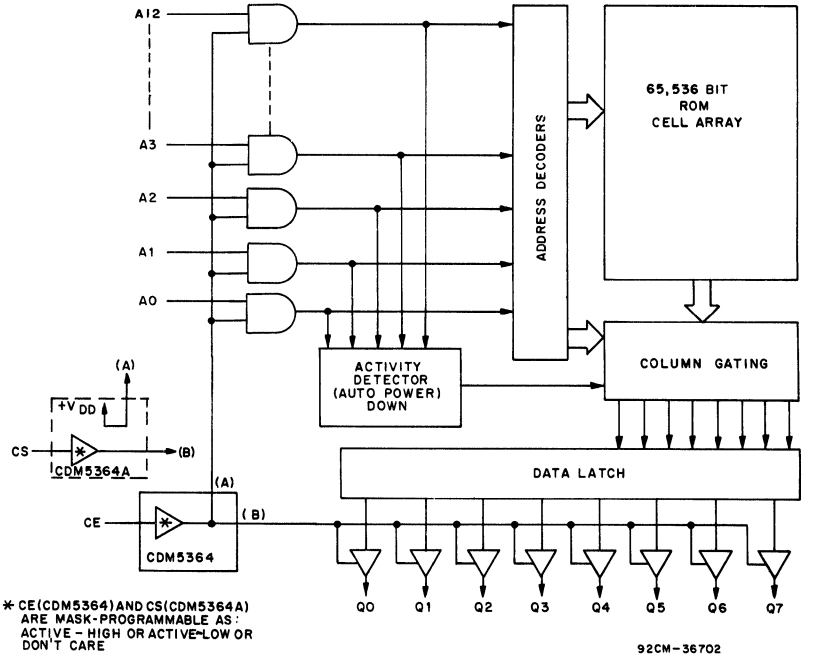


Fig. 1 - Functional block diagram.

CDM5364, CDM5364A

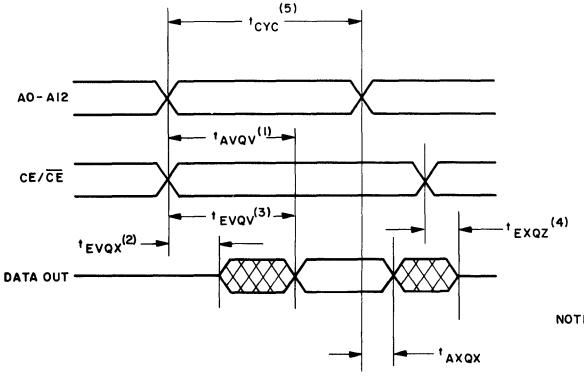
STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS CDM5364 Min.	Typ.•	Max.	UNITS
Average Operating Device Current[a]		V_{IN} = V_{IL}, V_{IH}, CE = V_{IH}, ($\overline{CE}$ = V_{IL})				
		t_{cyc} = 1 µs	—	—	15	mA
	I_{OPER1}[d]	t_{cyc} = 250 ns	—	—	35	
	I_{OPER2}[e]	V_{IN} = 0 2 V, V_{DD} -0 2 V, CE = V_{DD} -0 2 V,				
		($\overline{CE}$ = 0.2 V) t_{cyc} = 1 µs	—	—	10	
		t_{cyc} = 250 ns	—	—	30	
DC Active Device Current[b]	I_{ACT1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IH}, ($\overline{CE}$ = V_{IL})	—	—	15	mA
	I_{ACT2}[e]	V_{IN} = 0 2 V, V_{DD} -0 2 V, CE = V_{DD} -0 2 V, ($\overline{CE}$ = 0 2 V)	—	—	50	µA
Standby Device Current[c]	I_{SBY1}[d]	V_{IN} = V_{IL}, V_{IH}, CE = V_{IL}, ($\overline{CE}$ = V_{IH})	—	—	1 5	mA
	I_{SBY2}[e]	V_{IN} = 0 2 V, V_{DD} -0.2V, CE = 0 2 V, ($\overline{CE}$ = V_{DD} -0 2 V)	—	2	50	µA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3 2 mA	—	—	0 4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3 2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0 8	
Input High Voltage	V_{IH}	—	2 2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25°C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25°C	—	6	12	

•Typical values are for T_A = 25° C and nominal V_{DD}
[a]Address inputs toggling, chip enabled outputs open circuit.
[b]Inputs stable, chip enabled, outputs open circuit
[c]Independent of address input activity, chip disabled
[d]TTL inputs
[e]CMOS inputs

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V — See Fig. 2

CHARACTERISTIC		LIMITS CDM5364 Min.	Max.	UNITS
Address Access Time	t_{AVQV}	—	250	ns
Chip Enable to Output Active	t_{EVQX}	0	—	
Chip Enable Access	t_{EVQV}	—	250	
Data Hold after Address	t_{AXQX}	10	—	
Chip Disable to Output High Z	t_{EXQZ}	—	90	
Cycle Time	t_{CYC}	250	—	



NOTES:
(1) Assumes t_{EVQV} is satisfied.
(2) Output Active requires Chip Enable Active.
(3) Assumes t_{AVQV} is satisfied.
(4) Invalid Chip Enable causes Output High Z.
(5) Generates 10-ns Valid Output Pulses (I.e., t_{CYC}-t_{AVQV}+t_{AXQX}).

NOTE TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V

92CM-36699

Fig. 2 - Timing waveforms

CDM5364, CDM5364A

STATIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS	LIMITS CDM5364A Min.	Typ.•	Max.	UNITS
Average Operating Device Current[a]		V_{IN} = V_{IL}, V_{IH}; CS = V_{IH}; ($\overline{CS}$ = V_{IL})				
		t_{cyc} = 1 µs	—	—	15	mA
	I_{OPER1}[d]	t_{cyc} = 250 ns	—	—	35	
	I_{OPER2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CS = V_{DD} -0.2 V; ($\overline{CS}$ = 0.2 V)				
		t_{cyc} = 1 µs	—	—	10	
		t_{cyc} = 250 ns	—	—	30	
DC Active Device Current[b]	I_{ACT1}[d]	V_{IN} = V_{IL}, V_{IH}; CS = V_{IH}; ($\overline{CS}$ = V_{IL})	—	—	15	mA
	I_{ACT2}[e]	V_{IN} = 0.2 V, V_{DD} -0.2 V; CS = V_{DD} -0.2 V; ($\overline{CS}$ = 0.2 V)	—	—	50	µA
Quiescent Device Current[c]	I_{DDS}[e]	V_{IN} = 0.2 V, V_{DD} -0.2V; CS = 0.2 V; ($\overline{CS}$ = V_{DD} -0 2 V)	—	2	50	µA
Output Voltage Low-Level	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Output Voltage High-Level	V_{OH}	I_{OH} = -3 2 mA	2.4	—	—	
Input Low Voltage	V_{IL}	—	—	—	0.8	
Input High Voltage	V_{IH}	—	2.2	—	—	
Input Leakage Current (Any Input)	I_{IN}	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	±1	µA
3-State Output Leakage Current	I_{OUT}	$V_{SS} \leq V_{OUT} \leq V_{DD}$	—	—	±1	
Input Capacitance	C_{IN}	f = 1 MHz, T_A = 25°C	—	5	10	pF
Output Capacitance	C_{OUT}	f = 1 MHz, T_A = 25°C	—	6	12	

•Typical values are for T_A = 25° C and nominal V_{DD}.
[a] Address inputs toggling, chip selected outputs open circuit.
[b] Inputs stable, chip selected outputs open circuit
[c] Inputs stable, chip deselected.
[d] TTL inputs.
[e] CMOS inputs.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85° C, V_{DD} = 5 V ± 10%, Input t_r, t_f = 10 ns; C_L = 100 pF, and 1 TTL Load; Input Pulse Levels: 0.8 V to 2.2 V — See Fig. 3

CHARACTERISTIC		LIMITS CDM5364A Min.	Max.	UNITS
Address Access Time	t_{AVQV}	—	250	ns
Chip Select to Output Active	t_{SVQX}	0	—	
Chip Select to Output Valid	t_{SVQV}	—	90	
Data Hold after Address	t_{AXQX}	10	—	
Chip Deselect to Output High Z	t_{SXQZ}	—	70	
Cycle Time	t_{CYC}	250	—	

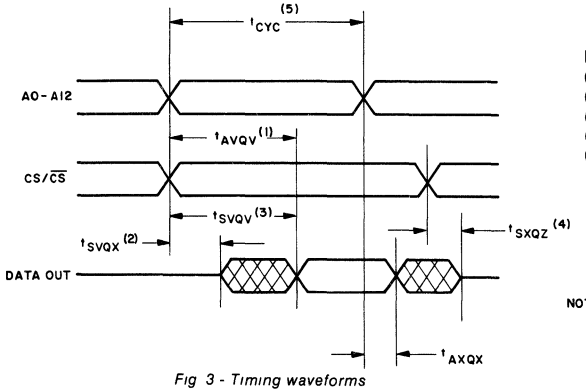


Fig 3 - Timing waveforms

NOTES:
(1) Assumes t_{SVQV} is satisfied.
(2) Output Active requires Chip Select Active.
(3) Assumes t_{AVQV} is satisfied.
(4) Invalid Chip Select causes Output High Z.
(5) Generates 10-ns Valid Output Pulses (i.e., t_{CYC}-t_{AVQV}+t_{AXQX}).

NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V

92CM-36700

APPLICATION INFORMATION

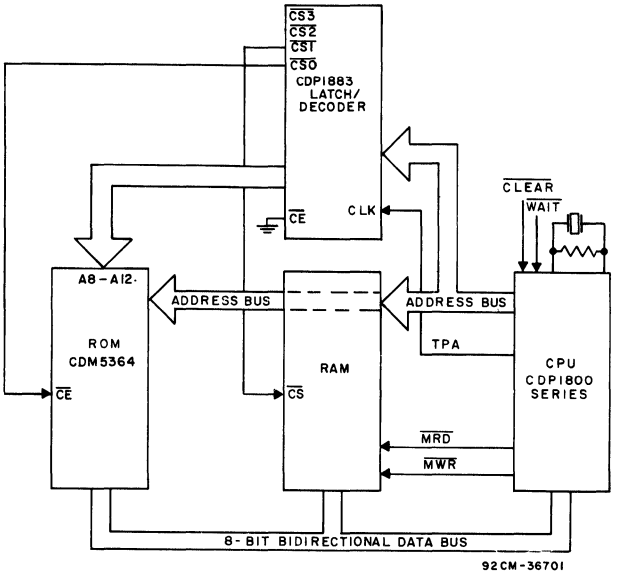


Fig. 4 - Typical CDP1800 series microprocessor system.

Decoupling Capacitors

The CDM5364 and CDM5364A operate with a low average dc power supply current that varies with cycle time. However, the CDM5364 and CDM5364A are large ROMs with many internal nodes. Precharging of selected nodes during portions of the memory cycle results in short duration peak currents that can be much higher than the average dc value. The rise and fall times of the peak current pulses can have a value sufficient to generate unwanted system noise components. To minimize or eliminate the effects of the current spikes, a 0.1 μF ceramic decoupling capacitor is recommended between the V_{DD} and V_{SS} pins of every ROM device.