

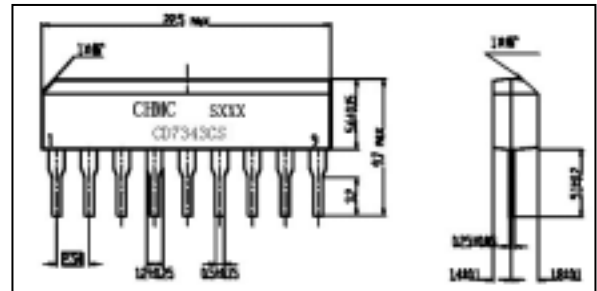


## FM STEREO MULTIPLEX DECODER CD7343CS

### ● GENERAL DESCRIPTION

The CD7343CS is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It is designed for car stereo, cassette recorder and other equipment.

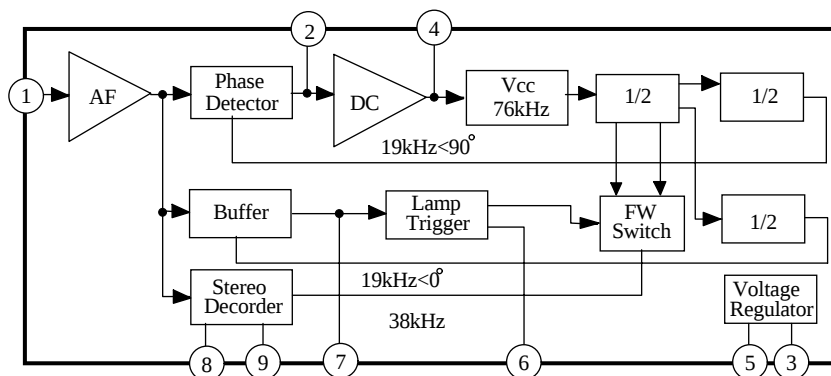
Outline Drawing



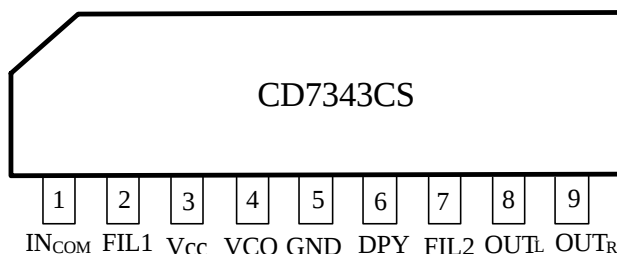
### FEATURES

- Wide operating supply voltage:  $V_{CC}=3.5V\sim 12V$
- High pilot lamp ON sensitivity ( $V_{L(ON)}=9mV$ )
- Built-in indicator lamp drive circuit
- Low distortion THD=0.08% at  $V_i=200mV$

### BLOCK DIAGRAM



### PIN CONNECTION



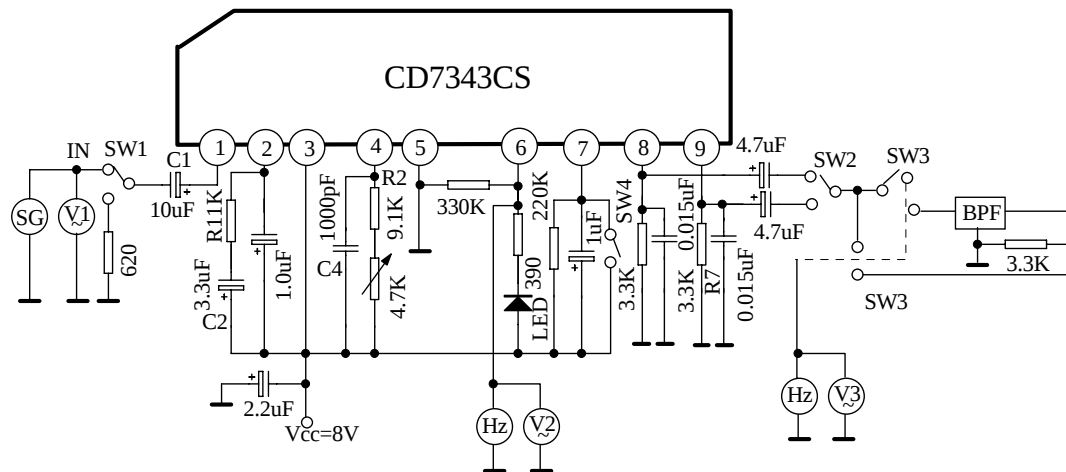
**MAXIMUM RATINGS**

| Characteristics                     | Symbol            | Value   | Unit |
|-------------------------------------|-------------------|---------|------|
| Supply Voltage                      | V <sub>CC</sub>   | 12      | V    |
| Lamp Voltage                        | V <sub>LAMP</sub> | 16      | V    |
| Lamp Current (Continuous)           | I <sub>LAMP</sub> | 20      | mA   |
| Power Dissipation                   | P <sub>D</sub>    | 500     | mW   |
| Operating Ambient Temperature Range | T <sub>opr</sub>  | -25~75  | °C   |
| Storage Temperature Range           | T <sub>stg</sub>  | -55~150 | °C   |

**ELECTRICAL CHARACTERISTICS**(Unless otherwise specified V<sub>CC</sub>=8V, T<sub>amb</sub>=25°C, f=1kHz)

| Characteristic                     | Symbol              | Test Condition         |       | Min. | Typ. | Max. | Unit |
|------------------------------------|---------------------|------------------------|-------|------|------|------|------|
| Quiescent Circuit Current          | ICCQ                | Vi=0                   |       |      | 11   | 18   | mA   |
| Maximum Input Voltage              | Vi(max)             | L+R=90%, P=10%, THD=1% |       |      | 900  |      | mV   |
| Channel Separation                 | Sep                 | L+R=180mV, Vp=20mV     |       | 36   | 45   |      | dB   |
| Total Harmonic Distortion (mono)   | THD1                | Vi=200mV               |       |      | 0.08 | 0.3  | %    |
| Total Harmonic Distortion (stereo) | THD2                | L+R=180mV, Vp=20mV     |       |      | 0.08 |      | %    |
| Voltage Gain                       | Av                  | Vi=200mV               |       | -2.0 | 0    | 2.0  | dB   |
| Channel Balance                    | CB                  | Vi=200mV               |       |      | 0    | 1.5  | dB   |
| Lamp ON level                      | V <sub>L(ON)</sub>  | Pilot only             |       |      | 9    | 15   | mV   |
| Lamp OFF level                     | V <sub>L(OFF)</sub> | Pilot only             |       | 2    | 6    |      | mV   |
| Lamp Hysteresis                    | V <sub>HY</sub>     |                        |       |      | 3    |      | mV   |
| Carrier Leakage                    | CL                  | L+R=180mV<br>Vp=20mV   | 19kHz |      | 34   |      | dB   |
|                                    |                     |                        | 38kHz |      | 42   |      | dB   |

## TEST CIRCUIT



BPF: 19kHz ≤ 55dB 38kHz ≤ 55dB L.P.F

## APPLICATION INFORMATION (refer to test circuit)

### External Components

#### 1. Input coupling capacitor (C1)

The recommended value is 10µF. If smaller values than 10µF are used, low frequency separation will worsens, and if large values are used ,POP noise occurs strongly.

#### 2. Low Pass Filter (C2, C1, R1)

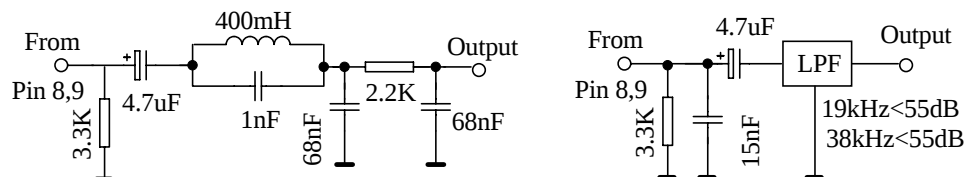
This is the low Pass filter for the PLL, which is determined the capture range and THD at low frequency.

#### 3. VCO network (C4, R2, R7)

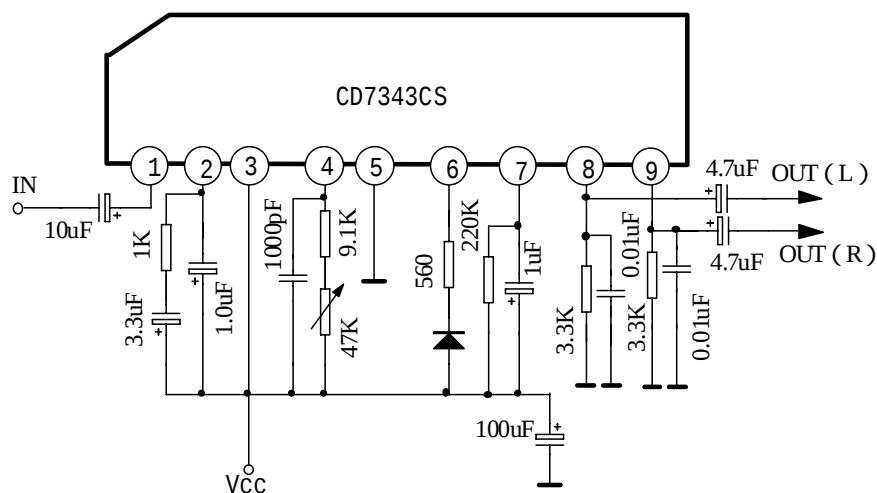
The VCO free running frequency is adjusted by connecting a frequency counter to monitor the 38kHz output of Pin6 .

#### 4. Decoder Output (Pin8,9)

These components provide Right and Left channel Output load circuits . The recommended circuits as follows:



### APPLICATION CIRCUIT



### CHARACTERISTICS CURVES

