CMOS 32-Stage Static Left/Right Shift Register

The RCA-CD40100B is a 32-stage shift register containing 32 D-type master-slave flip-flops.

The data present at the SHIFT-RIGHT INPUT is transferred into the first register stage synchronously with the positive CLOCK edge, provided the LEFT/RIGHT CONTROL is at a low level, the RECIRCULATE CONTROL is at a high level, and the CLOCK INHIBIT is low. If the LEFT/RIGHT CONTROL is at a high level and the RECIRCULATE CONTROL is also high, data at the SHIFT-LEFT INPUT is transferred into the 32nd register stage synchronously with the positive CLOCK transition, provided the CLOCK INHIBIT is low. The state of the LEFT/RIGHT CONTROL, RECIRCULATE CONTROL, and CLOCK INHIBIT should not be changed when the CLOCK is high.

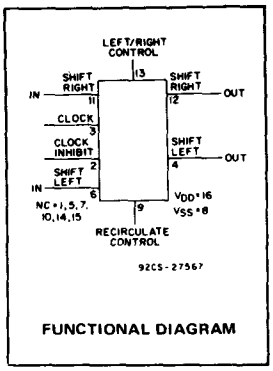
Data is shifted one stage left or one stage right depending on the state of the LEFT/RIGHT CONTROL, synchronously with the positive CLOCK edge. Data clocked into the first or 32nd register states is available at the SHIFT-LEFT or SHIFT-RIGHT OUTPUT respectively, on the next negative CLOCK transition (see Data Transfer Table). No shifting occurs on the positive CLOCK edge if the CLOCK INHIBIT line is at a high level. With the RECIRCULATE CONTROL low, data in the 32nd stage is shifted into the first stage when the LEFT/RIGHT CONTROL is low and from the 1st stage to the 32nd stage when the LEFT/RIGHT CONTROL is high.

The CD40100B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

High-Voltage Types (20-Volt Rating)

Features:

- **Fully static operation**
- ***Shift left/Shift right capability***
- **Multiple package cascading**
- **Recirculate capability**
- ***LIFO or FIFO capability***
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) =**
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Serial shift registers**
- **Time delay circuits**
- **Expandable N-bit data storage stack (LIFO operation)**

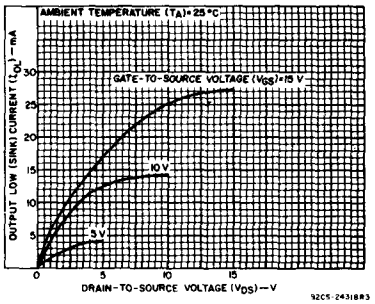


Fig. 1 – Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

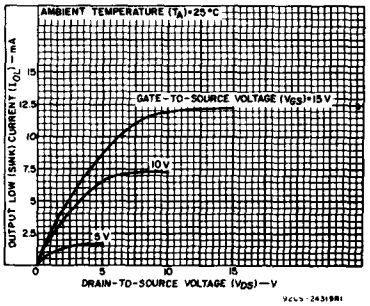


Fig. 2 – Minimum output low (sink) current characteristics.

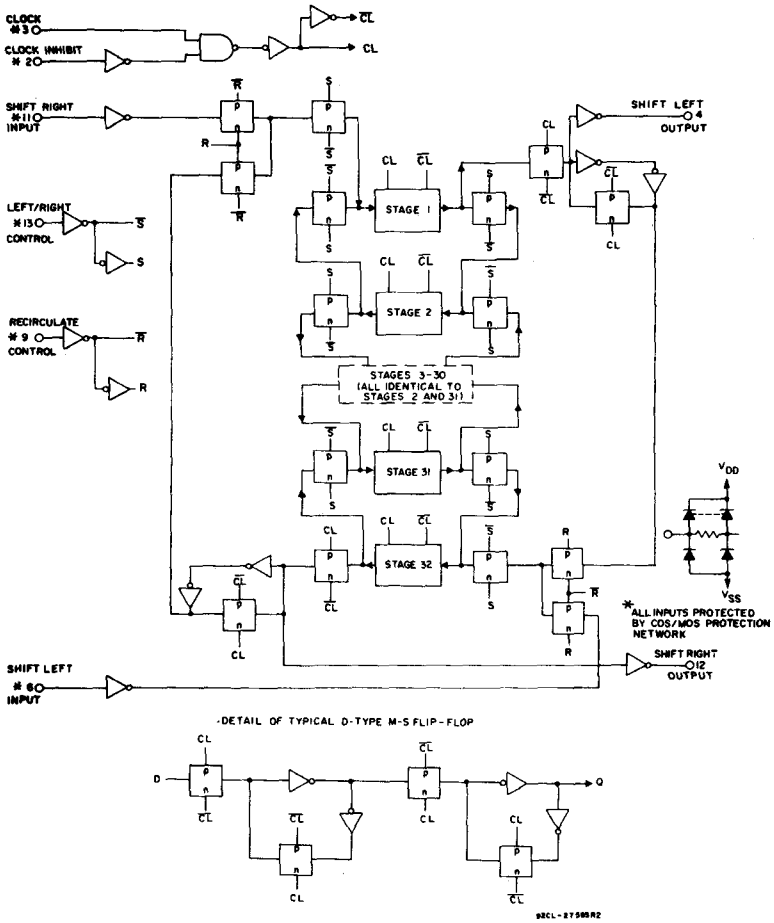


Fig. 3 – Logic diagram.

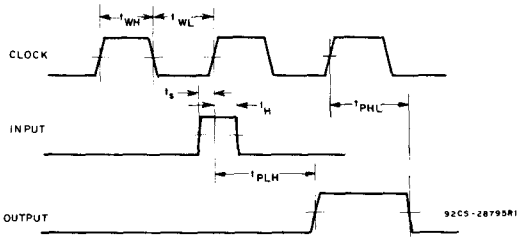


Fig. 4 – Timing diagram defining setup, hold, and propagation delay times.

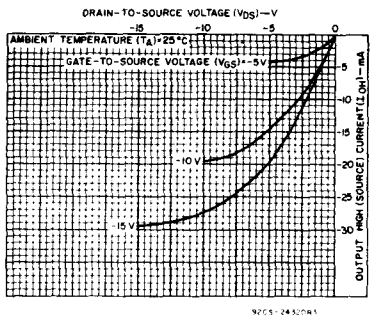


Fig. 5 – Typical output high (source) current characteristics.

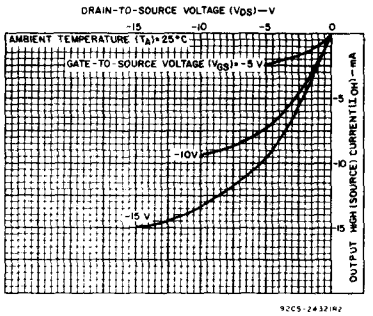


Fig. 6 – Minimum output high (source) current characteristics.

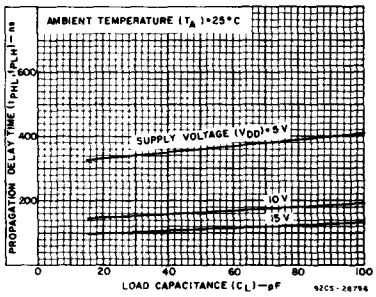


Fig. 7 – Typical propagation delay time (CLOCK to SHIFT LEFT/RIGHT) as a function of load capacitance.

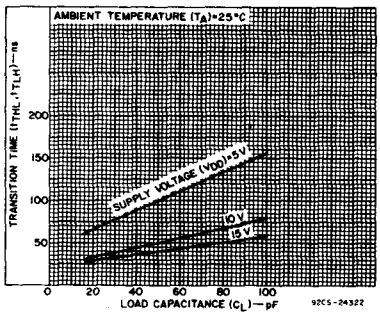


Fig. 8 – Typical transition time as a function of load capacitance.

RECOMMENDED OPERATING CONTITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5	100	–	ns
	10	20	–	
	15	10	–	
Data Hold Time, t_H	5	275	–	ns
	10	100	–	
	15	75	–	
Clock Input Frequency, f_{CL}	5		1	mHz
	10	dc	2.5	
	15		3	
Clock Input Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	
	15	–	15	
Clock Input Pulse Width: Low Level, t_{WL}	5	450	–	ns
	10	230	–	
	15	190	–	
High Level, t_{WH}	5	280	–	ns
	10	150	–	
	15	140	–	

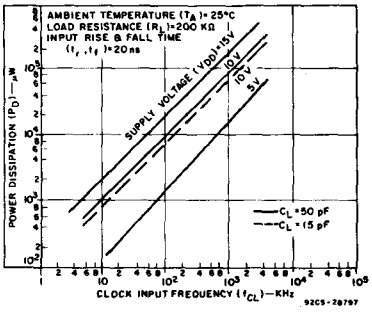


Fig. 9 – Typical dynamic power dissipation as a function of CLOCK frequency.

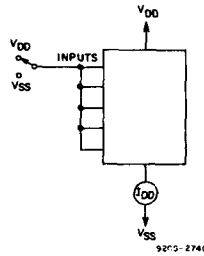


Fig. 10 – Quiescent-device-current test circuit.

CONTROL TRUTH TABLE

LEFT/RIGHT CONTROL	CLOCK INHIBIT	RECIRCULATE CONTROL	ACTION	INPUT BIT ORIGIN
1	0	1	Shift left	Shift left input
1	0	0	Shift left	Stage 1
0	0	1	Shift right	Shift right input
0	0	0	Shift right	Stage 32
X	1	X	No shift	–

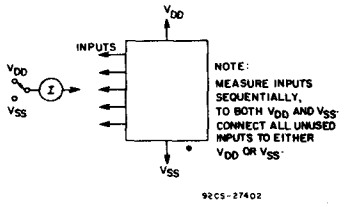


Fig. 11 – Input-current test circuit.

DATA TRANSFER TABLE*

INITIAL STATE			CLOCK	RESULTING STATE	
DATA INPUT	CLOCK INHIBIT	INTERNAL STAGE	LEVEL CHANGE	INTERNAL STAGE Q	OUTPUT
0	0	X	⌒	0	NC
X	0	0	⌒	NC	0
1	0	X	⌒	1	NC
X	0	1	⌒	NC	1
X	1	1	X	NC	NC

0 = Low level 1 = High level X = Don't care NC = No change

* For Shift-Right Mode
Data Input = SHIFT-RIGHT INPUT (Term. 11)
Internal Stage = Stage 1 (Q_1)
Output = SHIFT-LEFT OUTPUT (Term. 4)

For Shift-Left Mode
Data Input = SHIFT-LEFT INPUT (Term. 6)
Internal Stage = Stage 32 (Q_{32})
Output = SHIFT-RIGHT OUTPUT (Term. 12)

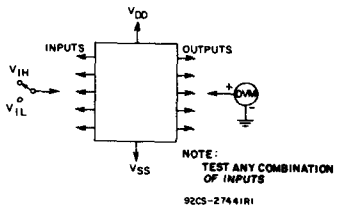
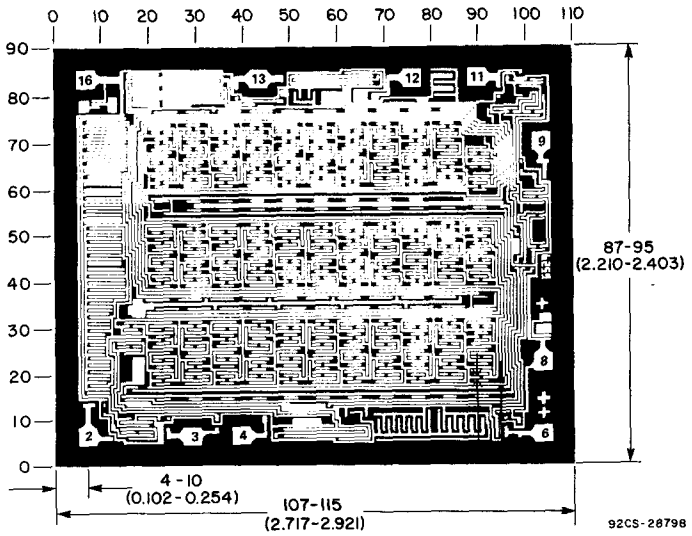


Fig. 12 – Input-voltage test circuit.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	1.5,13.5	–	15	4				–	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	-	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA



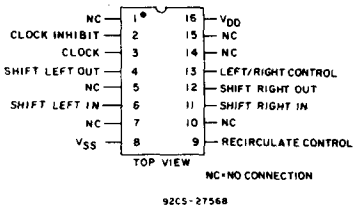
Dimensions and pad layout for CD40100BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Shift Left/Right Output, t_{PLH}, t_{PHL}		5		360	720	ns
		10		165	330	
		15		115	230	
Transition Time, t_{THL}, t_{TLH}		5		100	200	ns
		10		50	100	
		15		40	80	
Minimum Data Setup Time, t_S		5		50	100	ns
		10		10	20	
		15		5	10	
Minimum Data Hold Time, t_H		5		170	275	ns
		10		75	100	
		15		50	75	
Maximum Clock Input Frequency, f_{CL}		5	1	2		MHz
		10	2.5	5		
		15	3	6		
Minimum Clock Input Pulse Width: Low Level, t_{WL}		5		225	450	ns
		10		115	230	
		15		95	190	
High Level, t_{WH}		5		140	280	ns
		10		75	150	
		15		70	140	
Input Capacitance, C_{IN}	Any Input	–		5	7.5	pF



TERMINAL ASSIGNMENT