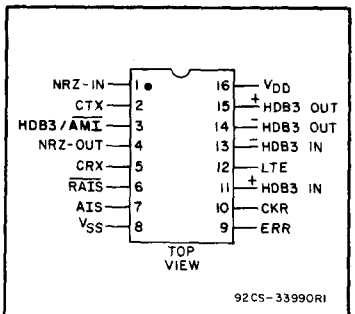
# CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications

**Features:**

- *HDB3 coding and decoding for data rates from 50 Kb/s to 10 Mb/s in a manner consistent with CCITT G703 recommendations.*
- *HDB3/AMI transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections.*
- *All transmitter and receiver inputs/outputs are TTL compatible.*
- *Internal Loop Test capability.*




**Terminal Assignment**

The RCA CD22103 is an LSI SOS integrated circuit which performs the HDB3 transmission coding and reception decoding functions with error detection. It is used in 2.048 and 8.448 Mb/s transmission applications. The CD22103 performs HDB3 coding and decoding for data rates from 50 Kb/s to 10 Mb/s in a manner consistent with CCITT G703 recommendations.

HDB3 transmission coding/reception decoding with code error detection is performed in independent code and decoder sections. All transmitter and receiver inputs/outputs are TTL compatible.

The HDB3 transmitter coder codes are NRZ binary unipolar input signal (NRZ-In) and a synchronous transmission clock (CTX) into two HDB3 binary unipolar RZ output signals (+HDB3 OUT, -HDB3 OUT). The TTL compatible output signals +HDB3 OUT, -HDB3 OUT are externally mixed to generate ternary bipolar HDB3 signals for driving transmission lines.

HDB3 reception decoding is performed on ternary bipolar HBD3 signals which have been externally split to provide binary unipolar receiver input signals, (+HDB3 IN, -HDB3 IN), and a synchronous receiver clock signal, (CRX) into binary unipolar NRZ signals (NRZ - Out).

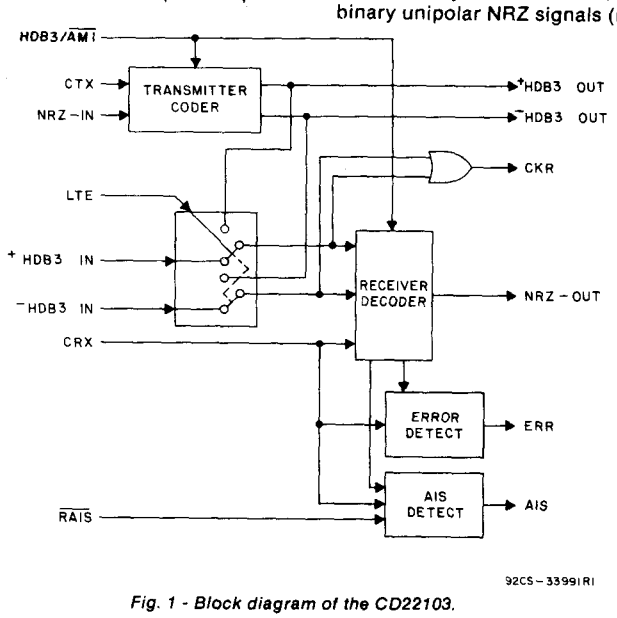



*Fig. 1 - Block diagram of the CD22103.*

Received signals not consistent with HDB3 coding rules are detected as errors. The receiver error output (ERR) is active high during one CRX period of each bit of received data which is inconsistent with HDB3 coding rules.

An input string consisting of all ones (or marks) is detected and signaled by a high level at the Alarm Signal (AIS) output. The AIS output is set to a high level when less than three zeros are received during two consecutive periods of the Reset Alarm Inhibit Signal (RAIS). The AIS output is subsequently reset to a low level when three or more zeros are received during two periods of the reset signal ($\overline{RAIS}$).

A diagnostic Loop-Test Mode may be entered by driving the Loop Test Enable Input (LTE) high. In this mode the HDB3 transmitter outputs (+HDB3 OUT, -HDB3 OUT) are internally connected to the HDB3 receiver inputs, and the external HDB3 receiving inputs (+HDB3 IN, -HDB3 IN) are disabled. The NRZ binary output signal (NRZ - Out) corresponds to the NRZ binary input signal (NRZ - In) delayed by approximately 8 clock periods.

The Clock Receiver Output (CKR) is the product of the two HDB3 input signals or-ed together. The CRX clock signal may be derived from the CKR signal with external clock extraction circuitry. In the Loop Test Mode (LTE = 1) CKR is the product of the +HDB3 OUT and -HDB3 OUT signals or-ed together.

The CD22103 may also be used to perform the AMI to NRZ coding/decoding function. To use the CD22103 in this mode, the HDB3/$\overline{AMI}$ control input is driven low.

The RCA CD22103 operates with a 5 V power supply voltage over the full military temperature range at data rates from 50 Kb/s up to 10 Mb/s.

The RCA CD22103 is similar in function and pin configuration to type MJ1471.

The CD22103 types are supplied in 16-lead hermetic dual-in-line ceramic packages (D suffix), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5 to + 8 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to $V_{DD}$ + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE ($P_D$)
For $T_A$ = -40 to + 60° C (PACKAGE TYPE E) ..... 500 mW
For $T_A$ = + 60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For $T_A$ = -55 to + 100° C (PACKAGE TYPE D) ..... 500 mW
For $T_A$ = + 100 to + 125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$)
PACKAGE TYPES D, H ..... -55 to + 125° C
PACKAGE TYPE E ..... -40 to + 85° C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65 to + 150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... + 265° C

**RECOMMENDED OPERATING CONDITIONS**

**For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| DC Supply Voltage Range | 4.5 | 5.5 | V |

**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | SYMBOL | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Quiescent Device Current | $I_{DD}$ | — | — | 100 | μA |
| Operating Device Current $f_{CL}$ = 10 MHz | | — | — | 8 | mA |
| HDB3 Output Low (Sink) Current ($V_{OL}$ = 0.5 V) | $I_{OL1}$ | 1.6 | — | — | |
| HDB3 Output High (Source) Current ($V_{OH}$ = 2.8 V) | $I_{OH1}$ | -10 | — | — | |
| All Other Outputs Low (Sink) Current ($V_{OL}$ = 0.5 V) | $I_{OL2}$ | 1.6 | — | — | |
| All Other Outputs High (Source) Current ($V_{OH}$ = 2.8 V) | $I_{OH2}$ | -1.6 | — | — | |
| Input Low Current | $I_{IL}$ | — | — | -1 | μA |
| Input High Current | $I_{IH}$ | — | — | 1 | |
| Input Low Voltage (Max.) | $V_{IL}$ | — | — | 0.8 | V |
| Input High Voltage (Min.) | $V_{IH}$ | 2 | — | — | |
| Input Capacitance | $C_{IN}$ | — | — | 5 | pF |

**DYNAMIC ELECTRICAL CHARACTERISTICS**

at $T_A$ range of -40° C to 85° C for plastic package
-55° C to 125° C for ceramic package
$V_{DD}$ range of 4.5 V to 5.5 V
$C_L$ = 15 pF

| CHARACTERISTIC | SYMBOL | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| INPUT | | | | | |
| CTX, CRX Input Frequency | $f_{CTX}$, $f_{CRX}$ | .05 | — | 10 | MHz |
| CTX, CRX Input Rise Time * | $t_{rcl}$ | — | — | 1 | μs |
| Fall Time * | $t_{fcl}$ | — | — | 1 | μs |
| NRZ-IN to CTX | | | | | |
| Data Setup Time * | $t_s$ | — | — | 15 | ns |
| Data Hold Time * | $t_H$ | — | — | 15 | ns |
| HDB3 IN to CRX | | | | | |
| Data Setup Time § | $t_s$ | — | — | 55 | ns |
| Data Hold Time * | $t_H$ | — | — | 0 | ns |
| CRX to CKR | | | | | |
| CRX = 8.448 MHz | | | | | |
| Pretrigger ° | $t_p$ | — | — | 20 | ns |
| Delay | $t_d$ | — | — | 20 | ns |

* See Fig. 4 § See Fig. 5 ° See Fig. 6

**DYNAMIC ELECTRICAL CHARACTERISTICS**

at $T_A$ range of -40° C to 85° C for plastic package
-55° C to 125° C for ceramic package
$V_{DD}$ range of 4.5 V to 5.5 V
$C_L$ = 15 pF

| CHARACTERISTIC | SYMBOL | LIMITS | | | UNITS |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| OUTPUT | | | | | |
| Transmitter Coder | | | | | |
| CTX to HDB3 OUT: | | | | | |
| Data Propagation Delay Time * | tDD | — | — | 90 | ns |
| Handling Delay Time | tHD | — | 4 | — | clock period |
| HDB3 OUT Output Pulse Width * | | | | | |
| (Clock duty cycle = 50%) | | | | | |
| fCL = 2.048 MHz | tw | 238 | — | 260 | ns |
| fCL = 8.448 MHz | tw | 53 | — | 65 | ns |
| Receiver Decoder | | | | | |
| CRX to NRZ OUT: | | | | | |
| Data Propagation Delay Times § | tDD | — | — | 90 | ns |
| Handling Delay Time # | tHD | — | 4 | — | clock period |
| HDB3 IN to CKR | | | | | |
| HDB3 Propagation Delay Time † | | | | | |
| LTE = 0 | tIN CKR | — | — | 65 | ns |
| LTE = 1 | | — | — | 30 | ns |

§ See Fig. 5 * See Fig. 4 † See Fig. 2 # See Fig. 3

**TRANSCODER OPERATION**

**Transmitter Coder (See Fig. 2)**

The HDB3/AMI transmitter coder operates on 4 bit serial strings of NRZ binary data and a synchronous transmitter clock (CTX). NRZ binary data is serially clocked into the transmitter on the negative transition of the (CTX) clock. HDB3/AMI coding is performed on the 4 bit string, and HDB3/AMI binary output data is clocked out to the (+ HDB3 OUT, -HDB3 OUT) outputs on the positive transition of the transmitter clock (CTX) 4 clock pulses after the data appeared at the (NRZ-In) input.

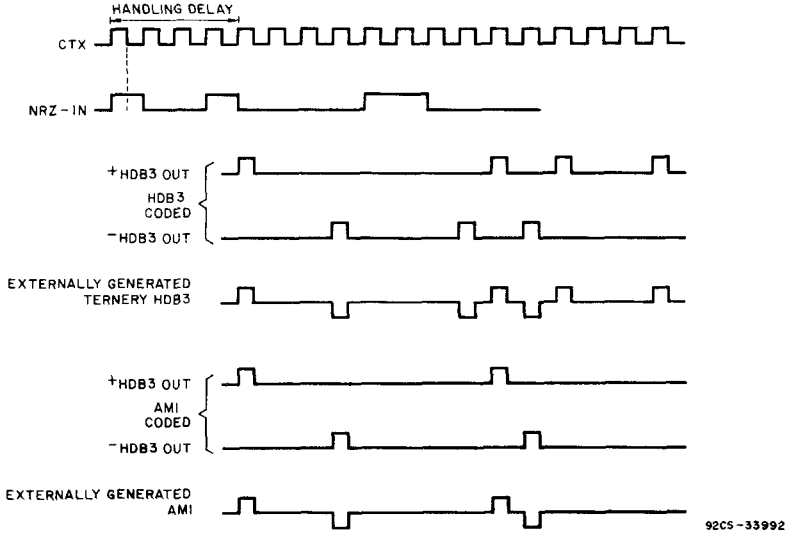



*Fig. 2 - Transmitter coder operation timing waveforms - NRZ to HDB3/AMI coding.*

**Receiver Decoder (See Fig. 3)**

The HDB3/AMI receiver decoder operates on 4 bit serial strings of binary coded HDB3/AMI signals, and a synchronous receiver clock (CRX), HDB3/AMI binary data is serially clocked into the receiver on the positive transition of the (CRX) clock. HDB3/AMI decoding is performed on the 4 bit string, and NRZ binary output data is clocked out to the (NRZ-OUT) output on the positive transition of the receiver clock (CRX) 4 clock pulses after the data appeared at the (+ HDB3 IN, -HDB3 IN) inputs.

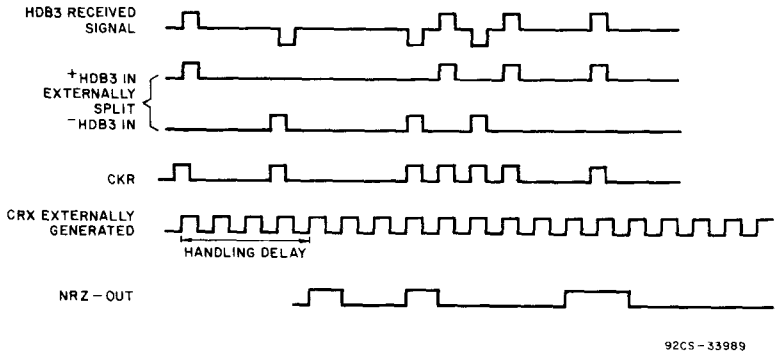



*Fig. 3 - Receiver decoder operation timing waveforms - HDB3 to NRZ decoding.*

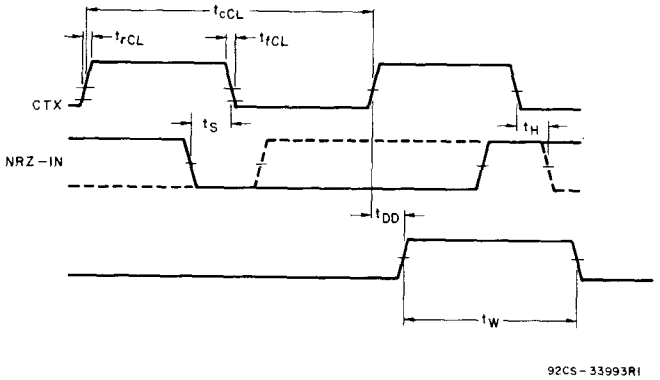



*Fig. 4 - Transmitter coder timing waveforms.*

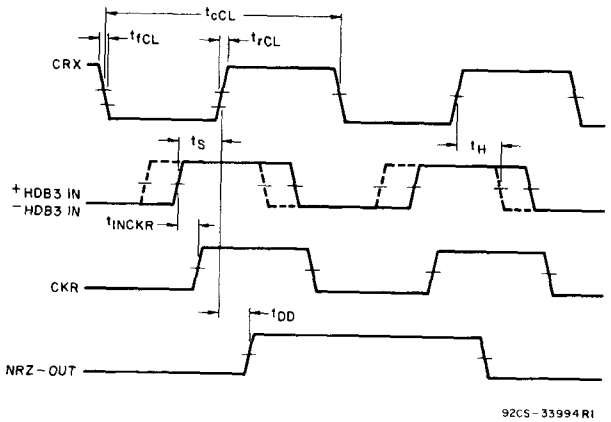



*Fig. 5 - Receiver decoder timing waveforms.*

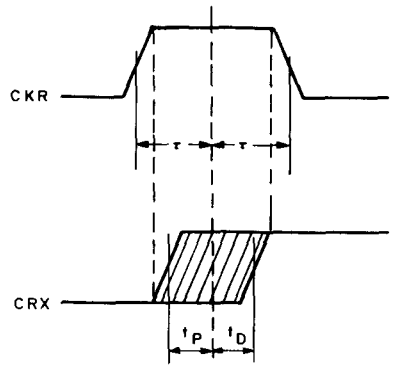



*Fig. 6 - CRX Reconstruction Requirements.*

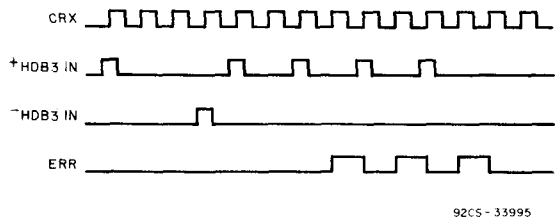



*Fig. 7 - Receiver error-signals timing waveforms.*

**Definition of HDB3 Code Used In CD22103 HDB3 Transcoder (As Per CCITT G703 Annex Recommendations) and Error Detection**

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. HDB3 signal is pseudoternary; the three states are denoted B+, B-, and 0.
2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (See Item 4 below).
3. Marks in the binary signal are coded alternately as B+ and B-in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (See Item 4 below).
4. Strings of four spaces in the binary signal are coded according to the following rules:

   A) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself; it is coded as a mark, i.e., not a violation (i.e., B+ or B-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

   This rule ensures that successive violations are of alternate polarity so that no dc component is introduced.

   B) The second and third spaces of a string are always coded as spaces.

   C) The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V- according to their polarity.

The CD22103 is designed to code and decode HDB3 signals which are coded as binary digital signals (NRZ-In) and (+ HDB3 IN, -HDB3 IN), accompanied by sampling clocks (CTX) and (CRX). The two binary coded HDB3 outputs, (+ HDB3 OUT, -HDB3 OUT) may be externally mixed to create the ternary HDB3 signals (See Fig. 2).

The two binary HDB3 input signals have been split from the input ternary HDB3 in an external line receiver.

**Error Detection**

Received HDB3/AMI binary input signals are checked for coding violations, and an error signal (ERR) is generated as described below.

**HDB3 Signals HDB3/$\overline{\text{AMI}}$ = High**

The error signal (ERR) is flagged high for one CTX period if a violation pulse (±V) is received of the same polarity as the last received violation pulse.

A violation pulse (±V) is considered a reception error and does not cause replacement of the last string of 4 bits to zeros, if:

The received 4 data bits previous to reception of the violation pulse have not been the sequence BX00 (where X = don't care). The error signal (ERR) remains low.

**NOTES:**

The data sequences B000V and BB00V are valid HDB3 codings of the NRZ binary sequence 10000.

The error signal (ERR) count, is the accurate number of all single bit errors.

**AMI Signals HDB3/$\overline{\text{AMI}}$ = Low**

A coding error (ERR) is signaled when a violation pulse (+V) is received.

**In either the HDB3 or AMI mode:**
When high levels appear simultaneously on both HDB3 inputs (+ HDB3 IN, -HDB3 IN) a logical one is assumed in the HDB3/AMI input stream and the error signal (ERR) goes high.

**Alarm Inhibit Signal**

The alarm output (AIS) is set high if in two successive periods of the external Reset Alarm Signal, ($\overline{\text{RAIS}}$), less than three zeros are received.

The alarm output (AIS) is reset low when three or more zeros are received during two reset alarm signal periods.