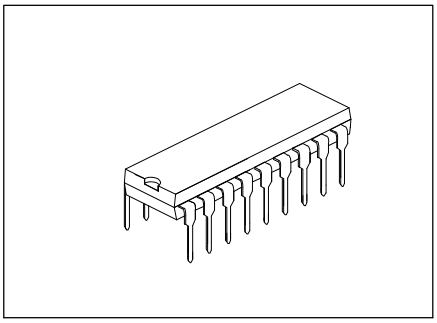
1517 LINEAR INTEGRATED CIRCUIT

2 × 6 W stereo power amplifier



DESCRIPTION

TheCD1517isanintegratedclassBdualoutput amplifier in a plastic single in-line medium power package with fin and a plastic heat-dissipating dual in-line package. The device is primarily developed for multi-media applications.

FEATURES

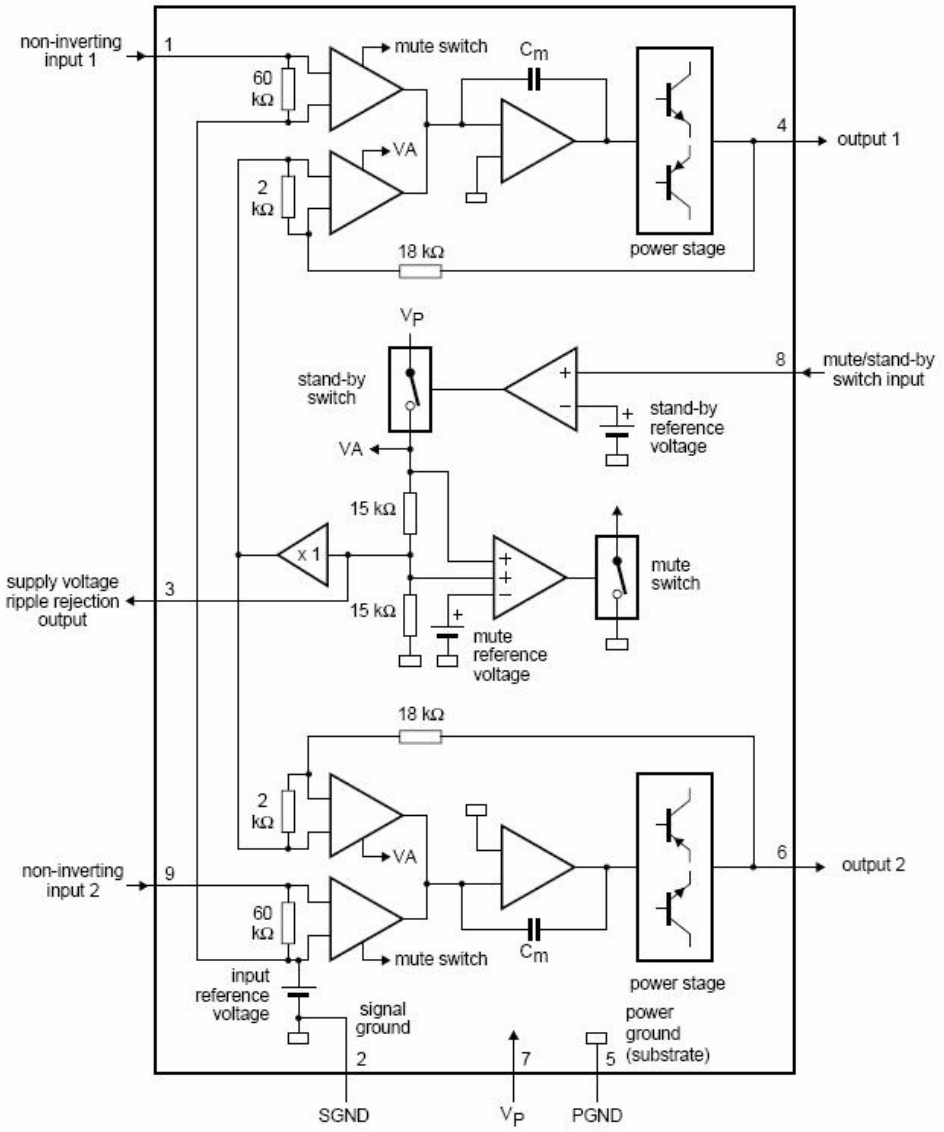
* Requires very few external components
* High output power
* Fixed gain
* Good ripple rejection
* Mute/standby switch
* AC and DC short-circuit safe to ground and VP
* Thermally protected
* Reverse polarity safe
* Capability to handle high energy on outputs (V_P = 0 V)
* No switch-on/switch-off plop
* Electrostatic discharge protection.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		-	-	2.5	A
$I_{q(tot)}$	total quiescent current		-	40	80	mA
I_{sb}	standby current		-	0.1	100	μA
I_{sw}	switch-on current		-	-	40	μA
|ZI|	input impedance		50	-	-	kΩ
P_o	output power	R_L =4Ω; THD = 0.5%	-	5	-	W
		R_L =4Ω; THD = 10%	-	6	-	W
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz	48	-	-	dB
αcs	channel separation		40	-	-	dB
G_v	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		-	50	-	μV
T_c	crystal temperature		-	-	150	℃

1517 LINEAR INTEGRATED CIRCUIT

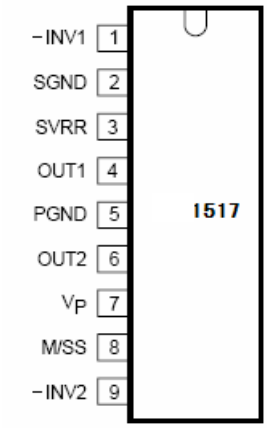
BLOCK DIAGRAM

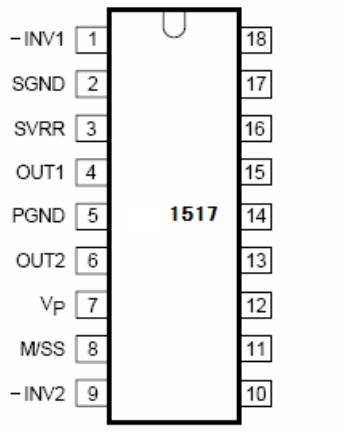


1517 LINEAR INTEGRATED CIRCUIT

PINNING

SYMBOL	PIN	DESCRIPTION
-INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
VP	7	supply voltage
M/SS	8	mute/standby switch input
-INV2	9	non-inverting input 2





1517 LINEAR INTEGRATED CIRCUIT

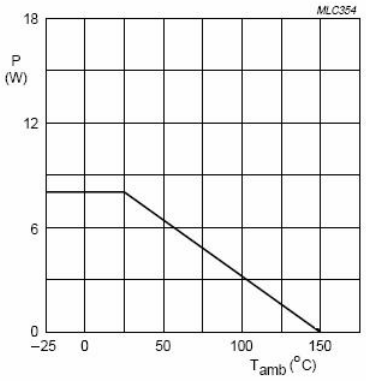
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		-	18	V
$V_{P(sc)}$	AC and DC short-circuit safe voltage		-	18	V
$V_{P(r)}$	reverse polarity		-	6	V
ERG_0	energy handling capability at outputs	V_P =0V	-	200	mJ
I_{OSM}	non-repetitive peak output current		-	4	A
I_{ORM}	repetitive peak output current		-	2.5	A
P_{tot}	total power dissipation	see Fig.4	-	15	W
T_{stg}	storage temperature		-55	+150	° C
Tamb	operating ambient temperature		-40	+85	° C
Tc	crystal temperature		-	150	° C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-p}$	thermal resistance from junction to pins	15	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient	50	K/W



$R_{th\ j-p}$ = 15 K/W.

Fig.4 Power derating curve.

DC CHARACTERISTICS

VP = 14.4 V; Tamb = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current		-	40	80	mA
V_O	DC output voltage		-	6.95	-	V
Mute/standby switch						
V_8	switch-on voltage level	see Fig.5	8.5	-	-	V
Mute condition						
V_O	output signal in mute position	$V_{I(max)}$ =1V; f_i =20Hzto15kHz	-	-	2	mV
Standby condition						
I_{sb}	DC current in standby condition		-	-	100	μA
V_{sw}	switch-on current		-	12	40	μA

Note: 1. The circuit is DC adjusted at VP = 6 to 18 V and AC operating at VP = 8.5 to 18 V.

AC CHARACTERISTICS

VP = 14.4 V; RL = 4 W; f = 1 kHz; Tamb = 25℃; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%; note 1	4	5	-	W
		THD = 10%; note 1	5.5	6.0	-	W
THD	total harmonic distortion	P_o =1W	-	0.1	-	%
f_{lr}	low frequency roll-off	at -3 dB; note 2	-	45	-	Hz
f_{hr}	high frequency roll-off	at -1dB	20	-	-	kHz
G_v	closed loop voltage gain		19	20	21	dB
SVRR	supply voltage ripple rejection	note 3				
	on		48	-	-	dB
	mute		48	-	-	dB
	standby		80	-	-	dB
|Zi|	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s =0Ω; note 4	-	50	-	μV
	on	R_s =10Ω; note 4	-	70	100	μV
	mute	note 5	-	50	-	μV
α_{cs}	channel separation	R_s =10 W	40	-	-	dB
$\lvert\triangle G_v\rvert$	channel unbalance		-	0.1	1	dB

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0Ω, maximum ripple amplitude of 2 V (p-p) and a frequency between 100 Hz and 10 kHz.
4. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of R_s (V_I = 0 V).

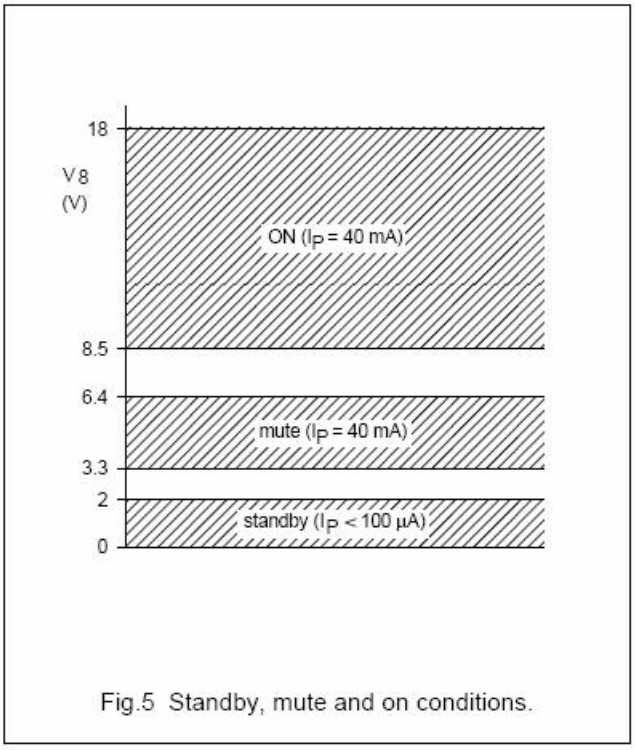


Fig.5 Standby, mute and on conditions.

APPLICATION INFORMATION

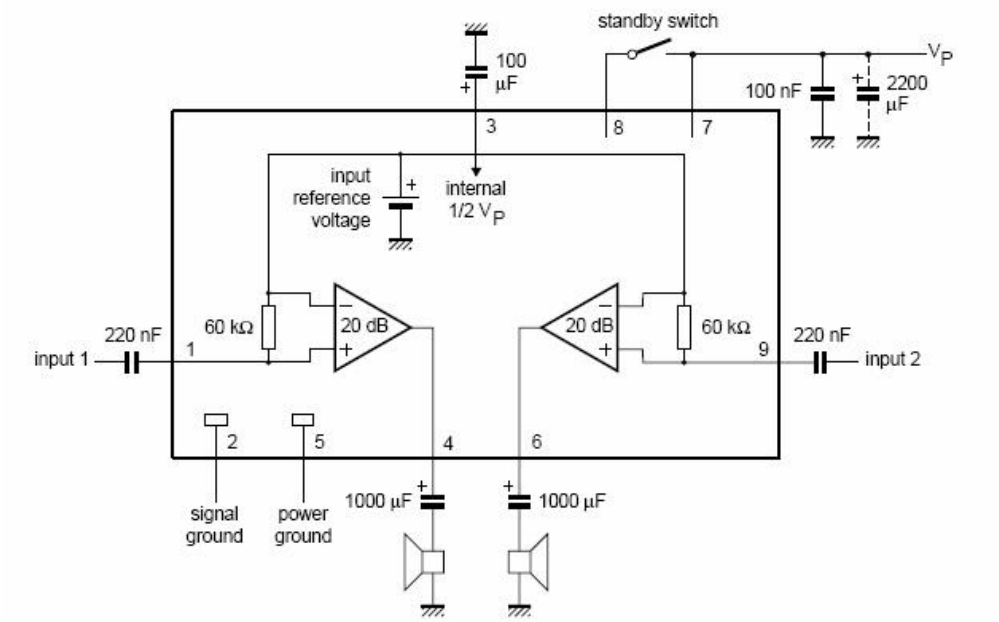


Fig.6 Application circuit diagram.

1517 LINEAR INTEGRATED CIRCUIT

PACKAGE OUTLINE

DIP-18-300 UNIT：mm