CAT7117

Dual Channel 800mA High Efficiency Step-Down DC/DC Converter

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General Description

The CAT7117 is a high efficiency step-down DC/DC converter using a constant frequency, current mode architecture. The device integrates a main switch and a synchronous rectifier for high efficiency without an external schottky diode. Supply current during operation is only 300µA and drops to ≤ 1µA in shutdown. The CAT7117 can supply 800mA of load current from 2.5V to 5.5V input voltage. The output voltage can be regulated as low as 0.6V.
Switching frequency is internally set at 1.8MHz, allowing the use of small surface mount inductors and capacitor. It can also run 100% duty cycle for low dropout applications.

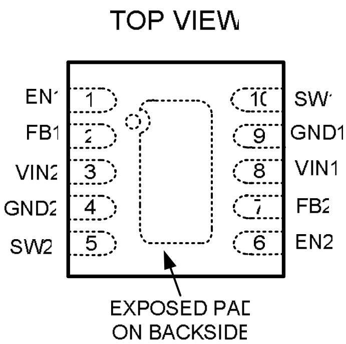
Features

- High Efficiency up to 95%
- Low Quiescent Current < 300uA (active mode)
- 2.5V to 5.5V Input Voltage Range
- 800mA Output Current on each Channel
- Fix Frequency Operation
- Full Duty ratio, 0 – 100% in Dropout
- 0.6V Reference Allows Low Output Voltages
- Current Mode Operation
- Internal soft-start
- Over-temperature Protected
- < 0.1µA Shutdown Current
- DFN3x3 small Package
- RoHS Compliant (100% Green available)

Application

- Cellular Telephones
- PDAs and Smart Phones
- MP3 Players
- Microprocessors and DSP Core Supplies
- Wireless and DSL Card
- Digital Still Cameras
- Slim-Type DVD
- Portable Instruments

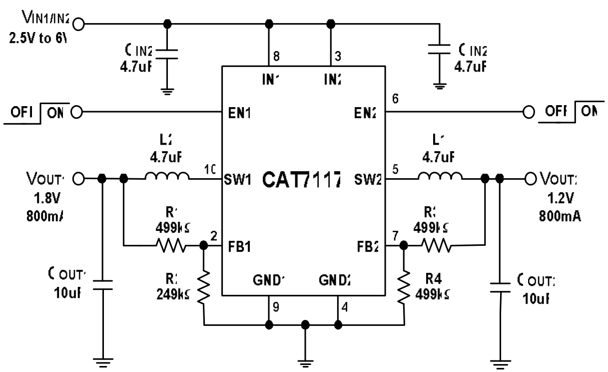
Pin Configuration



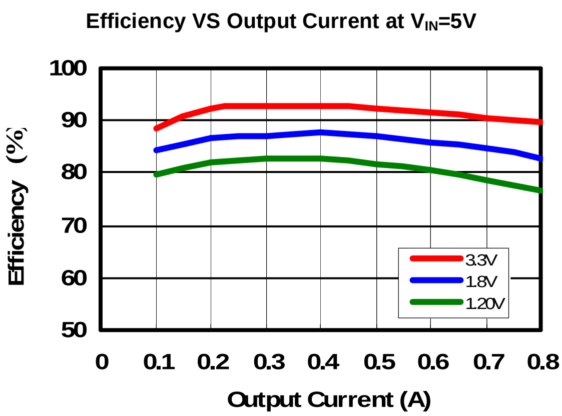
Ordering Information

Part Number	Package	Ship
CAT7117CE	DFN10 3x3	2500/ Tape & Reel

Typical Application



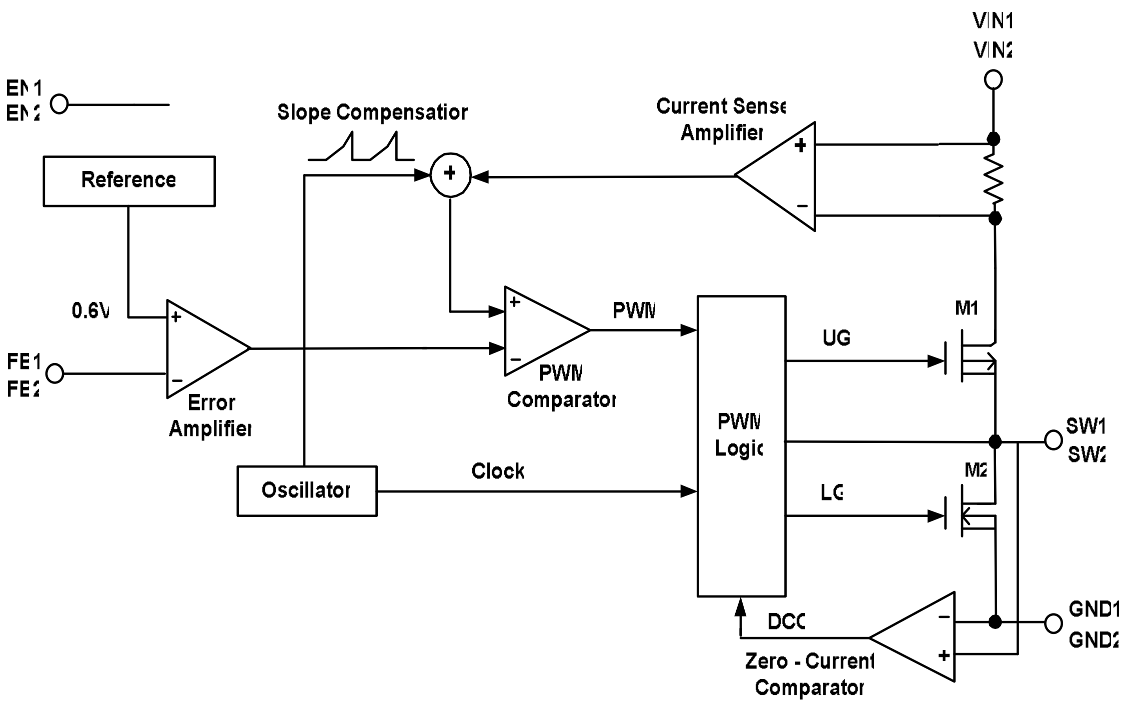
Efficiency Table



Pin Description

Pin	Symbol	Description
1	EN1	Channel1 Regulator enable control input Pin. Drive EN1 above 1.5V to turn on Channel1. Drive EN1 below 0.3V to turn it off (shutdown current < 0.1uA).
2	FB1	Channel1 Voltage feedback Pin.
3	VIN2	Channel2 Main supply Pin.
4	GND2	Channel2 Ground Pin.
5	SW2	Channel2 Power switch output
6	EN2	Channel2 Regulator enable control input Pin. Drive EN2 above 1.5V to turn on Channel2. Drive EN2 below 0.3V to turn it off (shutdown current < 0.1uA).
7	FB2	Channel2 Voltage feedback Pin.
8	VIN1	Channel1 Main supply Pin.
9	GND1	Ground Pin.
10	SW1	Channel1 Power switch output

Function Block Diagram



Absolute Maximum Ratings

Input Supply Voltage…………GND- 0.3V to +6.5V
SW Voltage …………….……. - 0.3 to VIN+0.3V
ENB, VFB Voltage……….………. -0.3V to VIN
ESD Classification…………………………Class 2
Junction Temperature Range……………..…125℃
Operating Temperature ……….-20℃ to 85℃ (note2)
Storage Temperature Range ……....-65℃ to 150℃
Lead Temperature (Soldering 10s) ………… 260℃

Package Thermal Characteristics

Thermal Resistance	θJA	θJC	
DFN10 3mx3m	50	10	℃/W

*note1: The IC has a protection circuit against static electricity. Do not apply high static electricity or high voltage that exceeds the performance of the protection circuit to the IC.
*note2: Fully production test at +25℃. Specificati ons over the temperature range are guaranteed by design and characterization.

Electrical Characteristic

(Recommended Operating Conditions, Unless Otherwise Noted; V_{IN} = 3.6V; Temperature = 0 - 70 °C (typical = 25 °C))

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage	V_{IN}		2.5		5.5	V
Feedback Current	I_{VFB}		-30	0.5	30	nA
Regulated Feedback Voltage	V_{FB}	T_A = 25℃ -40℃ ≦ T_A ≦ 85℃	0.588 0.582	0.6 0.6	0.612 0.618	V
Reference Voltage Line Regulation	$\triangle V_{FB}$	V_{IN} = 2.5V to 5.5V		0.04	0.4	%V
Output Voltage Line Regulation	$\triangle V_{OUT}$	V_{IN} = 2.5V to 5.5V		0.04	0.4	%V
Output Voltage Load Regulation	$V_{LOADRGE}$			0.5		%
Shutdown Current	I_S	V_{EN} = 0V, V_{IN} = 5.5V		0.01	1	μA
Quiescent Current	I_Q	V_{EN} = V_{IN}, V_{FB} = 0.65V, No switching		300		μA
SW Leakage Current	I_{LEAK}	V_{EN} = 0V, V_{IN} = 5.5V V_{SW} = 0V or 5.5V	-1		1	μA
PMOSFET On Resistance	R_{DSONP}	I_{SW} = 100mA		0.35		Ω
NMOSFET On Resistance	R_{DSONN}	I_{SW} = -100mA		0.24		Ω
PMOSFET Current Limit	I_{PCL}	Duty Cycle = 100% Current Pulse Width < 1ms	0.9	1.2	1.4	A
Oscillator Frequency	F_{OSC}		1.2	1.6	2.0	MHz
Thermal Shutdown Threshold	T_S			145		℃
EN high level input voltage	V_{EN}	- 40℃ ≦ T_A ≦ +85℃	0.9			V
EN low level input voltage	V_{EN}	- 40℃ ≦ T_A ≦ +85℃			0.3	V
EN Input Current	I_{EN}	V_{EN} = 0V to V_{IN}	-1		1	μA

*note: Fully production test at +25℃. Specificatio ns over the temperature range are guaranteed by design and characterization.

Function Description

The CAT7117 is a constant frequency current mode PWM step-down converter. The CAT7117 is optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. The CAT7117 uses an external resistor divider to set the output voltage from 0.6V to 5.5V. The device integrates both a main switch and a synchronous rectifier, which provides high efficiency and eliminates an external Schottky diode. The CAT7117 can achieve 100% duty cycle. The duty cycle D of a step-down converter is defined as:
D = TON * FOSC * 100% ≒ VOUT/VIN * 100%
where TON is the main switch on time, and FOSC is the oscillator frequency.

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load and line response and protection of the internal main switch and synchronous rectifier. The CAT7117 switches at a constant frequency (1.8MHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until either the next cycle starts or the inductor current drops to zero. The device skips pulses to improve efficiency at light load.

Internal soft-start

The CAT7117 features an internal soft−start function, which reduces inrush current and overshoot of the output voltage. Soft−start is achieved by ramping up the reference voltage (V_{ref}) which is applied to the input of the error amplifier. The typical soft−start time is about 2 msec and depends on components values on AP circuit.

Dropout Operation

The CAT7117 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the P MOSFET current limit. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor.

Short Circuit Protection

The CAT7117 has short circuit protection. When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the P MOSFET current limit. The P MOSFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

Maximum Load current

The CAT7117 can operate down to 2.5V input voltage; however the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases match other diagrams in this datasheet.

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{IN}RMS = I_{OUT}\sqrt{D \times (1 - D)}$$

where D is the duty cycle, I_{inRMS} is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times I_{IN}RMS^2$$

where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and affects the load transient response. Higher inductance reduces the inductor's ripple current and induces lower output ripple voltage. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{in} - V_{out}}{F_S \times L} \bullet \frac{V_{out}}{Vin}$$

$$\Delta V_{out} = \Delta I \times ESR$$

Although increase the inductance reduce the ripple current and voltage, but the large inductance reduces the regulator's response time to load transient. Increasing the switching frequency (Fs) for a given inductor also reduces the ripple current and voltage but it will increase the switching loss of the power MOS.

To select the inductor value, a guideline is to choose the ripple current (△I) to be approximately 10%~50% of the maximum output current. Once the inductor value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) are reasonable tolerances that most manufacturers can meet. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitors Selection

An output capacitor is required to filter the output and supply the load transient current. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. These requirements are met with a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by using the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$\text{Number Of Capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

$\triangle V_{ESR}$ = change in output voltage due to ESR (assigned by the designer).

△IOUT = load transient.

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Consult the capacitors manufacturer to make sure the decoupling requirements.

Output Voltage

The output voltage is set using the FB pin and a resistor divider connected to the output as shown in next page AP Circuit. The FB pin voltage is 0.6V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$V_{FB} = V_{out} \times \frac{R_2}{(R_1 + R_2)}$$

Thus the output voltage is:

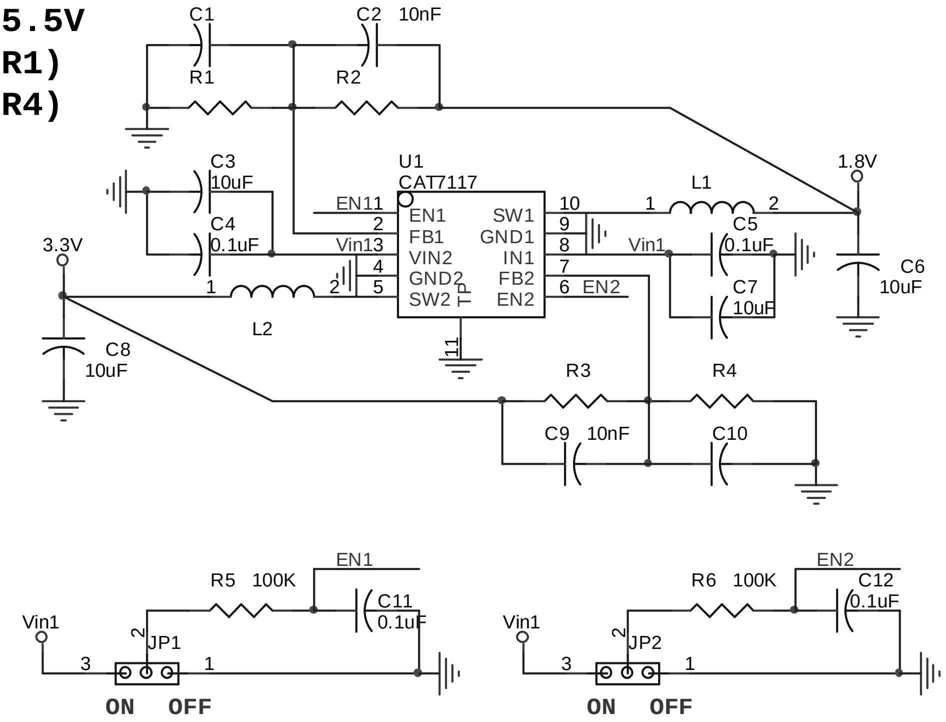
$$V_{out} = 0.6 \times \frac{(R_1 + R_2)}{R_2}$$

Application & BOM List Table:

V_{OUT}	L1/L2	R2/R3	R1/R4
3.3V	4.7uH	300KΩ	68KΩ
1.8V	4.7uH	1MΩ	500KΩ
1.2V	4.7uH	300KΩ	300KΩ
1.0V	4.7uH	220KΩ	330KΩ

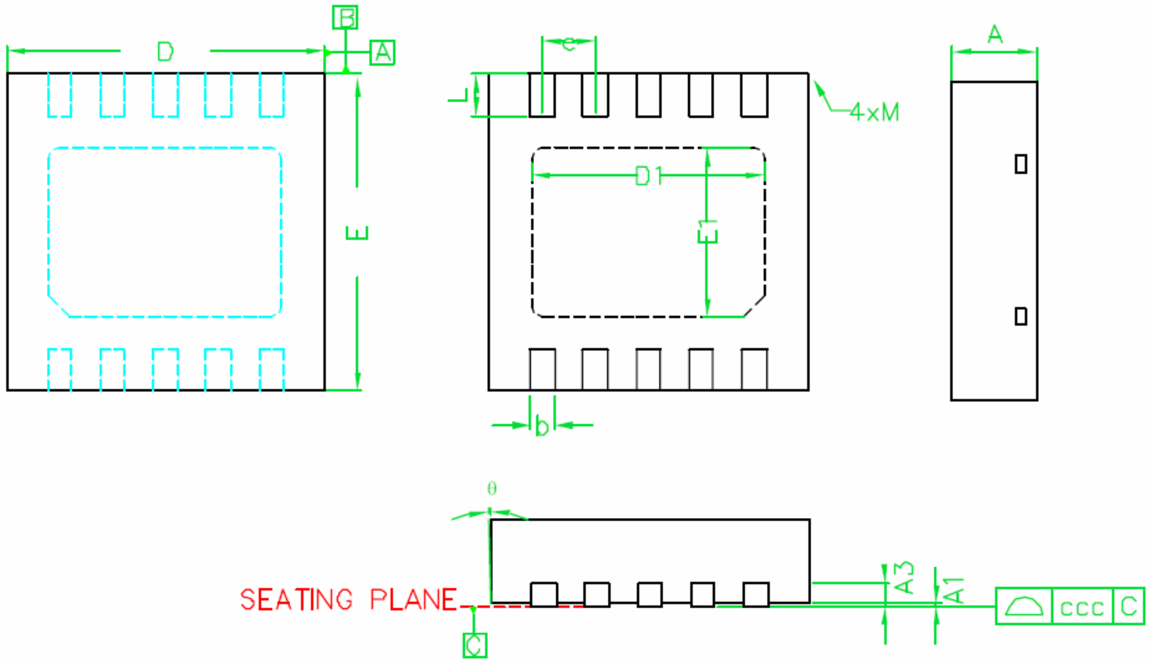
CAT7117 AP Circuit

Vin1, Vin2=2.5V~5.5V
Vout1=0.6*(1+R2/R1)
Vout2=0.6*(1+R3/R4)



Package Dimensions

DFN3X3 PACKAGE

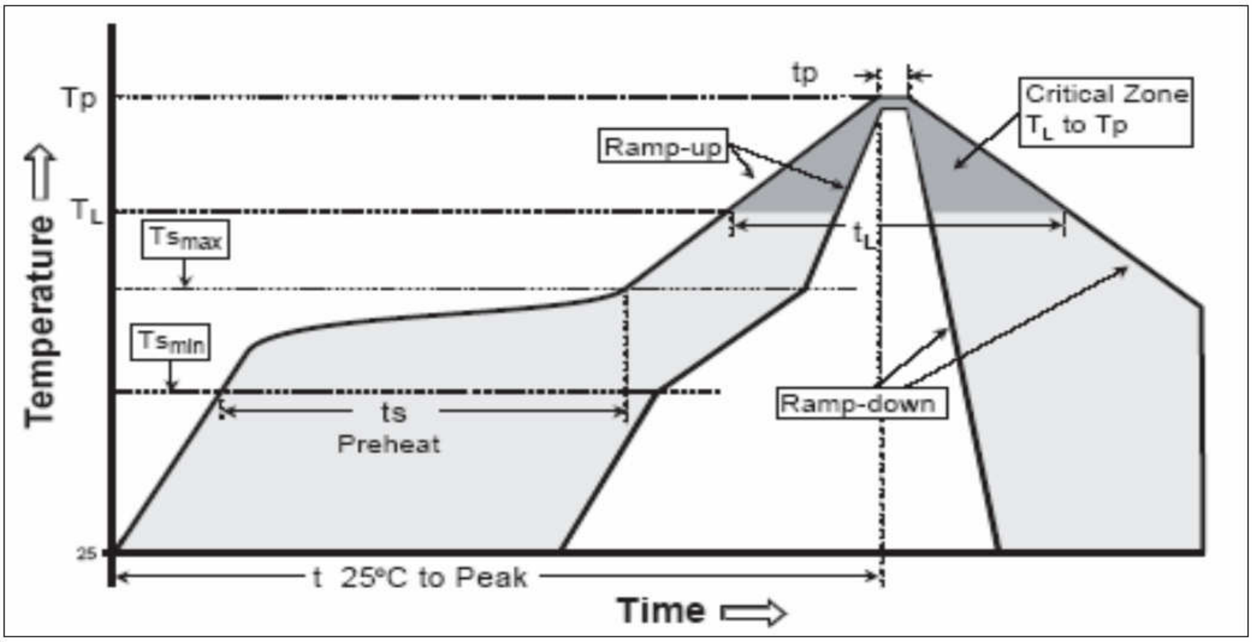


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.010	0.030
A3	---	0.20REF.	---
b	0.18	0.23	0.28
D	2.95	3.00	3.03
D1	---	2.20BSC	---
E	2.95	3.00	3.03
E1	---	1.60BSC	---
e	---	0.5BSC	---
L	0.35	0.40	0.45
ccc	---	0.08	---
M	---	---	0.05
θ	-12	---	0
Burr	0	0.03	0.06

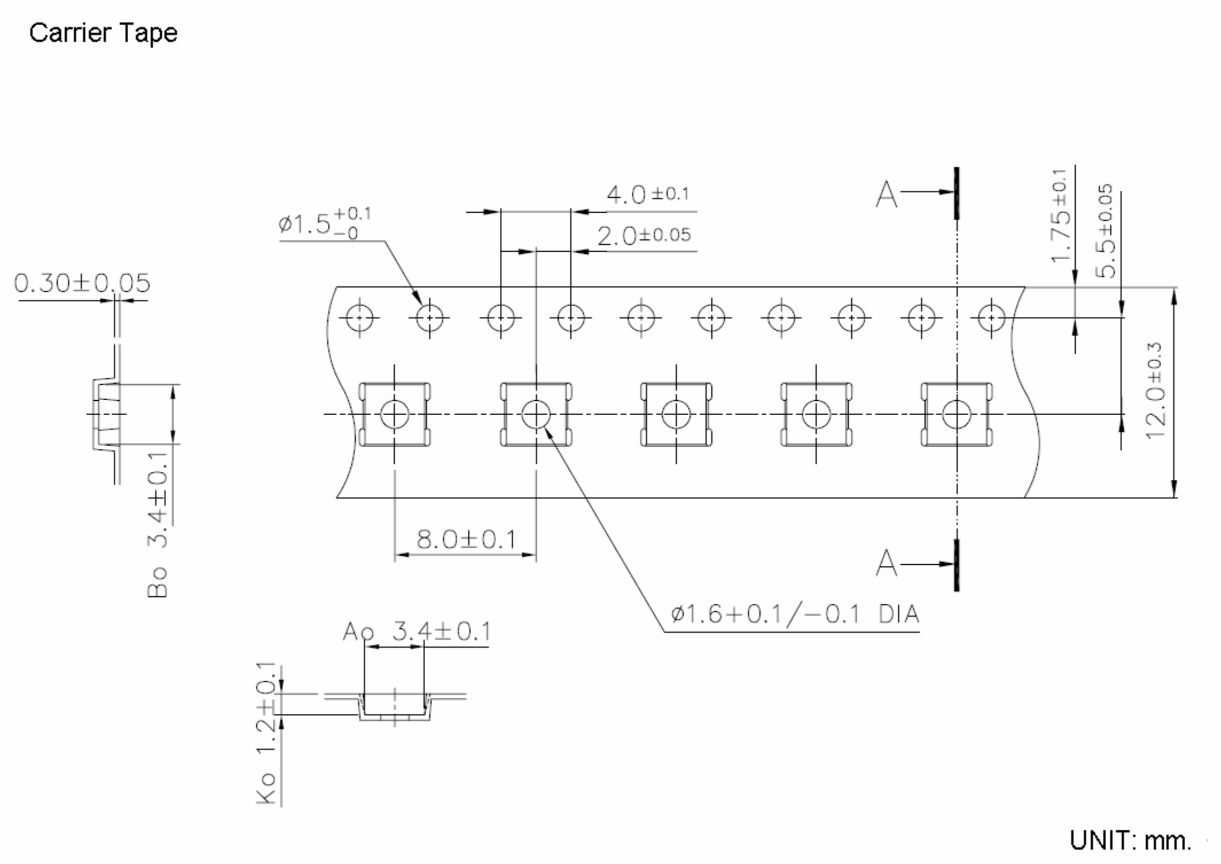
Classification Reflow Profiles

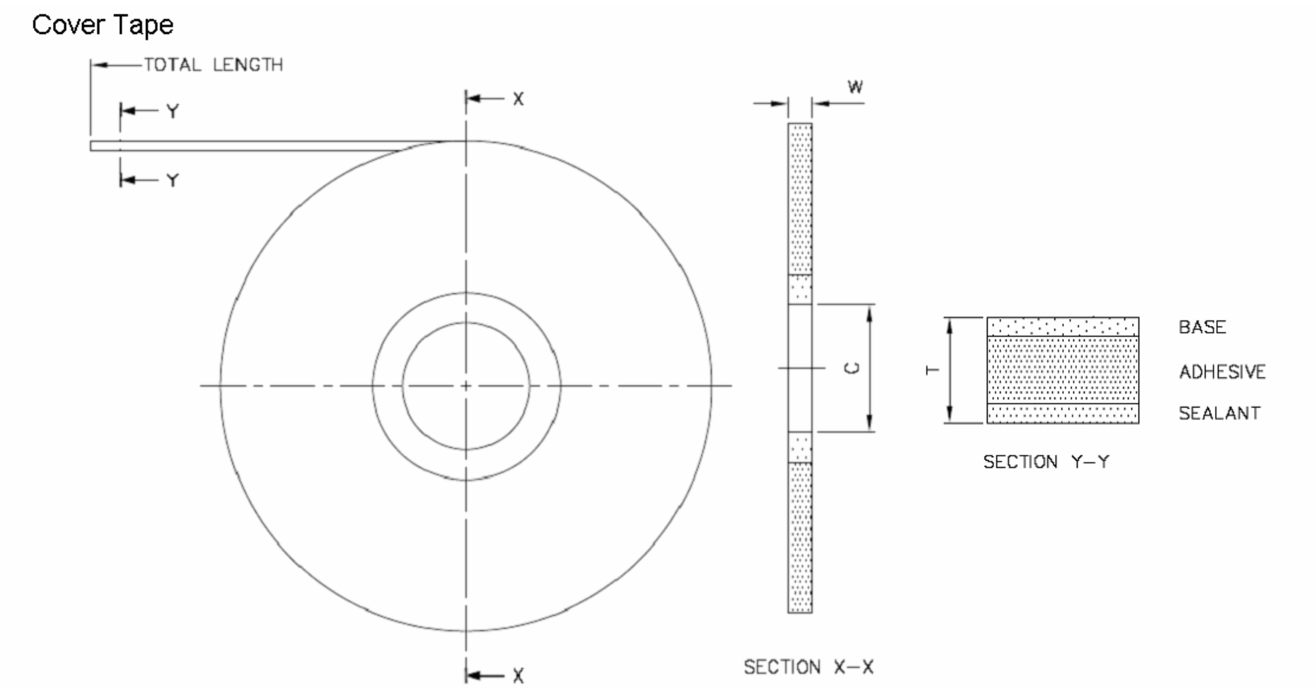
Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0/-5 ℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.



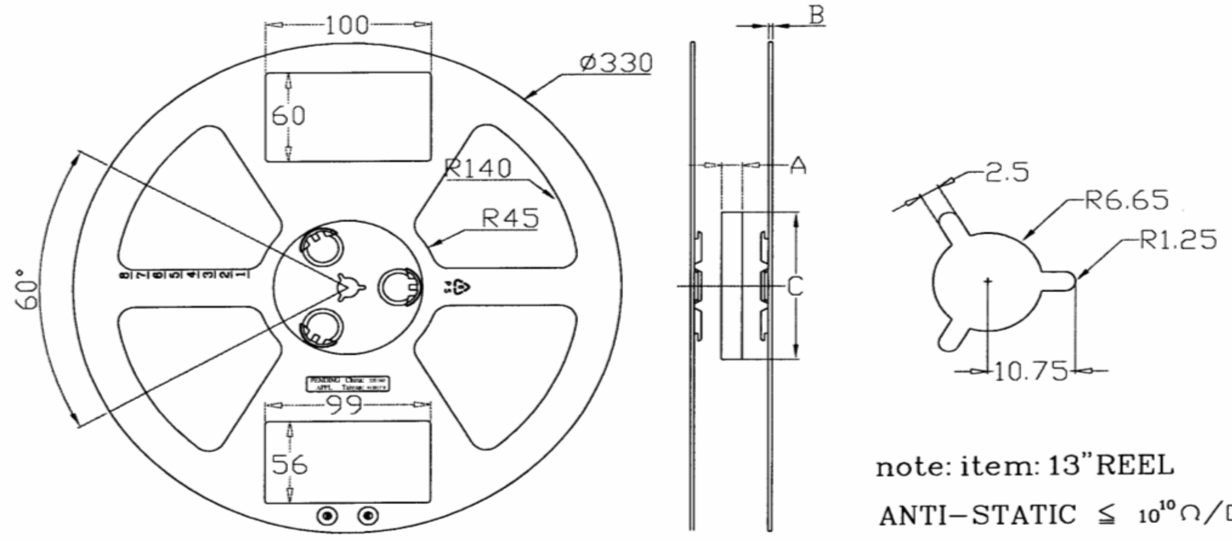
Carrier Tape & Reel Dimensions





CARRIER TAPE WIDTH	C NOMINAL	T	W	TOTAL LENGTH
12mm	76.2mm	0.06±0.01mm	9.3±0.1mm	300M

Reel Outline



note: item: 13"REEL

ANTI−STATIC ≦ 10^{10}Ω/□

material: P.S

SPEC	12	16	24	32	44	56	72
DIM A $^{+1.5}_{-0.5}$	12.5	16.5	24.5	32.5	44.5	57	73
DIM B ±0.2	2.3	2.3	2.3	2.3	2.3	2.3	2.3
DIM C ±1.5	99	99	99	99	99	99	99

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