

# 10 Channel Automotive LED Display Driver

## FEATURES

- Automotive “load dump” protection (40V)
- 10 independent LED channels
- Up to 50mA output per channel
- Overvoltage detection at 19V
- Serial interface for channel programming
- Daisy chain output for multi-driver cascading
- LED blanking control
- Operating temperature from -40°C to +125°C
- 20-pin SOIC package

## APPLICATIONS

- Automotive lighting
- White and other color high brightness LEDs
- Multi-color high-brightness LED cluster displays
- General LED lighting

## ORDERING INFORMATION

| Part Number | Package              | Quantity per Reel | Package Marking |
|-------------|----------------------|-------------------|-----------------|
| CAT310J     | SOIC-20              | 1000              | CAT310J         |
| CAT310W     | SOIC-20<br>Lead free | 1000              | CAT310W         |

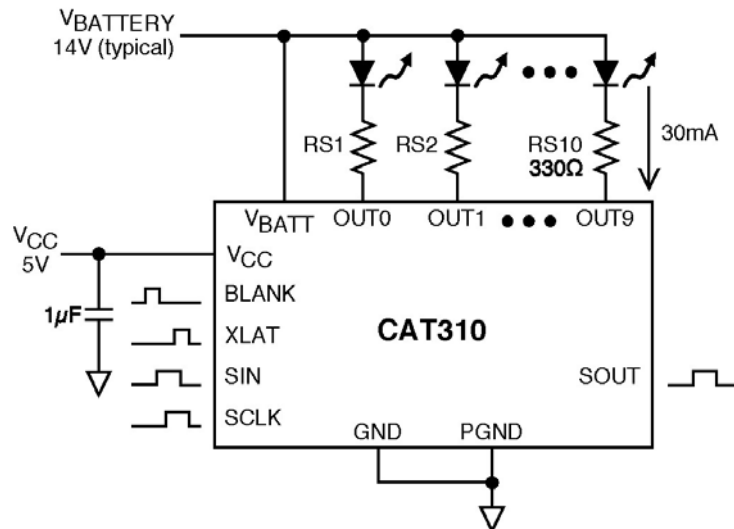
## PRODUCT DESCRIPTION

The CAT310 is a 10-channel LED driver for automotive and other lighting applications. All LED output channels are driven from a low on-resistance open-drain High Voltage CMOS Nch-FETs and are fully compliant with “Load Dump” transients of up to 40 volts. The LED bias current of each channel can be set independently using an external series ballast resistor, making the device ideal for multi-color instrumentation displays.

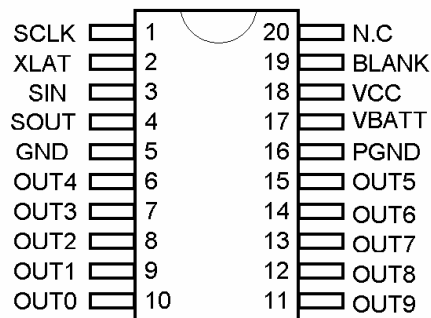
A high-speed serial interface (suitable with both 3.3 volt and 5 volt systems) feeding a 10 bit shift register is used to program the desired state (on/off) of each channel. The device offers a blanking control pin (BLANK) which can be used to disable all channels on demand. A serial output data pin (SOUT) is provided to daisy-chain devices in large cluster LED applications

During initial power up all channels are reset and cleared via an under-voltage lock out (UVLO) detector and for added protection all channels are disabled in the event of a battery over-voltage condition (19 volts or more).

## TYPICAL APPLICATION CIRCUIT



## PIN DIAGRAM



SOIC 20-pin package

## ABSOLUTE MAXIMUM RATINGS

| Parameter                                                             | Rating            | Unit |
|-----------------------------------------------------------------------|-------------------|------|
| VCC voltage                                                           | 7                 | V    |
| Input voltage range (SIN, SCLK, BLANK, XLAT)                          | -0.3V to VCC+0.3V | V    |
| SOUT voltage range                                                    | -0.3V to VCC+0.3V | V    |
| Peak OUT0 to OUT9 voltage                                             | 40                | V    |
| VBATT input voltage                                                   | 40                | V    |
| DC output current on OUT0 to OUT9                                     | 70                | mA   |
| Storage Temperature Range                                             | -55 to +160       | °C   |
| Operating Junction Temperature Range                                  | -40 to +150       | °C   |
| Lead Soldering Temperature (10sec.)                                   | 300               | °C   |
| ESD Rating: Low Voltage Pins<br>Human Body Model<br>Machine Model     | 3000<br>300       | V    |
| ESD Rating: VBATT, OUT[0:9] pins<br>Human Body Model<br>Machine Model | 1000<br>100       | V    |

## RECOMMENDED OPERATING CONDITIONS

| Parameter                       | Range       | Unit |
|---------------------------------|-------------|------|
| VCC                             | 3.0 to 5.5  | V    |
| Voltage applied to OUT0 to OUT9 | 9 to 17     | V    |
| Output current on OUT0 to OUT9  | 0 to 50     | mA   |
| Ambient Temperature Range       | -40 to +125 | °C   |

## ELECTRICAL OPERATING CHARACTERISTICS

**DC Characteristics** VCC = 5.0V, -40°C ≤ T<sub>A</sub> ≤ 125 °C, over recommended operating conditions unless specified otherwise.

| Symbol                             | Name                                                            | Conditions                                      | Min                    | Typ     | Max                | Units |
|------------------------------------|-----------------------------------------------------------------|-------------------------------------------------|------------------------|---------|--------------------|-------|
| I <sub>STBY</sub>                  | Standby Quiescent Current                                       | Static input signal. All outputs turned off.    |                        | 1       | 10                 | μA    |
| V <sub>OVP</sub>                   | VBATT Over Voltage Protection Trigger threshold                 |                                                 | 17                     | 19      | 21                 | V     |
| V <sub>UVLO</sub>                  | VCC Under Voltage Lockout Trigger threshold                     |                                                 |                        | 1.7     | 2.5                | V     |
| R <sub>SW</sub>                    | Switch on resistance for OUT0 to OUT9                           | I <sub>O(n)</sub> = 30mA                        | 2                      | 5       | 12                 | Ω     |
| I <sub>O(n)LKG</sub>               | OUT0 to OUT9 Output Switch Leakage                              | V <sub>(OUT(n))</sub> = 15V                     |                        | 0.1     | 10                 | μA    |
| I <sub>XLAT</sub>                  | XLAT Internal Pull-down current                                 | XLAT = V <sub>CC</sub><br>XLAT = 0.3V           | 4<br>1                 | 10<br>3 | 30<br>6            | μA    |
| I <sub>BLANK</sub>                 | BLANK Internal Pull-up current                                  | BLANK = 0V<br>BLANK = V <sub>CC</sub> - 0.3V    | 4<br>1                 | 10<br>3 | 30<br>6            | μA    |
| V <sub>IH</sub><br>V <sub>IL</sub> | Logic high input voltage<br>Logic low input voltage             |                                                 | 0.3 V <sub>CC</sub>    |         | 0.7V <sub>CC</sub> | V     |
| I <sub>IL</sub>                    | Logic Input leakage current (SCLK, SIN)                         | V <sub>I</sub> = V <sub>CC</sub> or GND         | -5                     | 0       | 5                  | μA    |
| V <sub>OH</sub><br>V <sub>OL</sub> | SOUT logic high output voltage<br>SOUT logic low output voltage | I <sub>OH</sub> = -1mA<br>I <sub>OL</sub> = 1mA | V <sub>CC</sub> - 0.3V |         | 0.3                | V     |

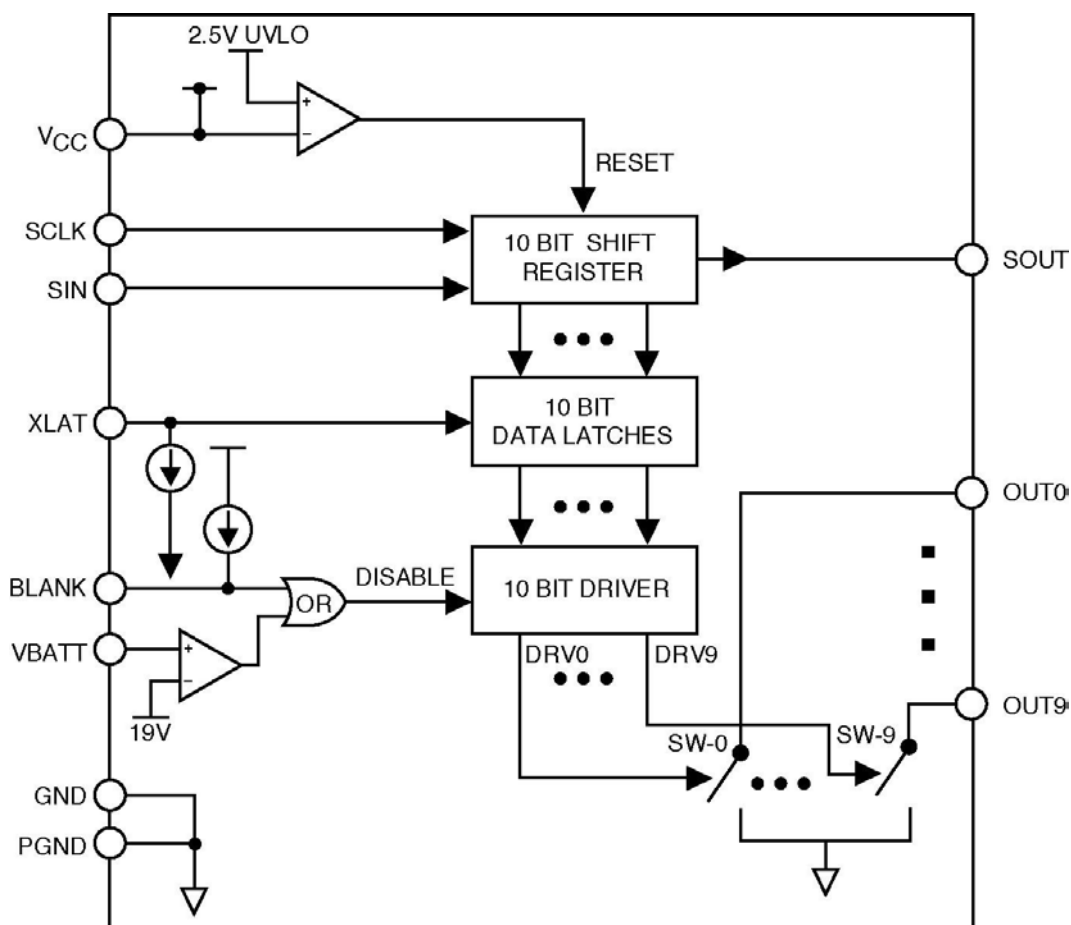
## ELECTRICAL OPERATING CHARACTERISTICS

**Switching Characteristics**  $V_{CC} = 5.0V$ ,  $-40^{\circ}C \leq T_A \leq 125^{\circ}C$ , over recommended operating conditions unless specified otherwise.

| Symbol      | Name                        | Conditions                   | Min | Typ | Max | Units |
|-------------|-----------------------------|------------------------------|-----|-----|-----|-------|
| <b>SCLK</b> |                             |                              |     |     |     |       |
| $f_{SCLK}$  | SCLK Clock Frequency        |                              |     |     | 10  | MHz   |
| $t_{wh/wl}$ | SCLK Pulse width            | High or Low                  | 30  |     |     | ns    |
| <b>SIN</b>  |                             |                              |     |     |     |       |
| $t_{su}$    | Setup time SIN to SCLK      |                              | 10  |     |     | ns    |
| $t_h$       | Hold time SIN to SCLK       |                              | 10  |     |     | ns    |
| <b>XLAT</b> |                             |                              |     |     |     |       |
| $t_w$       | XLAT Pulse width            | SIN to SCLK                  | 20  |     |     | ns    |
| $t_h$       | Hold time<br>SCLK to XLAT   |                              | 20  |     |     | ns    |
| $t_r$       | SOUT rise time (10% to 90%) | $C_L = 15pF$                 |     | 20  |     | ns    |
| $t_f$       | SOUT fall time (90% to 10%) | $C_L = 15pF$                 |     | 15  |     | ns    |
| $t_{pd}$    | Propagation delay time      | Blank $\uparrow$ to OUT(n)   |     | 25  |     | ns    |
| $t_{pd}$    | Propagation delay time      | Blank $\downarrow$ to OUT(n) |     | 25  |     | ns    |
| $t_{pd}$    | Propagation delay time      | SCLK to SOUT                 |     | 25  |     | ns    |

All logic inputs contain Schmitt trigger inputs.

## BLOCK DIAGRAM



## PIN DESCRIPTIONS

**VCC** is the supply input for the internal logic and is compatible with both 3.3V and 5V systems. The logic is held in a reset state until VCC exceeds 2.5V. It is recommended that a small bypass ceramic capacitor (1uF) be placed between VCC and GND pins on the device.

**SIN** is the CMOS logic pin for delivering the serial input data stream into the internal 10-bit shift register. The most recent or last data value in the serial stream is used to configure the state of output channel “zero” (OUT0). During the initial power up sequence all contents of the shift register are reset and cleared to zero.

**SCLK** is the CMOS logic pin used to clock the internal shift register. On each rising edge of clock, the serial data will advance through one stage of the shift register.

**XLAT** is the CMOS logic input used to transfer data from the 10-bit shift register into the output channel latches. An internal pull-down current of 10 microampere is present on this pin. When XLAT is low, the state of each output channel remains unchanged. When XLAT is driven high, the contents of the shift register appear at their respective output channels. An external pull-up resistance of 10kΩ or less is adequate for logic high.

**PGND, GND** pins should be connected to the ground on the PCB.

**BLANK** is the CMOS logic input (active high) used to temporarily disable all outputs. An internal pull-up current of 10 microampere is present on this pin. The BLANK pin must be driven to a logic low in order for channel outputs to resume normal operation. An external pull-down resistance of 10kΩ or less is adequate for logic low.

**SOUT** is the CMOS logic output used for daisy chain applications. The serial output data stream is fed from the last stage of the internal 10-bit shift register. On each rising edge of the clock, the SOUT value will be updated. The data value present on this pin is identical to the data value being used for configuring the state of output channel nine (OUT9). At initial power up, the SOUT data stream will contain all zeroes until the shift register has been fully loaded.

**VBATT** input monitors the battery voltage. If an over-voltage, above 19V typical, is detected, all outputs are disabled. Upon conclusion of the over-voltage condition, all outputs resume normal operation. The current drawn by the VBATT pin is less than 1 microampere during normal operation.

**OUT0-OUT9** are the ten LED outputs connected internally to the switch N-channel FETs. They sink currents up to 50mA per channel and can withstand transients up to 40V compatible with automotive “load dump”. The output on-resistance is 5Ω, and the off-resistance is 5MΩ.

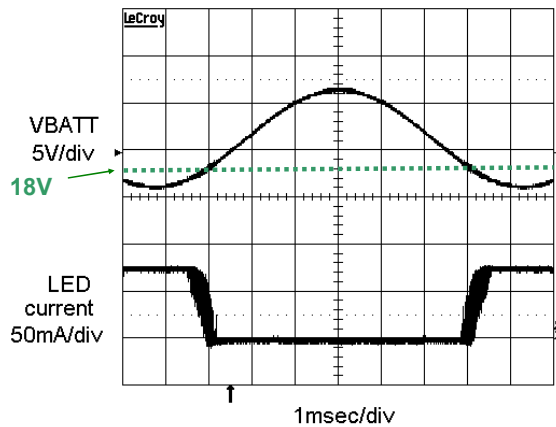
## PIN TABLE

| Pin Number | Pin Name    | Description/Function                                                    |
|------------|-------------|-------------------------------------------------------------------------|
| 1          | SCLK        | Clock input for the data shift register.                                |
| 2          | XLAT        | Control input for the data latch.                                       |
| 3          | SIN         | Serial data input.                                                      |
| 4          | SOUT        | Serial data output.                                                     |
| 5          | GND         | Ground.                                                                 |
| 6-10       | OUT4 - OUT0 | Open drain outputs.                                                     |
| 11-15      | OUT9 - OUT5 | Open drain outputs.                                                     |
| 16         | PGND        | Ground for LED driver outputs.                                          |
| 17         | VBATT       | Battery sense input.                                                    |
| 18         | VCC         | Power supply voltage for the logic                                      |
| 19         | BLANK       | Blank input. When BLANK is high, all the output drivers are turned off. |
| 20         | N.C.        | No connect.                                                             |

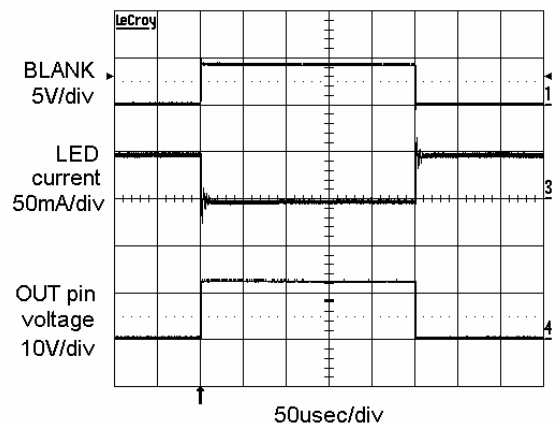
## TYPICAL CHARACTERISTICS

VCC = 5V, VBATT = 14V, T<sub>AMB</sub> = 25°C, unless otherwise specified.

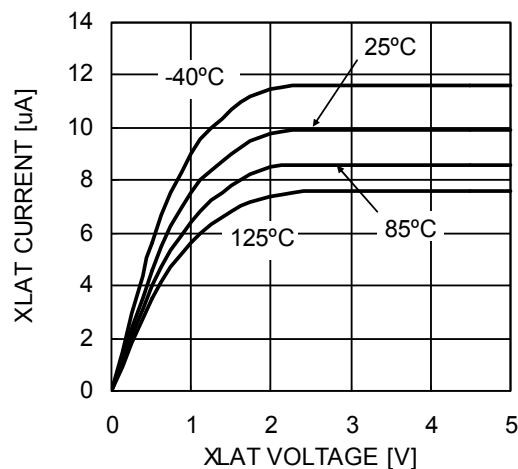
**VBATT Overvoltage Detection**  
 Amplitude between 16V and 26V



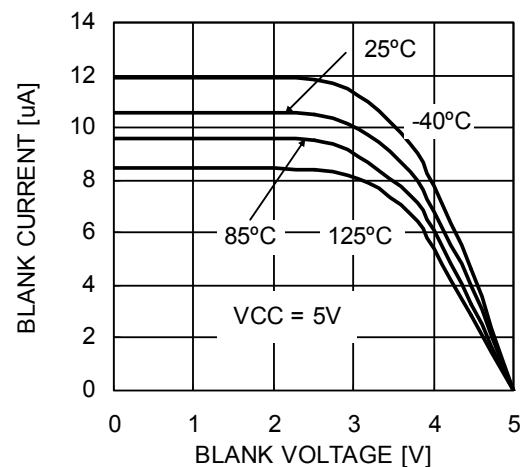
**BLANK and Output waveform**



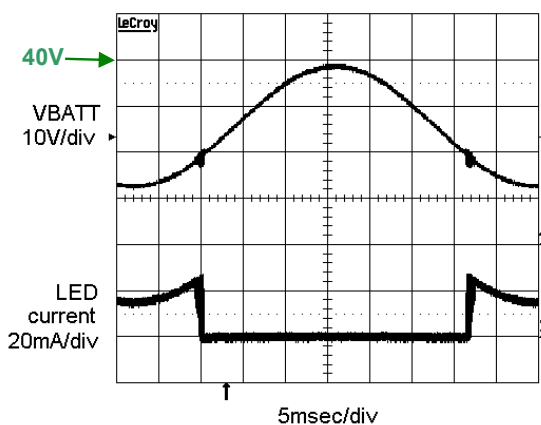
**XLAT pull-down Current vs. Input Voltage**



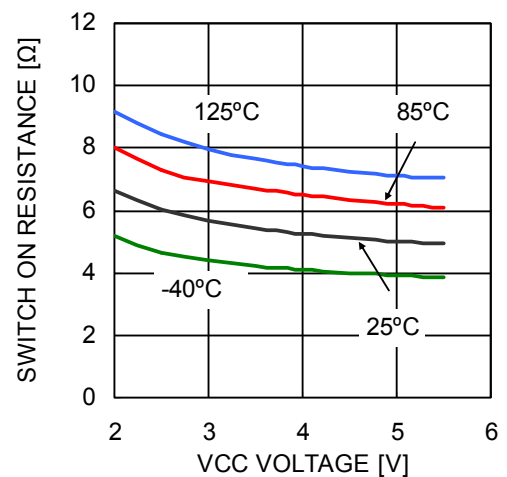
**BLANK pull-up Current vs. Input Voltage**



**VBATT Load Dump**



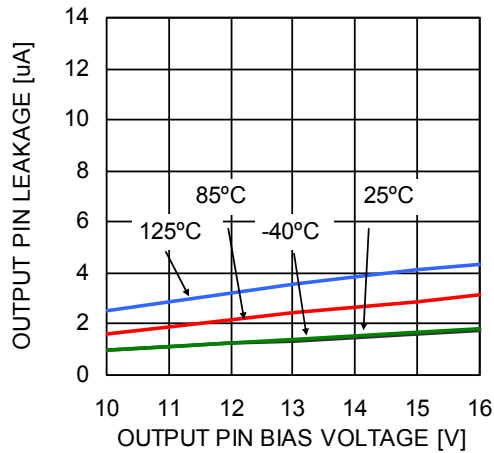
**Switch On-resistance vs. VCC**



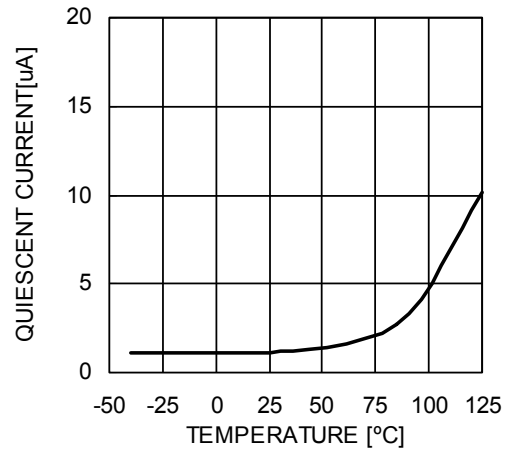
## TYPICAL CHARACTERISTICS

VCC = 5V, VBATT = 14V, T<sub>AMB</sub> = 25°C, unless otherwise specified.

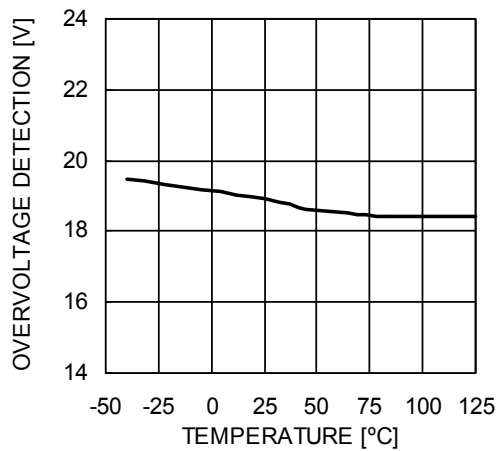
**Output Channel Leakage vs. Bias Voltage**



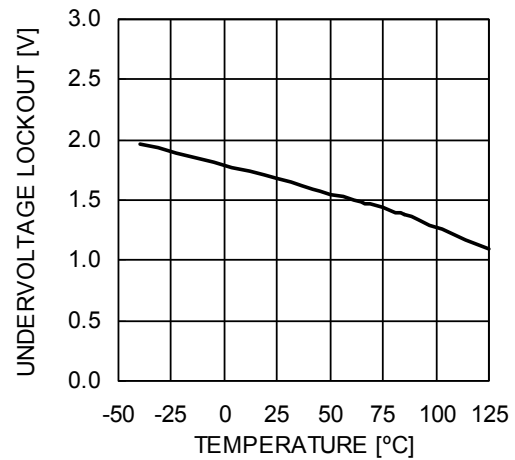
**Quiescent Current vs. Temperature**



**VBATT Overvoltage Detection vs. Temperature**



**VCC Undervoltage Lockout vs. Temperature**



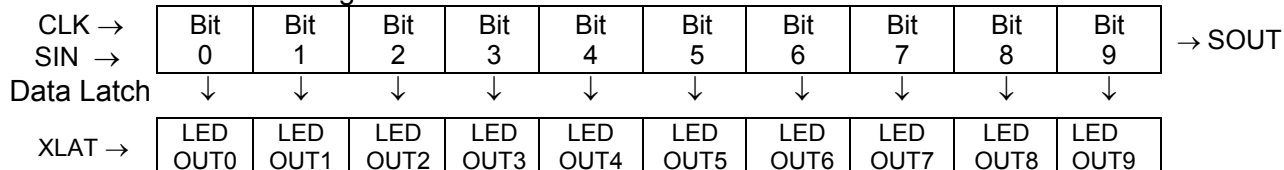
## FUNCTIONAL DESCRIPTION

The CAT310 implements a 10-bit serial-in shift register for storing the setting of the ten outputs. Serial input data SIN are clocked into the shift register on the rising edge of the clock. At the 10<sup>th</sup> clock pulse, the first data bit entered is outputted from the shift register to SOUT. The following clock pulses will output the following data bits onto SOUT. The output data pattern replicates the input data stream with a delay of ten clock pulses.

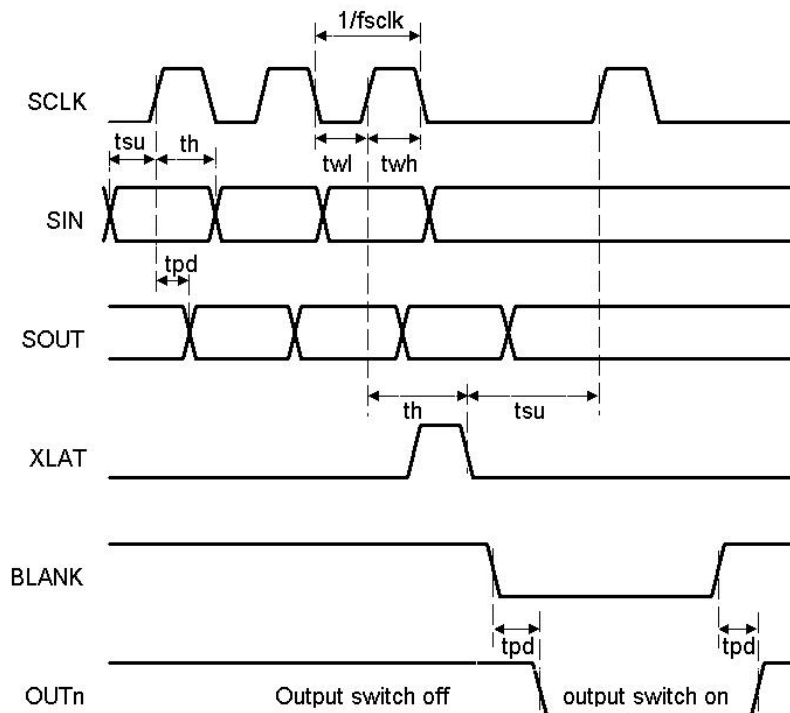
The 10-bit data pattern present in the shift register is stored in the 10-bit data latch when

the latch signal XLAT is logic high. When XLAT transitions to logic low, data are latched and stay unchanged for as long as XLAT remains low. The last serial input data corresponds to OUT0. The serial input data that was received 10 clock pulse ago is stored in OUT9. When the BLANK input is logic high, all the output switches are in the off state. If the BLANK input is low, the 10-bit data latches control the 10 output switches. A data bit value of zero keeps the switch off. A data bit value of one keeps the switch on.

### Serial to Parallel Shift Register



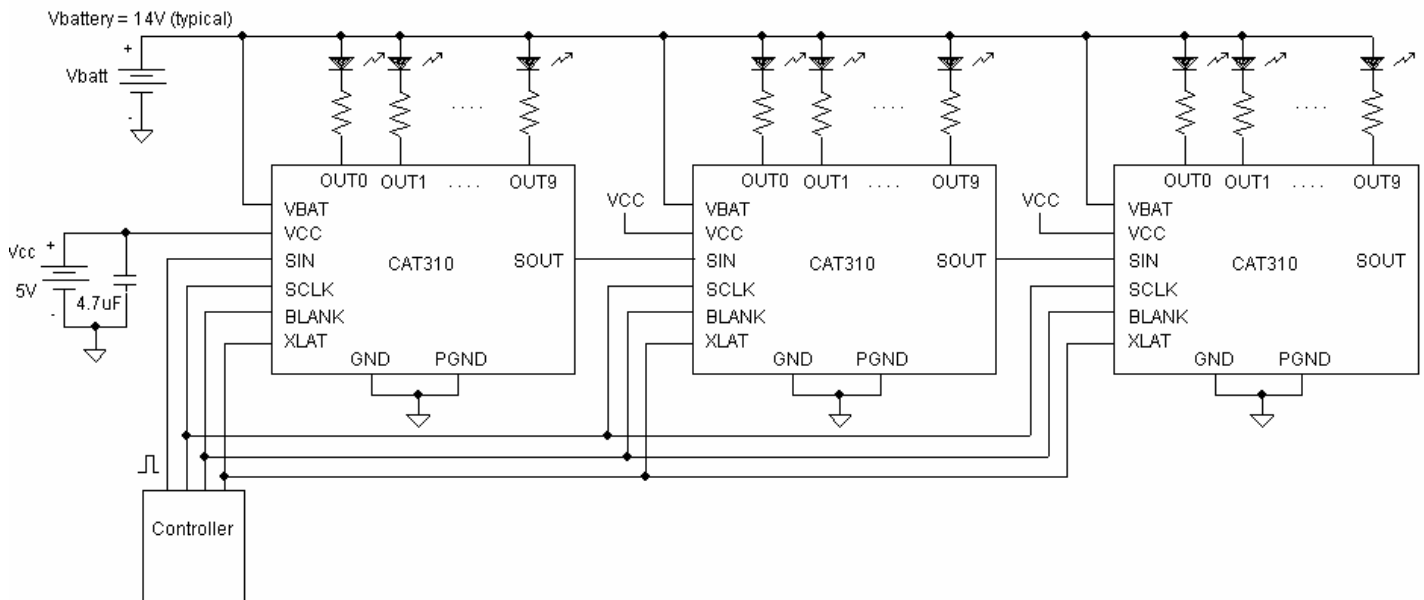
## TIMING DIAGRAM



## APPLICATION INFORMATION

For applications with a large number of LEDs, several CAT310 drivers can be daisy chained. The serial data output pin (SOUT) of the first driver is connected to the second driver data input pin (SIN). This sequence is repeated until the last driver is linked. All drivers are controlled by the same clock signal. Figure 1 shows an

example with three CAT310 devices driving a total of 30 LEDs in parallel. The controller transmits the serial data sequentially through the CAT310 devices. For N drivers connected in cascade, after  $10 \times N$  clock pulses, the data are latched with one single XLAT transition.

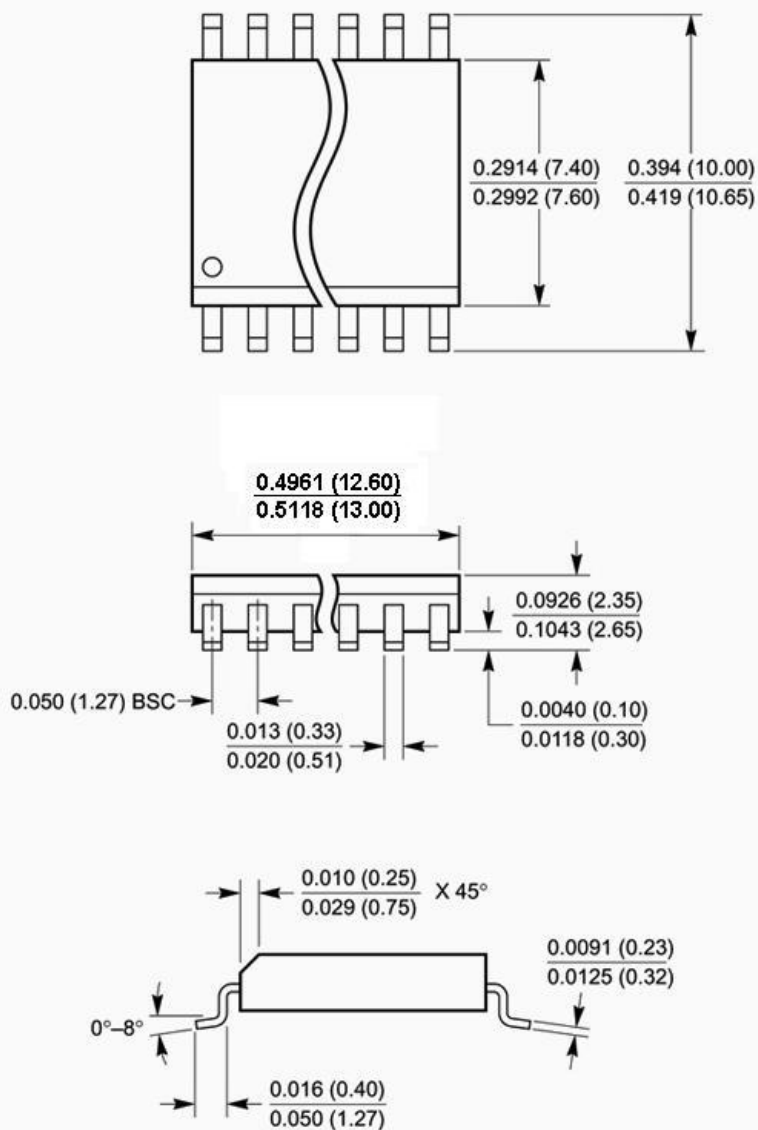


**Figure 1. Daisy Chain Application Diagram**



## PACKAGE DRAWING AND DIMENSIONS

### 20-LEAD 300 MIL WIDE SOIC (J)



#### Notes:

1. Complies with JEDEC publication 95 MS-013 dimensions; however, some dimensions may be more stringent.
2. All linear dimensions are in inches and parenthetically in millimeters.
3. Lead coplanarity is 0.004" (0.102mm) maximum.

**REVISION HISTORY**

| Date       | Revision | Reason        |
|------------|----------|---------------|
| 05/05/2005 | 00       | Initial issue |
|            |          |               |

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