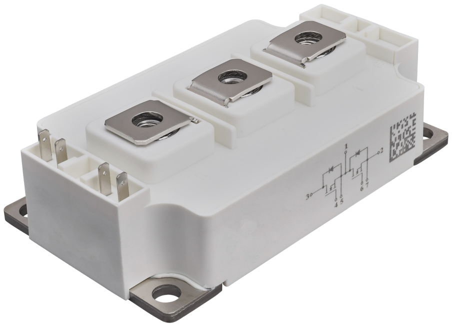
CAB530M12BM3, CAB530M12BM3T

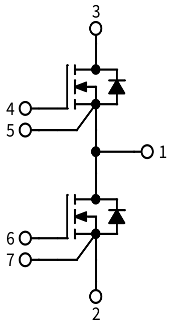
V_{DS}	1200 V
I_{DS}	530 A

1200 V, 530 A All-Silicon Carbide, Half-Bridge Module

Technical Features

- Industry Standard 62 mm Footprint
- Ultra Low Loss, High-Frequency Operation
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Copper Baseplate and Aluminum Nitride Insulator





Applications

- Railway & Traction
- EV Charging Infrastructure
- Industrial Automation & Testing
- High-Frequency Power Supplies
- Renewable Energy Systems & Grid-Tied Inverters
- Active Front Ends & AC InvertersUPS and SMPS

System Benefits

- Lightweight, Compact Form-Factor with 62 mm-Format Enables System Retrofit
- Increased System Efficiency due to Low Switching & Conduction Losses of SiC

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	T_C = 25 °C	
Gate-Source Voltage, Maximum Value	$V_{GS(max)}$	-10		+23		Transient	Note 1 Fig. 32
Gate-Source Voltage, Recommended	$V_{GS(op)}$		-4/+15			Static	
DC Continuous Drain Current	I_D		719			V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
			541			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	Notes 2, 3 Fig. 21
DC Source-Drain Current (Body Diode)	$I_{SD(BD)}$		442		A	V_{GS} = -4 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain-Source Current	I_{DM}		1060			t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_C = 25 °C	
Power Dissipation	P_D		2308		W	T_C = 25 °C, T_{VJ} ≤ 175 °C	Note 4 Fig. 21
Virtual Junction Temperature	$T_{VJ(op)}$	-40		150	°C	Operation	
				175		Intermittent with Reduced Life	

Note (1): Recommended turn-on gate voltage is 15 V with ±5 % regulation tolerance. Not for use in linear region.
Note (2): Current limit at T_C = 90 °C calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$
Note (3): Verified by design
Note (4): $P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 140 mA	
Zero Gate Voltage Drain Current	I_{DSS}		10	250	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}			2	µA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		2.67	3.55	mΩ	V_{GS} = 15 V, I_D = 530 A	Fig. 2 Fig. 3
			3.96		mΩ	V_{GS} = 15 V, I_D = 530 A, T_{VJ} = 150 °C	
Transconductance	g_{fs}		375		S	V_{DS} = 20 V, I_{DS} = 530 A	Fig. 4
			364		S	V_{DS} = 20 V, I_{DS} = 530 A, T_{VJ} = 150 °C	
Turn-On Switching Energy, T_J = 25 °C T_J = 125 °C T_J = 150 °C	E_{ON}		16.8 15.6 16.1		mJ	V_{DS} = 600 V, I_D = 530 A, V_{GS} = -4 V/+15 V, $R_{G(ext)}$ = 1.5 Ω, L = 13.6 µH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_J = 25 °C T_J = 125 °C T_J = 150 °C	E_{OFF}		15.5 14.9 14.9		mJ		
Internal Gate Resistance	$R_{G(int)}$		2.9		Ω	V_{AC} = 25 mV, f = 100 kHz	
Input Capacitance	C_{iss}		39.6		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.4		nF		
Reverse Transfer Capacitance	C_{rss}		84		pF		
Gate to Source Charge	Q_{GS}		384		nC	V_{DS} = 800 V, V_{GS} = -4 V/+15 V I_D = 530 A Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		462		nC		
Total Gate Charge	Q_G		1362		nC		
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.065		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Diode Forward Voltage	V_F		5.7		V	V_{GS} = -4 V, I_F = 530 A, T_{VJ} = 25 °C	Fig. 7
			5.0		V	V_{GS} = -4 V, I_F = 530 A, T_{VJ} = 150 °C	
Reverse Recovery Time	t_{rr}		44		ns	V_{GS} = -5 V, I_{SD} = 530 A, V_R = 800 V di_F/dt = 14.0 A/ns, T_{VJ} = 150 °C	Fig. 31
Reverse Recovery Charge	Q_{RR}		8.5		µC		
Peak Reverse Recovery Current	I_{RRM}		300		A		
Diode Energy T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{rr}		0.52 1.75 2.37		mJ	V_{DS} = 600 V, I_D = 530 A, V_{GS} = -5 V/20 V, $R_{G(ext)}$ = 1.5 Ω, L = 13.6 µH	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1 (High-Side)	R_{1-3}		0.42		mΩ	T_C = 25 °C, I_{SD} = 530 A, Note 5
			0.60			T_C = 150 °C, I_{SD} = 530 A, Note 5
Package Resistance, M2 (Low-Side)	R_{1-2}		0.28			T_C = 25 °C, I_{SD} = 530 A, Note 5
			0.40			T_C = 150 °C, I_{SD} = 530 A, Note 5
Stray Inductance	L_{Stray}		11.1		nH	Between Terminals 1 and 3
Case Temperature	T_C	-40		125	°C	
Weight	W		300		g	
Mounting Torque	M_S	4	5	5.5	N-m	Baseplate, M6-1.0 Bolts
		4	5	5.5		Power Terminals, M6-1.0 Bolts
Case Isolation Voltage	V_{isol}	5			kV	AC, 50 Hz, 1 min
Clearance Distance		9			mm	Terminal to Terminal
		30				Terminal to Baseplate
Creepage Distance		30				Terminal to Terminal
		40				Terminal to Baseplate

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Typical Performance

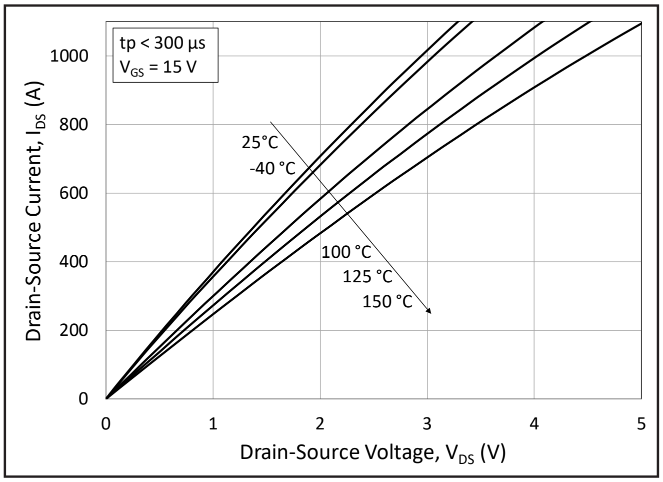


Figure 1. Output Characteristics for Various Junction Temperatures

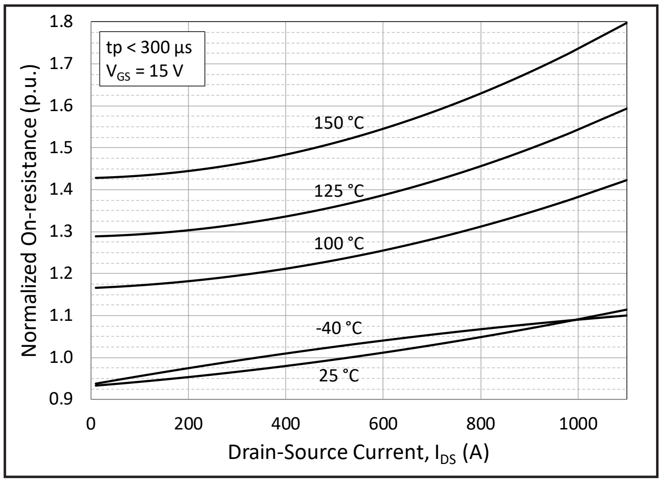


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

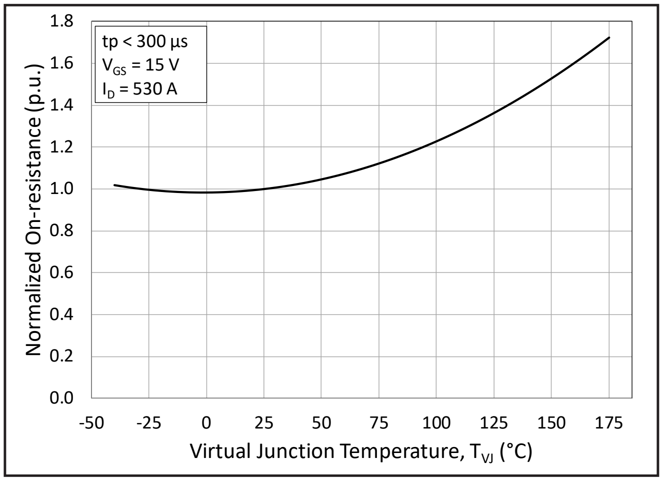


Figure 3. Normalized On-State Resistance vs. Junction Temperature

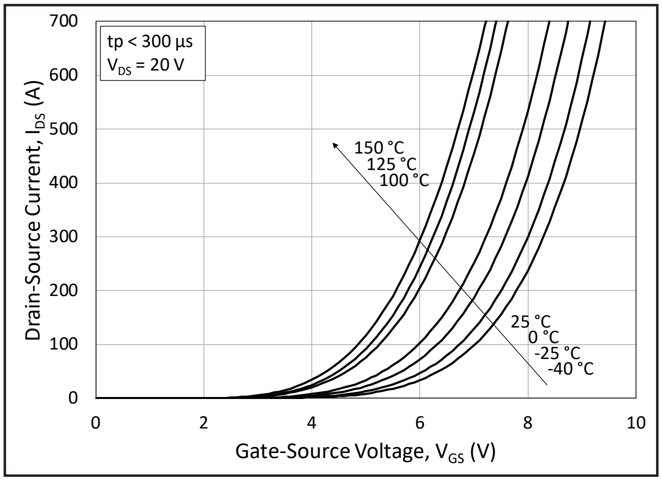


Figure 4. Transfer Characteristic for Various Junction Temperatures

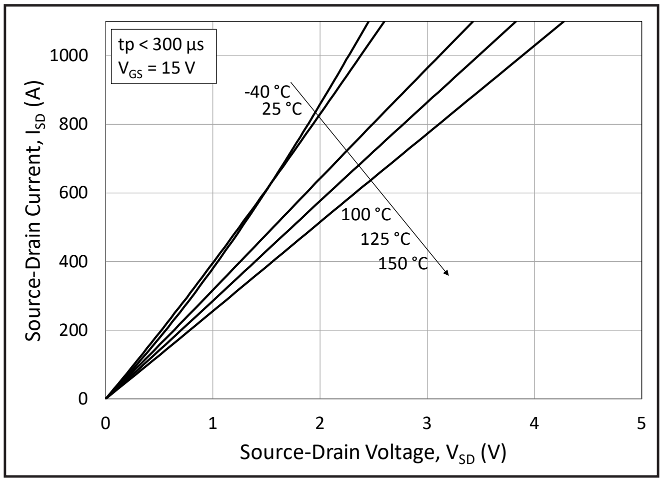


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

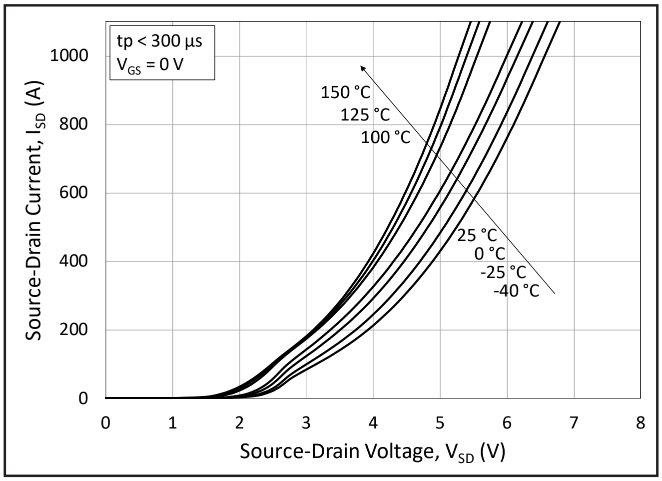


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Diode)

Typical Performance

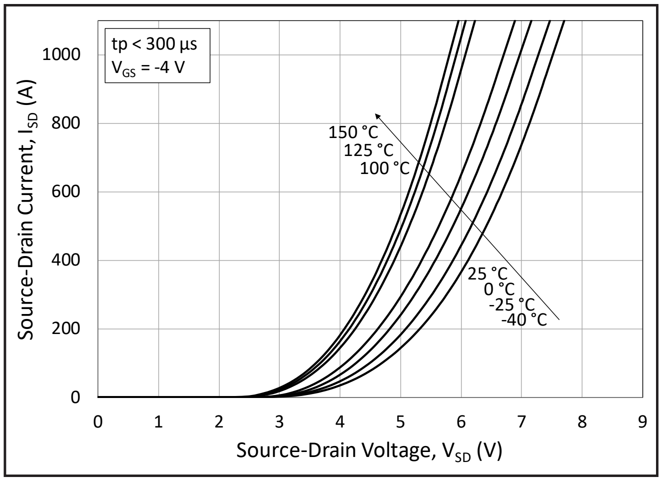


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -4 V (Diode)

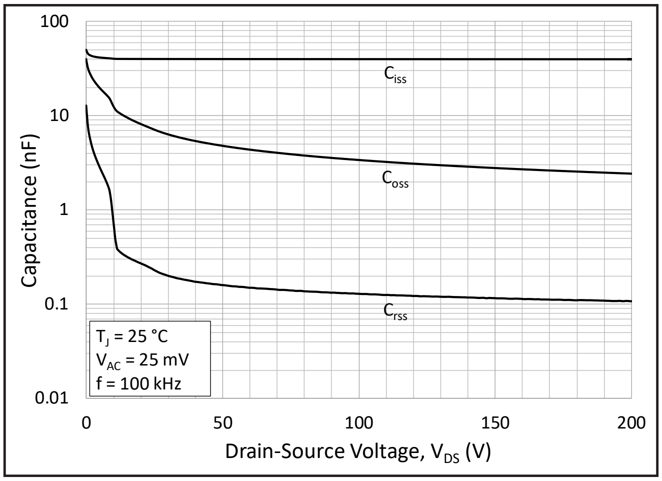


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 V - 200 V)

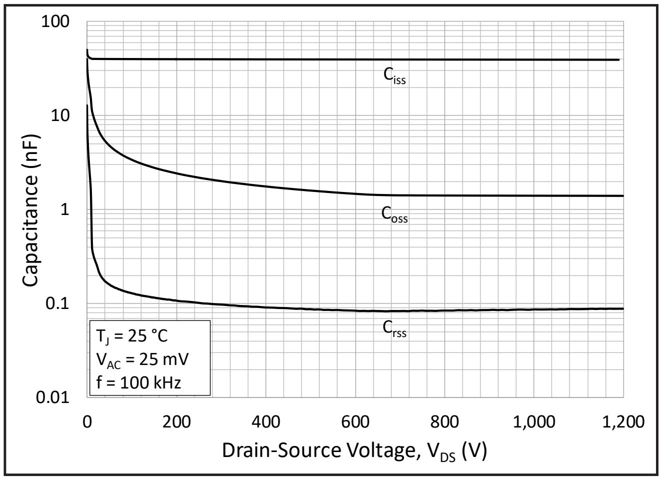


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 V - 1200 V)

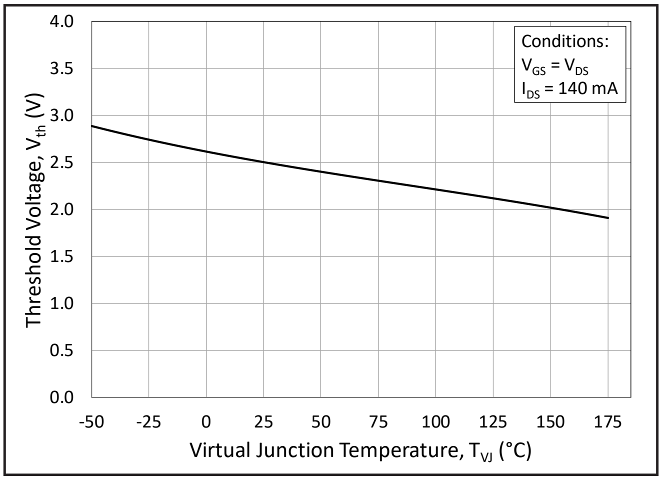


Figure 10. Threshold Voltage vs. Junction Temperature

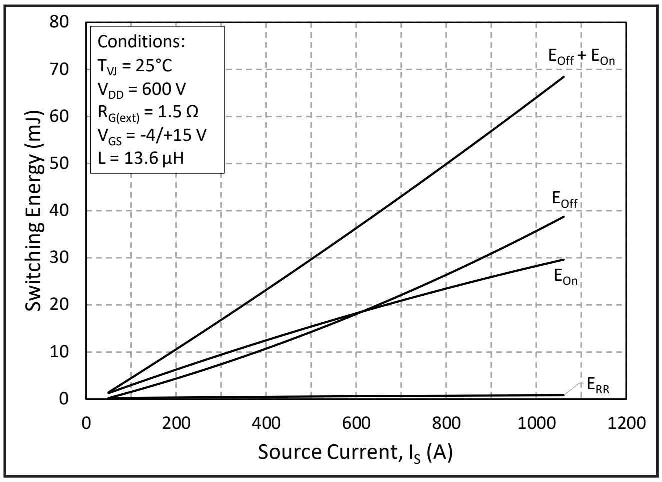


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

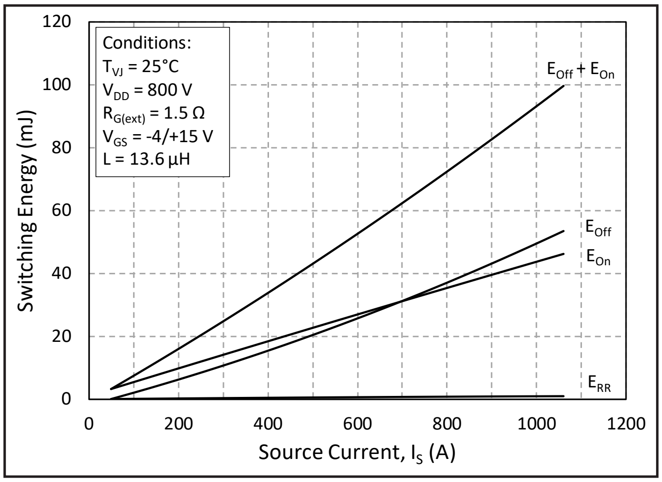


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

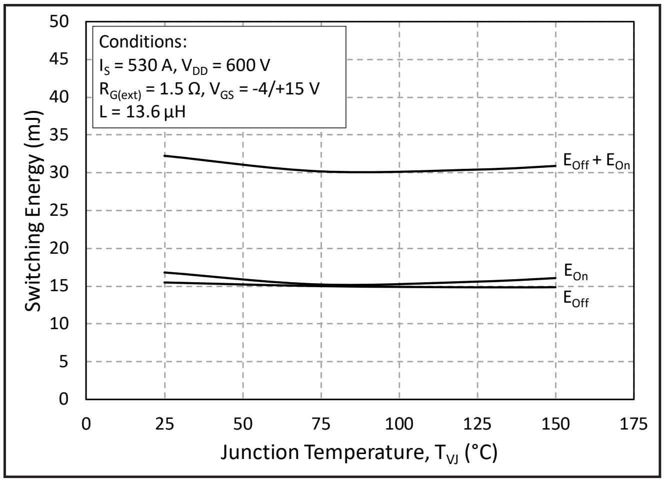


Figure 13. MOSFET Switching Energy vs. Junction Temperature

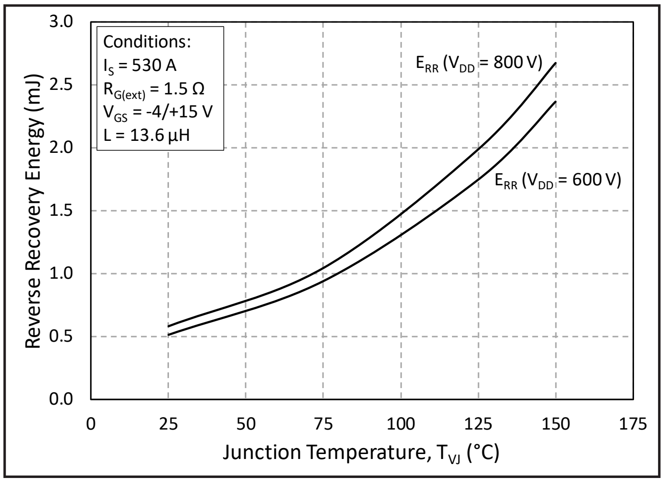


Figure 14. Reverse Recovery Energy vs. Junction Temperature

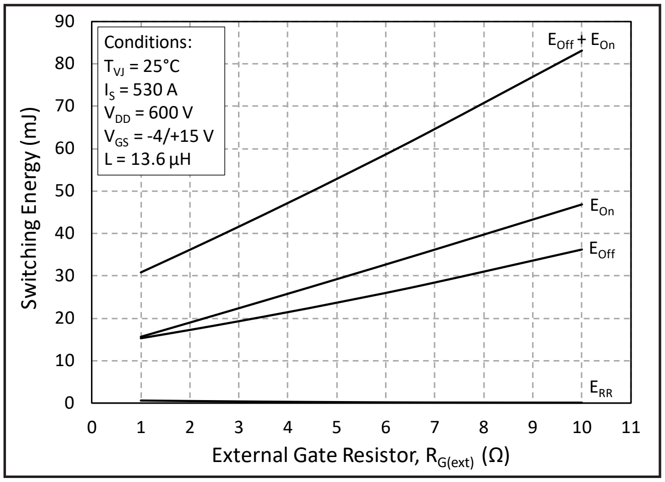


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

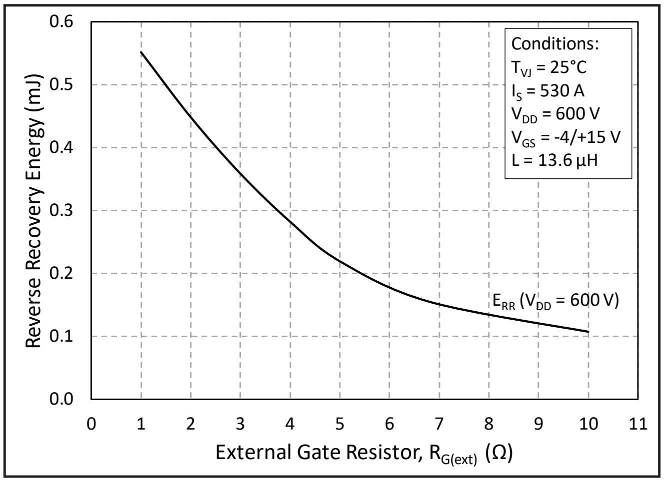


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

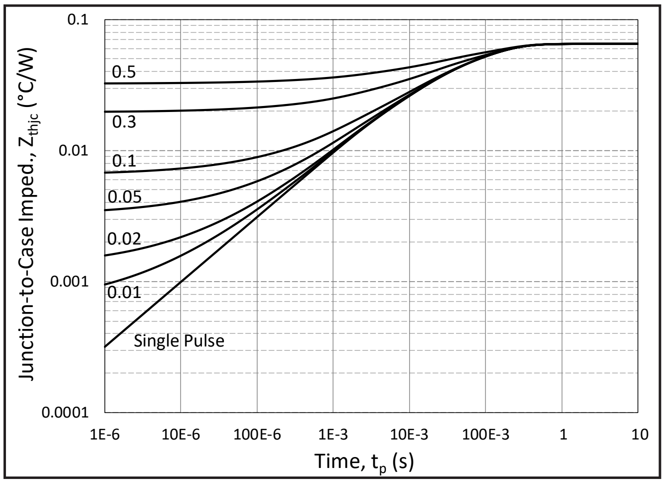


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

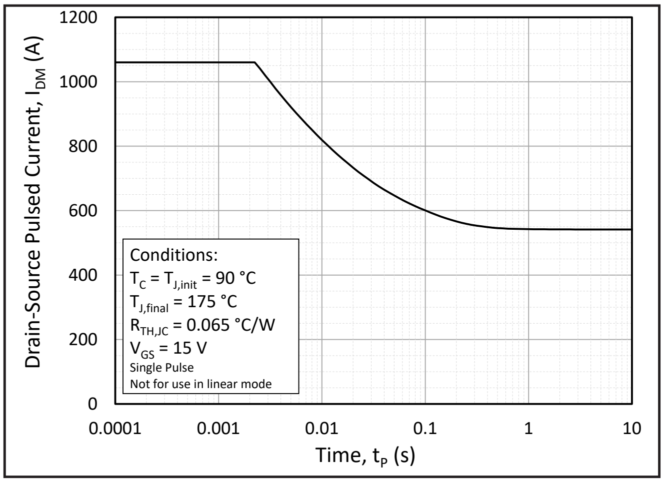


Figure 18. Pulsed Current Safe Operating Area

Typical Performance

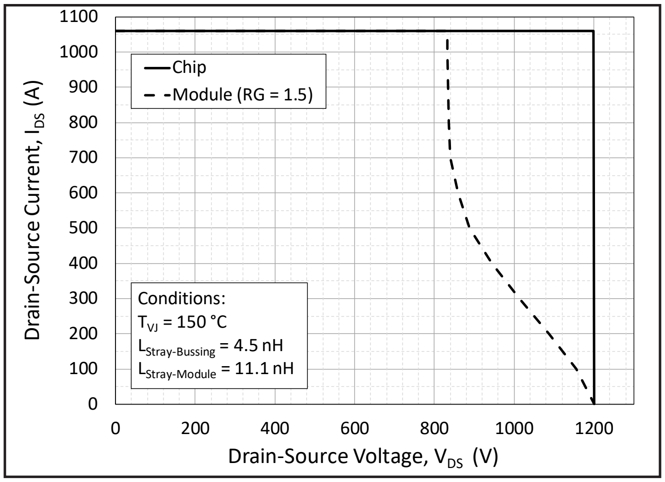


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

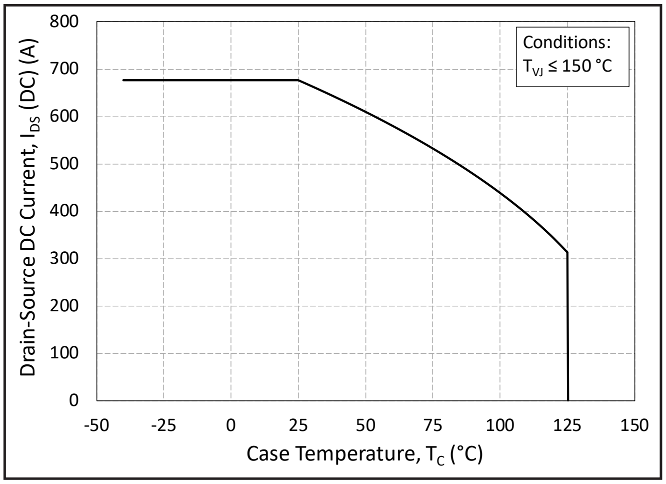


Figure 20. Continuous Drain Current Derating vs. Case Temperature

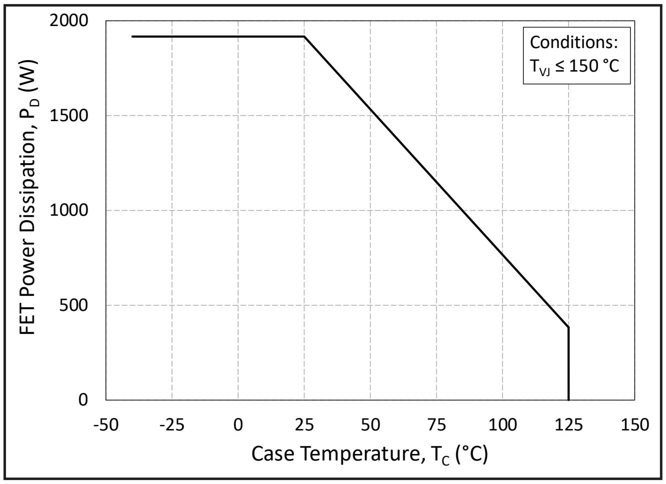


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

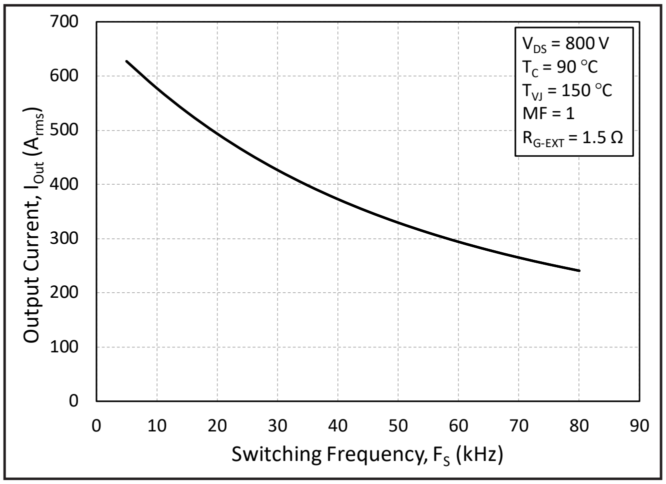


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

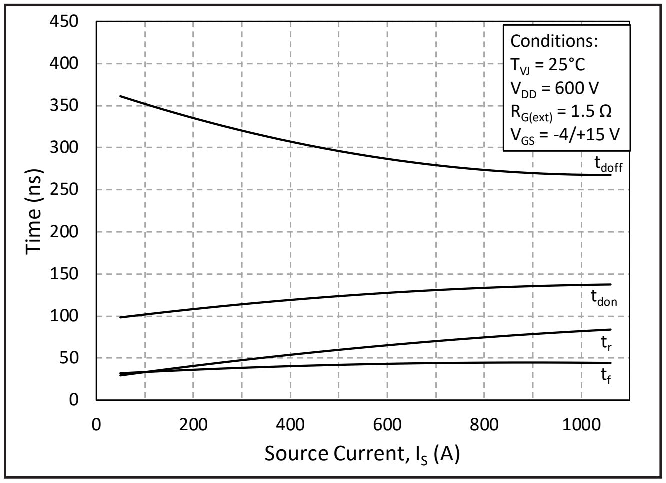


Figure 23. Timing vs. Source Current

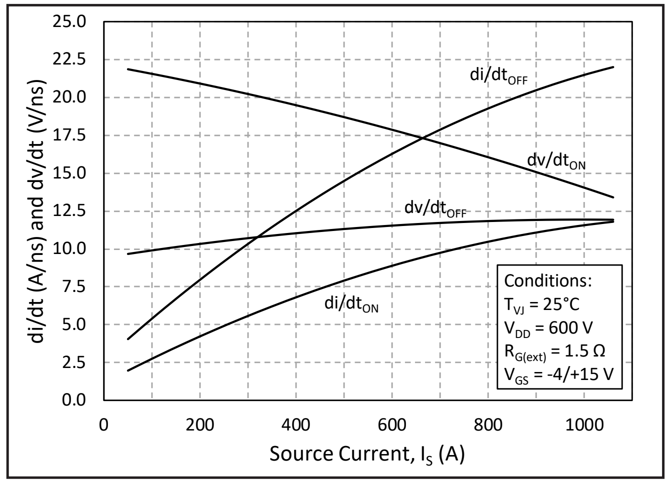


Figure 24. dv/dt and di/dt vs. Source Current

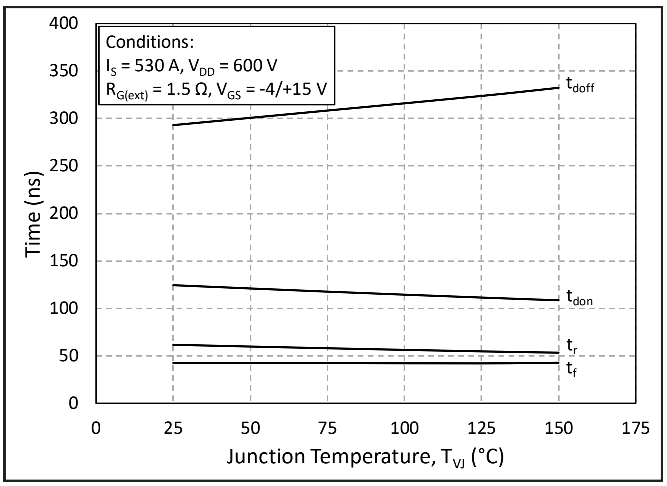


Figure 25. Timing vs. Junction Temperature

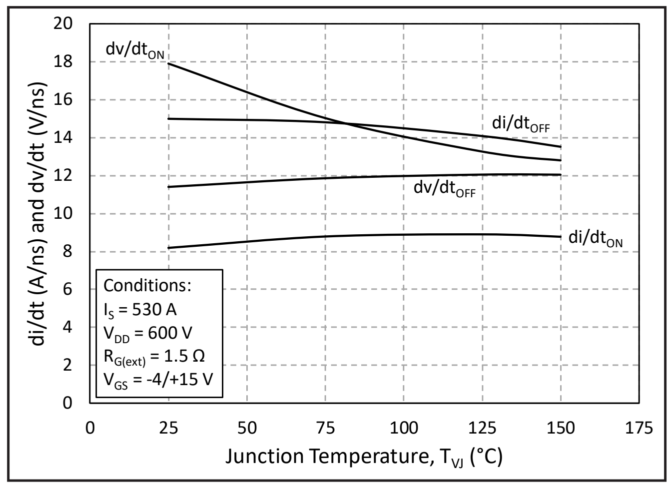


Figure 26. dv/dt and di/dt vs. Junction Temperature

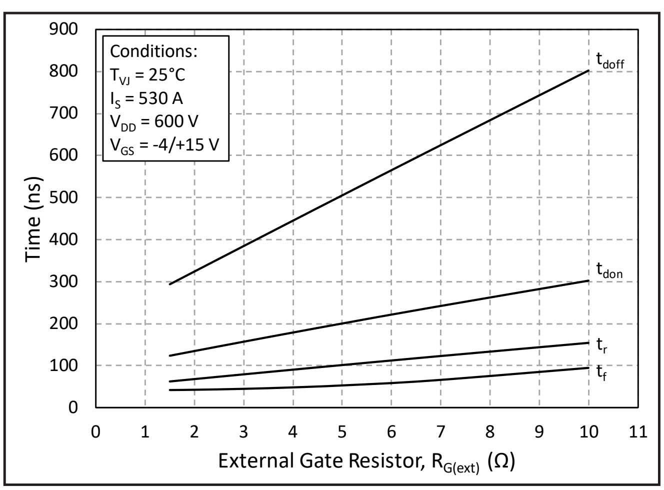


Figure 27. Timing vs. External Gate Resistance

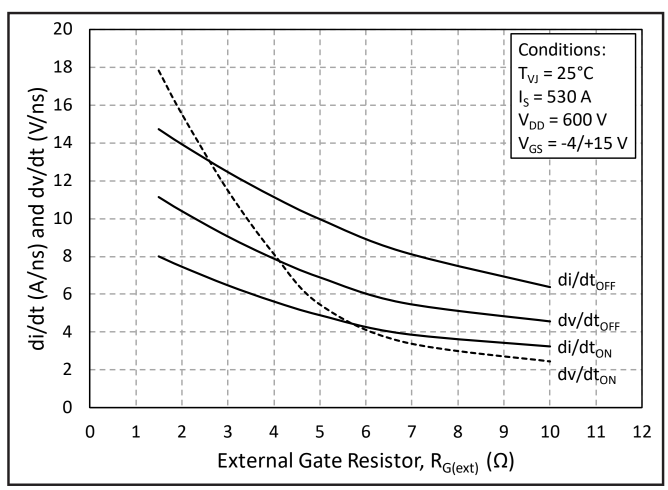


Figure 28. dv/dt and di/dt vs. External Gate Resistance

Definitions

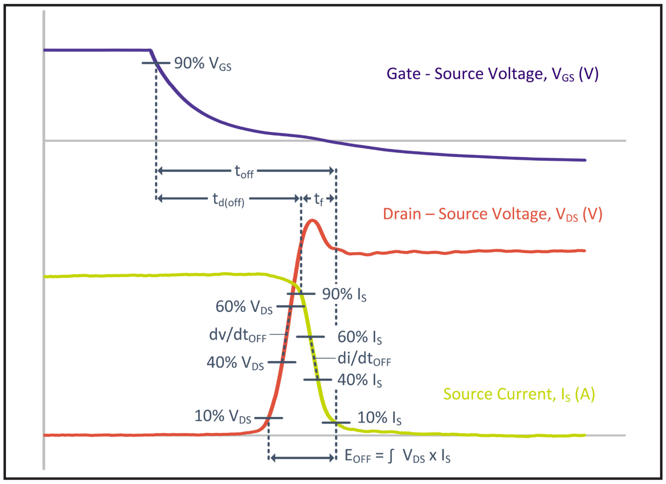


Figure 29. Turn-Off Transient Definitions

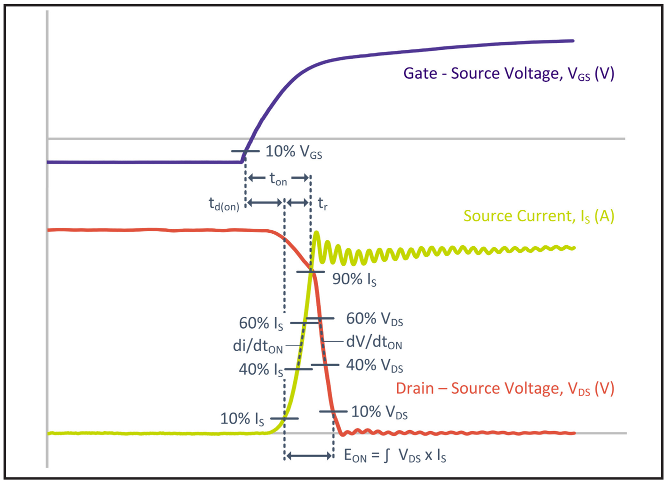


Figure 30. Turn-On Transient Definitions

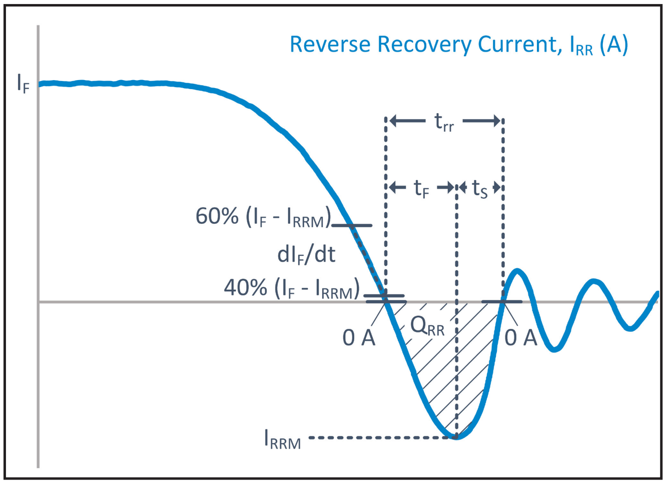


Figure 31. Reverse Recovery Definitions

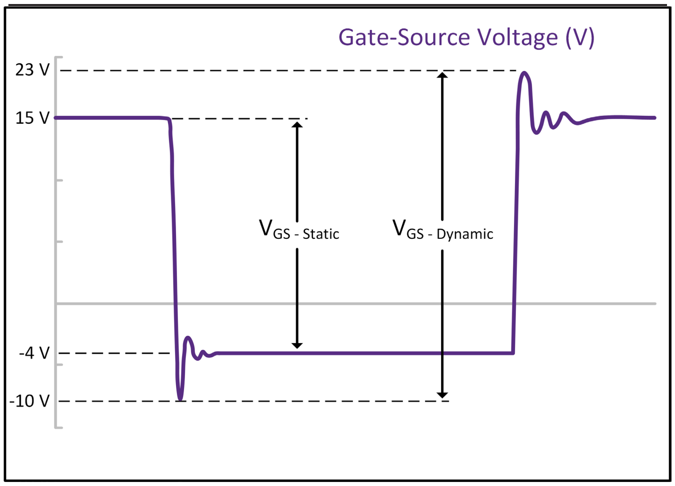
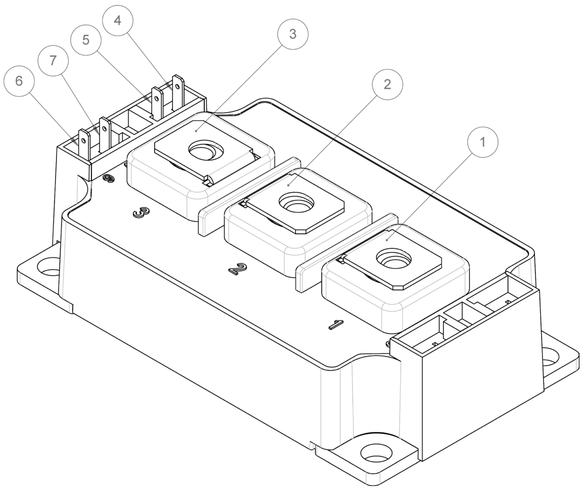
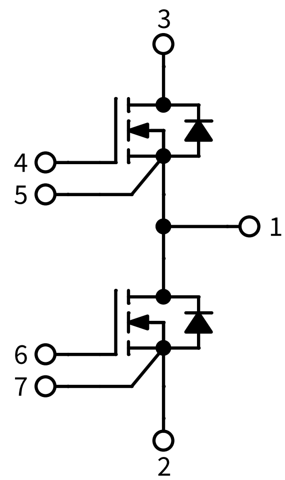


Figure 32. V_{GS} Transient Definitions

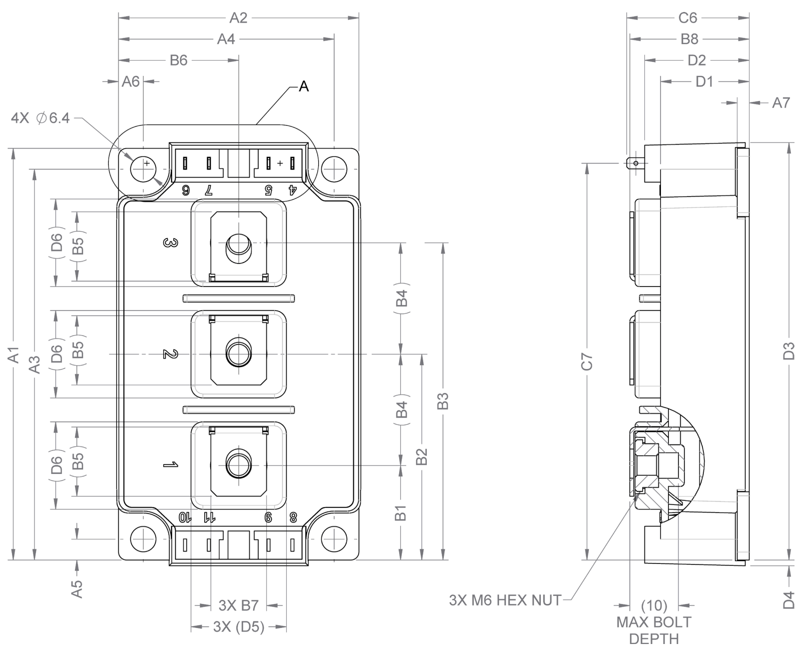
Schematic and Pin Out



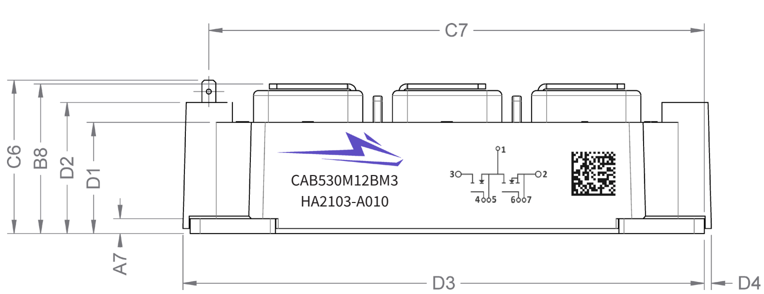


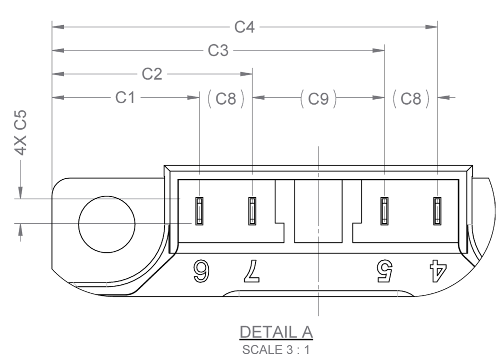
Note 2: The anti-parallel diodes shown in the schematic are MOSFET body diodes.

Package Dimensions (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	103.5	±0.30
A2	60.44	±0.30
A3	98.25	±0.30
A4	54.22	±0.30
A5	5.25	±0.30
A6	6.22	±0.30
A7	3	±0.30
B1	23.75	±0.40
B2	51.75	±0.40
B3	79.75	±0.40
B4	(28)	REF.
B5	(17.43)	REF.
B6	30.23	±0.40
B7	(14)	REF.
B8	30.03	±0.40
C1	16.73	±0.40
C2	22.73	±0.40
C3	37.73	±0.40
C4	43.73	±0.40
C5	2.8	±0.40
C6	30.8	±0.50
C7	99.75	±0.40
C8	(6)	REF.
C9	(15)	REF.
D1	22.3	±0.30
D2	26.3	±0.30
D3	104.95	±0.30
D4	1.45	±0.40
D5	(24)	REF.
D6	(22)	REF.





Product Ordering Code

Part Number	Description
CAB530M12BM3	Without Pre-Applied Phase Change Thermal Interface Material
CAB530M12BM3T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Simulation Tools & Support

- All LTSpice Models
- All PLECS Models
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Compatible Evaluation Hardware

- CGD1200HB2P-BM3: Dual Channel Differential Isolated Half Bridge Gate Driver Board
- KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 and BM3 Module
- CGD1700HB2P-BM3: Evaluation Gate Driver Tool Optimized for the 1700 V BM3 Power Modules
- KIT-CRD-CIL17N-BM: Dynamic Characterization Evaluation Tool Optimized for 1700 V BM Power Modules
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide
- PRD-06379: Environmental Considerations for Power Electronics
- PRD-08710: Measuring Stray Inductance in Power Electronic Systems
- PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility
- PRD-08376: Thermal Characterization Methods and Applications
- PRD-06933: Capacitance Ratio and Parasitic Turn-On

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