

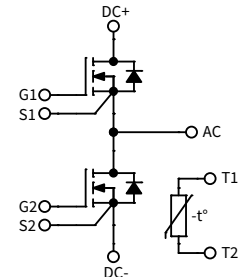
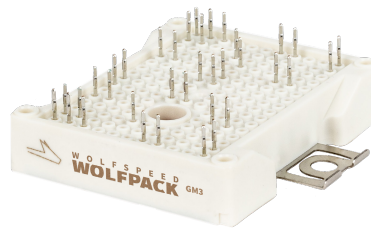
# CAB011A12GM3, CAB011A12GM3T

1200 V, 11 mΩ, Silicon Carbide, Half-Bridge Module

$V_{DS}$	1200 V
$R_{DS(on)}$	11 mΩ

## Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation
- Aluminum Nitride Ceramic Substrate
- Optional Pre-Applied Thermal Interface Material



## Typical Applications

- DC-DC Converters
- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation

## System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

## Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	$V_{DS}$			1200	V		
Maximum Gate-Source Voltage	$V_{GS(max)}$	-10		+23		Transient	Fig. 33
Operational Gate-Source Voltage	$V_{GS(op)}$		-4/15			Static	Note 1
DC Continuous Drain Current ( $T_{VJ} \leq 150^\circ\text{C}$ )	$I_D$		141		A	$V_{GS} = 15\text{ V}, T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 150^\circ\text{C}$	Notes 2,3,4 Fig. 20
DC Continuous Drain Current ( $T_{VJ} \leq 175^\circ\text{C}$ )			149			$V_{GS} = 15\text{ V}, T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 175^\circ\text{C}$	
DC Source-Drain Current (Body Diode)	$I_{SD\ BD}$		97			$V_{GS} = -4\text{ V}, T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 175^\circ\text{C}$	
Pulsed Drain Current	$I_D\ (pulsed)$			300		$t_{Pmax}$ limited by $T_{VJmax}$ $V_{GS} = 15\text{ V}, T_{HS} = 75^\circ\text{C}$	
Power Dissipation	$P_D$		470		W	$T_{HS} = 75^\circ\text{C}, T_{VJ} \leq 175^\circ\text{C}$	Note 5 Fig. 21
Virtual Junction Temperature	$T_{VJ(op)}$	-40		150	$^\circ\text{C}$	Operation	
		-40		175		Intermittent with Reduced Life	

Note (1): Recommended turn-on gate voltage is 15 V with  $\pm 5\%$  regulation tolerance. Not for use in linear region.

Note (2): DC current limits at  $T_{HS} = 75^\circ\text{C}$  calculated by  $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$ .

Note (3): See Figure 22 for implementable AC current.

Note (4): Verified by design.

Note (5):  $P_D = (T_{VJ} - T_{HS})/R_{TH(JH,typ)}$ .

**MOSFET Characteristics (Per Position) ( $T_{VJ} = 25^\circ\text{C}$  unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200				$V_{GS} = 0\text{ V}, T_{VJ} = -40^\circ\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.9	V	$V_{DS} = V_{GS}, I_D = 34\text{ mA}$	
			2.1			$V_{DS} = V_{GS}, I_D = 34\text{ mA}, T_{VJ} = 150^\circ\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$		3	300	$\mu\text{A}$	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	$I_{GSS}$		0.03	0.75		$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		10.7	14.8	$\text{m}\Omega$	$V_{GS} = 15\text{ V}, I_D = 150\text{ A}$	Fig. 2 Fig. 3
			17.1			$V_{GS} = 15\text{ V}, I_D = 150\text{ A}, T_{VJ} = 150^\circ\text{C}$	
			19.2			$V_{GS} = 15\text{ V}, I_D = 150\text{ A}, T_{VJ} = 175^\circ\text{C}$	
Transconductance	$g_{fs}$		104		S	$V_{DS} = 20\text{ V}, I_D = 150\text{ A}$	Fig. 4
			96			$V_{DS} = 20\text{ V}, I_D = 150\text{ A}, T_{VJ} = 150^\circ\text{C}$	
Turn-On Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$	$E_{On}$		2.8 3.3 3.5		$\text{mJ}$	$V_{DD} = 600\text{ V},$ $I_D = 150\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V},$ $R_{G(EXT)} = 1.5\ \Omega,$ $L = 22.7\ \mu\text{H}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$	$E_{Off}$		0.7 0.6 0.7				
Internal Gate Resistance	$R_{G(int)}$		1.57		$\Omega$	$f = 100\text{ kHz}, V_{AC} = 25\text{ mV}$	
Input Capacitance	$C_{iss}$		11		$\text{nF}$	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V},$ $V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	Fig. 9
Output Capacitance	$C_{oss}$		0.4				
Reverse Transfer Capacitance	$C_{rss}$		24		$\text{pF}$		
Gate to Source Charge	$Q_{GS}$		120		$\text{nC}$	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V},$ $I_D = 40\text{ A},$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	$Q_{GD}$		102				
Total Gate Charge	$Q_G$		354				
FET Thermal Resistance, Junction to Heatsink	$R_{th\ JHS}$		0.213		$^\circ\text{C}/\text{W}$	Measured with Pre-Applied TIM	Fig. 17

**Diode Characteristics (Per Position) ( $T_{VJ} = 25^\circ\text{C}$  unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	$V_{SD}$		5.3		V	$V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}$	Fig. 7
			4.8			$V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}, T_{VJ} = 150^\circ\text{C}$	
Reverse Recovery Time	$t_{RR}$		29		ns	$V_{GS} = -4\text{ V}, I_{SD} = 150\text{ A}, V_R = 600\text{ V},$ $di/dt = 13.5\text{ A/ns}, T_{VJ} = 150^\circ\text{C}$	Fig. 32
Reverse Recovery Charge	$Q_{RR}$		3.5		$\mu\text{C}$		
Peak Reverse Recovery Current	$I_{RRM}$		189		A		
Reverse Recovery Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$	$E_{RR}$		0.11 0.51 0.67		$\text{mJ}$	$V_{DD} = 600\text{ V}, I_D = 150\text{ A},$ $V_{GS} = -4\text{ V}/15\text{ V}, R_{G(EXT)} = 1.5\ \Omega,$ $L = 22.7\ \mu\text{H}$	Fig. 14



Module Physical Characteristics

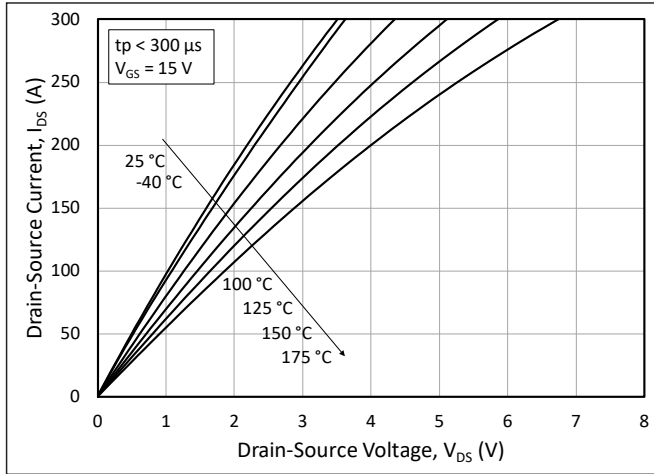
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R <sub>HS</sub>		0.28		mΩ	T <sub>HS</sub> = 125°C, I <sub>D</sub> = 75 A, Note 6
Package Resistance, M2 (Low-Side)	R <sub>LS</sub>		0.29			T <sub>HS</sub> = 125°C, I <sub>D</sub> = 75 A, Note 6
Stray Inductance	L <sub>Stray</sub>		18.3		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T <sub>C</sub>	-40		125	°C	
Mounting Torque	M <sub>S</sub>		2.0	2.3	N-m	M4 bolts
Weight	W		39		g	
Case Isolation Voltage	V <sub>isol</sub>	3			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	200				
Clearance Distance			5.0		mm	Terminal to Terminal
			10.0			Terminal to Heatsink
Creepage Distance			6.3			Terminal to Terminal
			11.5			Terminal to Heatsink

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET R<sub>DS(on)</sub> + Switch Position Package Resistance

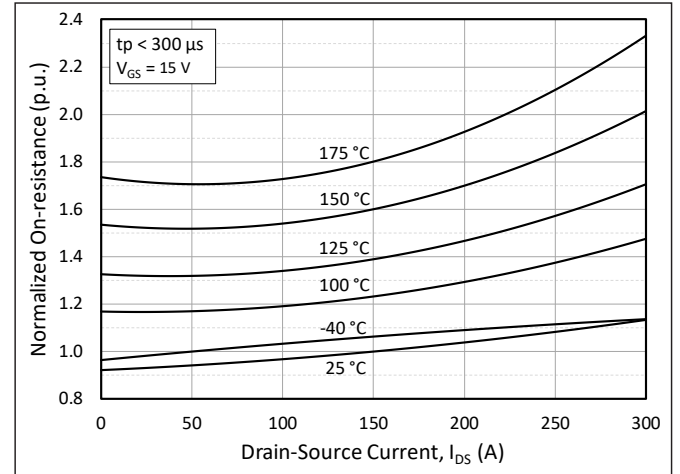
NTC Thermistor Characterization

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rated Resistance	R <sub>NTC</sub>		5.0		kΩ	T <sub>NTC</sub> = 25°C
Resistance Tolerance at 25 °C	ΔR/R	-5		5	%	
Beta Value (T <sub>2</sub> = 50 °C)	β <sub>25/50</sub>		3380		K	
Beta Value (T <sub>2</sub> = 80 °C)	β <sub>25/80</sub>		3468		K	
Beta Value (T <sub>2</sub> = 100 °C)	β <sub>25/100</sub>		3523		K	
Power Dissipation	P <sub>Max</sub>			10	mW	T <sub>NTC</sub> = 25°C

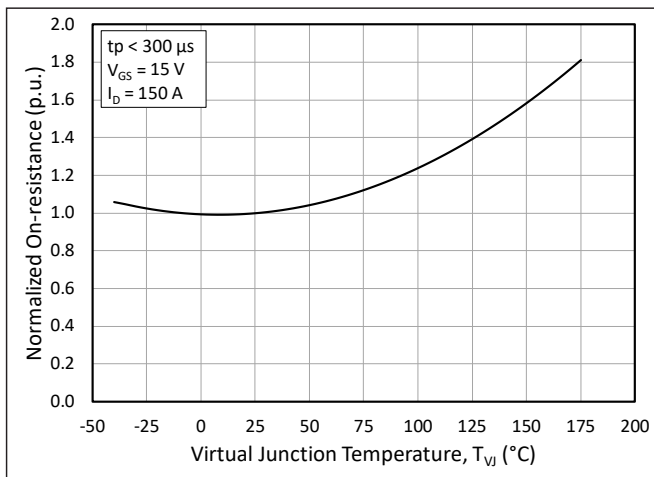
## Typical Performance



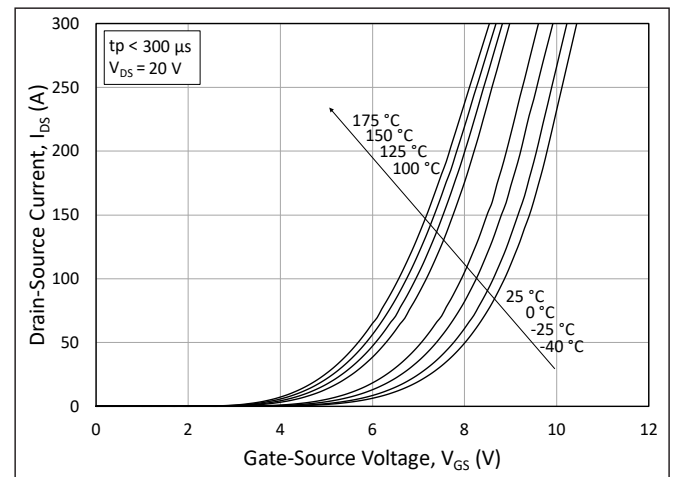
**Figure 1.** Output Characteristics for Various Junction Temperatures



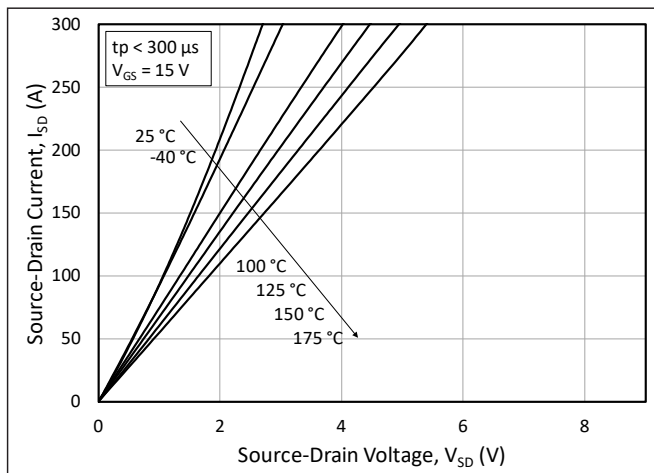
**Figure 2.** Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures



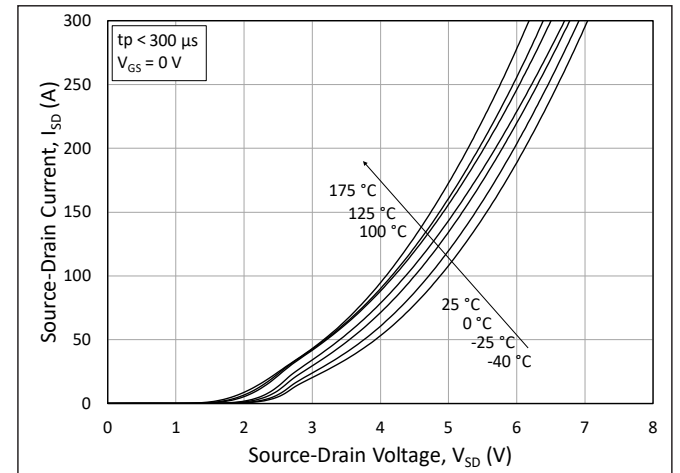
**Figure 3.** Normalized On-State Resistance vs. Junction Temperature



**Figure 4.** Transfer Characteristic for Various Junction Temperatures

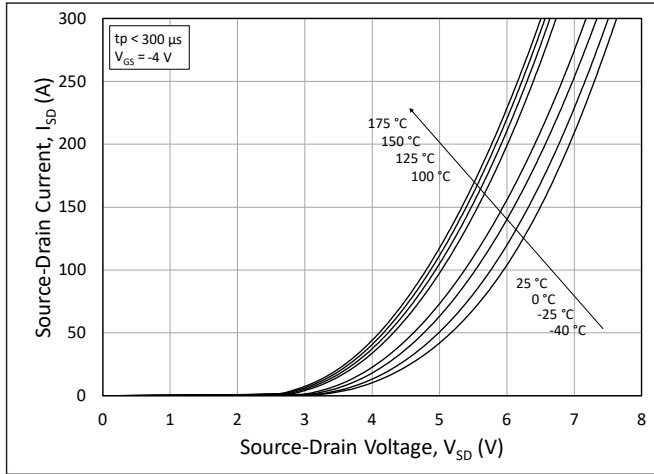


**Figure 5.** 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 15$  V

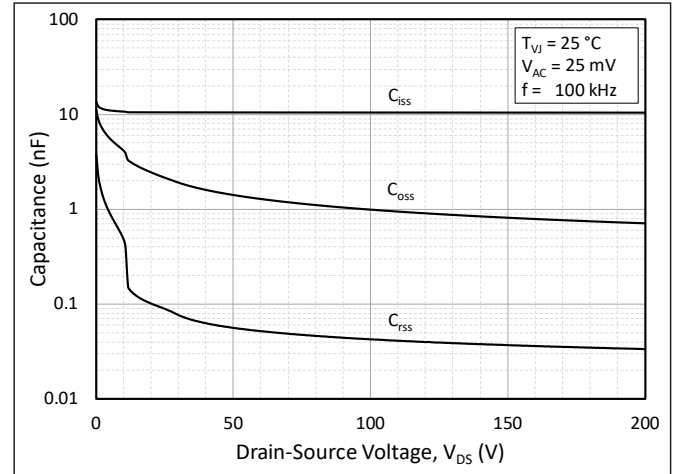


**Figure 6.** 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = 0$  V

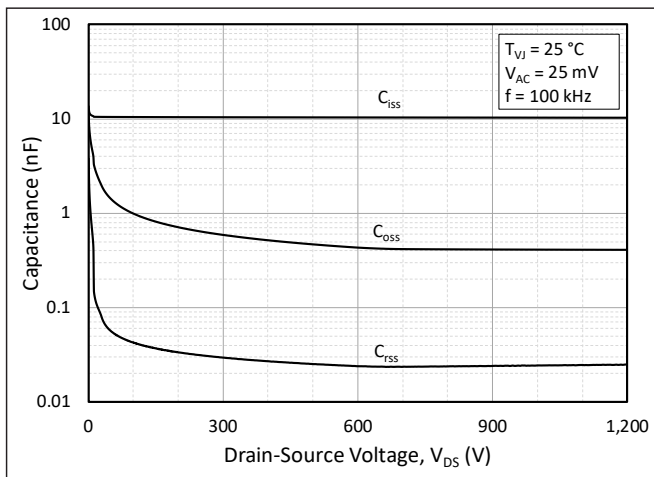
## Typical Performance



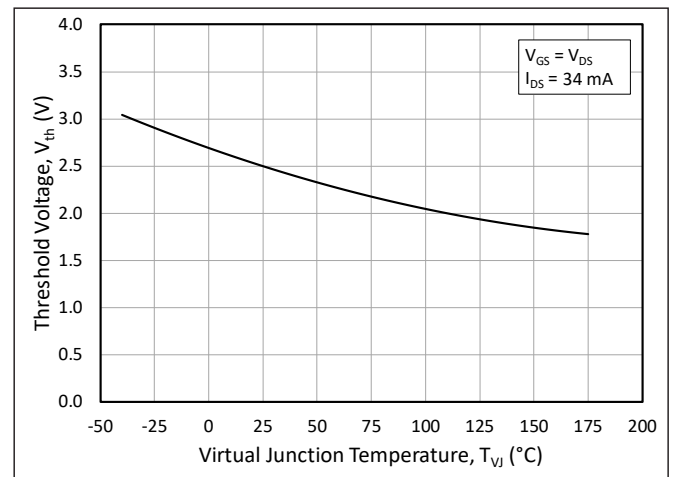
**Figure 7.** 3<sup>rd</sup> Quadrant Characteristic vs. Junction Temperatures at  $V_{GS} = -4$  V (Body Diode)



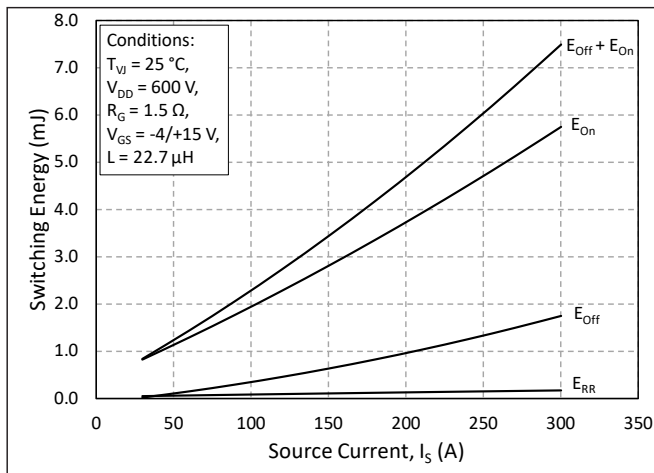
**Figure 8.** Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)



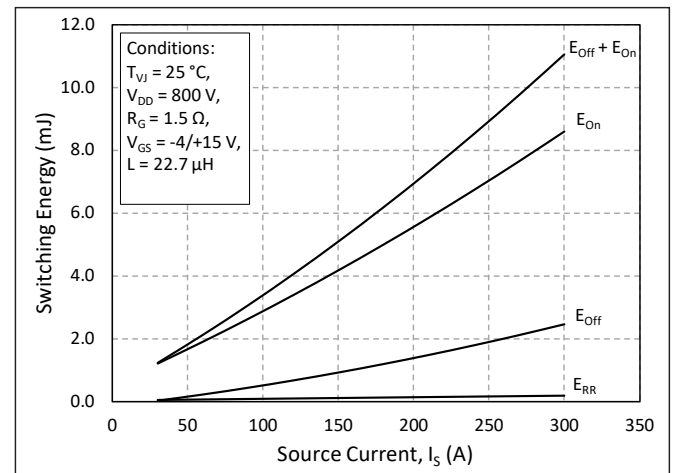
**Figure 9.** Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)



**Figure 10.** Threshold Voltage vs. Junction Temperature

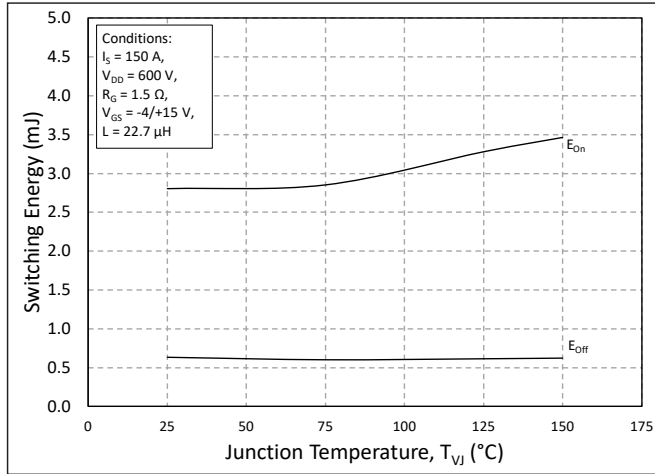


**Figure 11.** Switching Energy vs. Drain Current ( $V_{DD} = 600$  V)

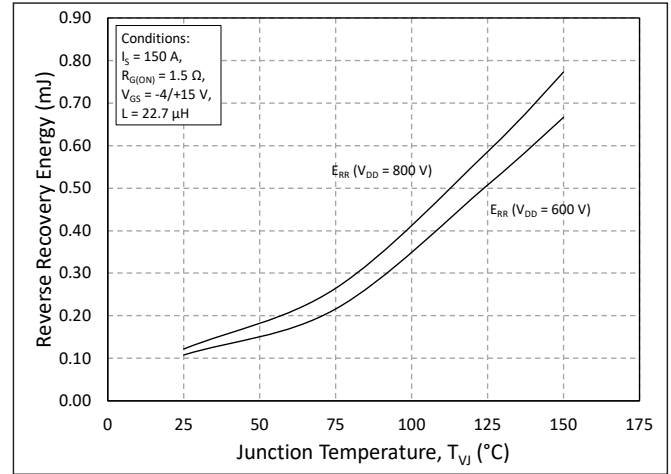


**Figure 12.** Switching Energy vs. Drain Current ( $V_{DD} = 800$  V)

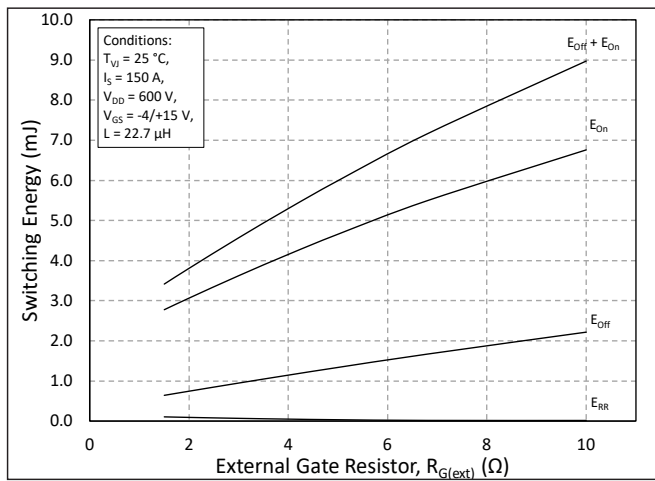
## Typical Performance



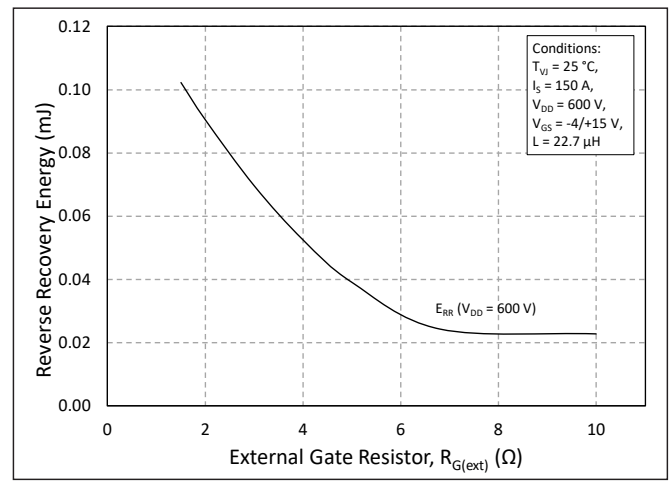
**Figure 13.** MOSFET Switching Energy vs. Junction Temperature



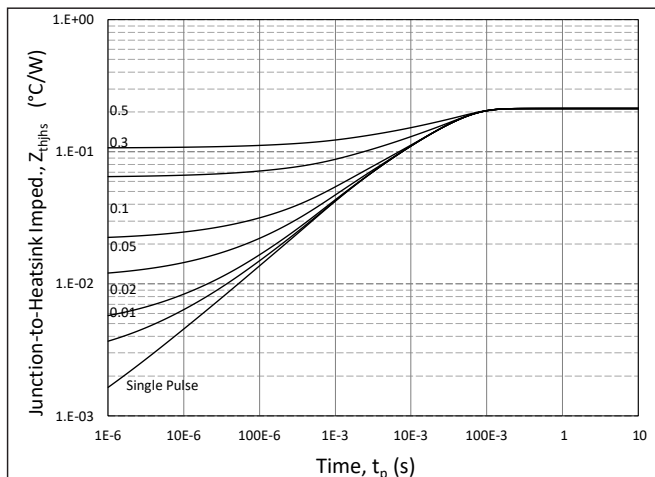
**Figure 14.** Reverse Recovery Energy vs. Junction Temperature



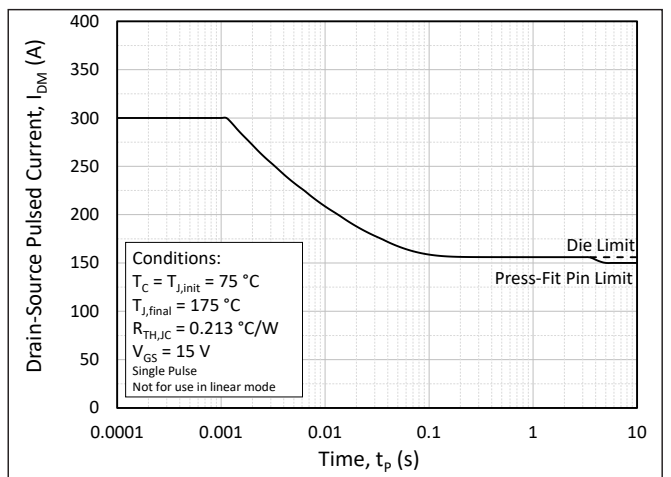
**Figure 15.** MOSFET Switching Energy vs. External Gate Resistance



**Figure 16.** Reverse Recovery Energy vs. External Gate Resistance



**Figure 17.** MOSFET Junction to Heatsink Transient Thermal Impedance,  $Z_{th JHS}$  (°C/W)



**Figure 18.** Pulsed Current Safe Operating Area



Typical Performance

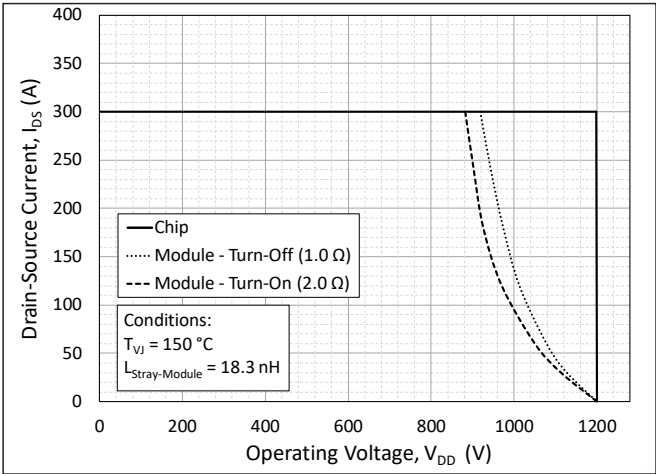


Figure 19. Switching Safe Operating Area

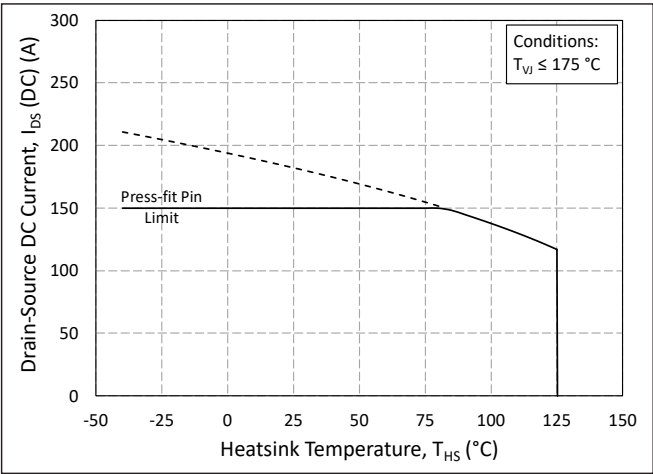


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

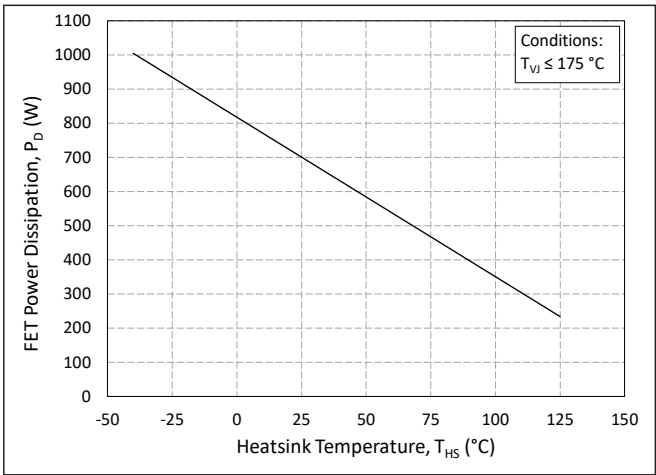


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

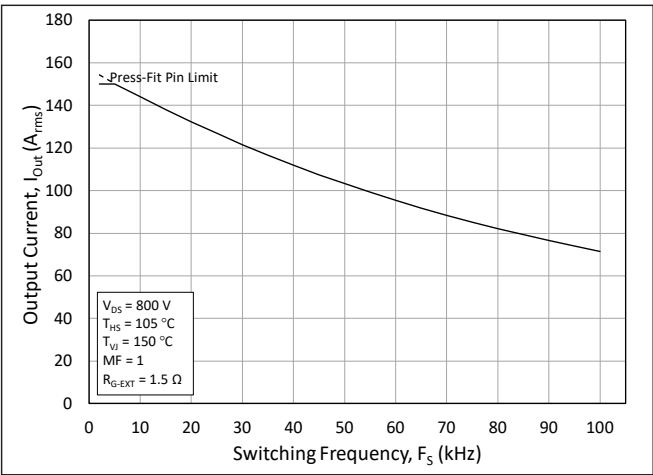


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

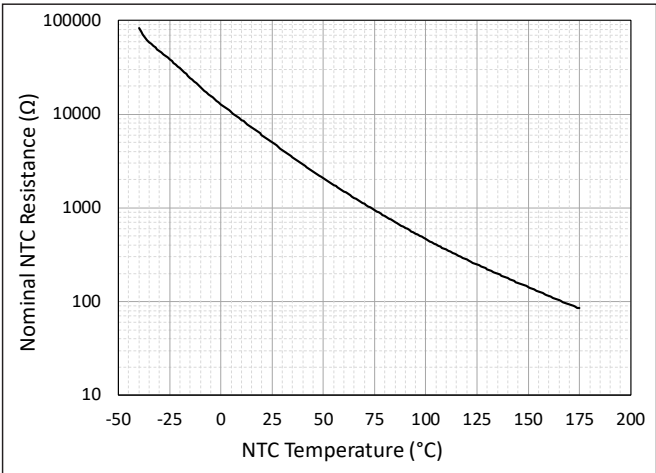
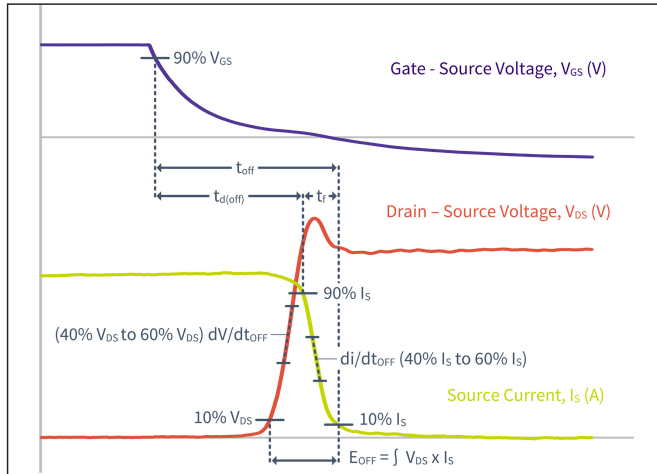
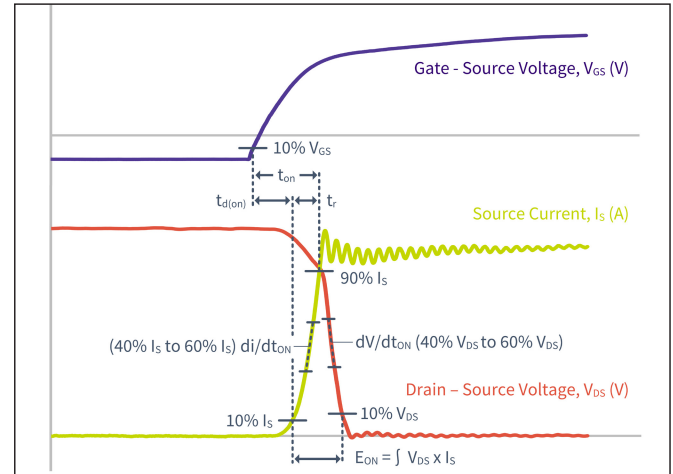


Figure 23. Nominal NTC Resistance vs. NTC Temperature

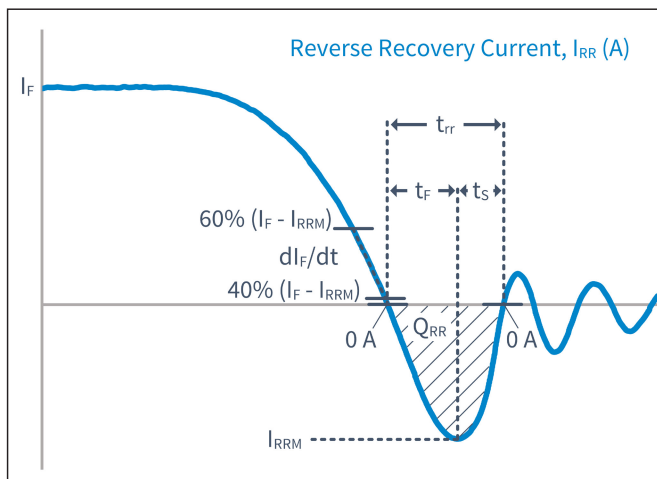
## Definitions



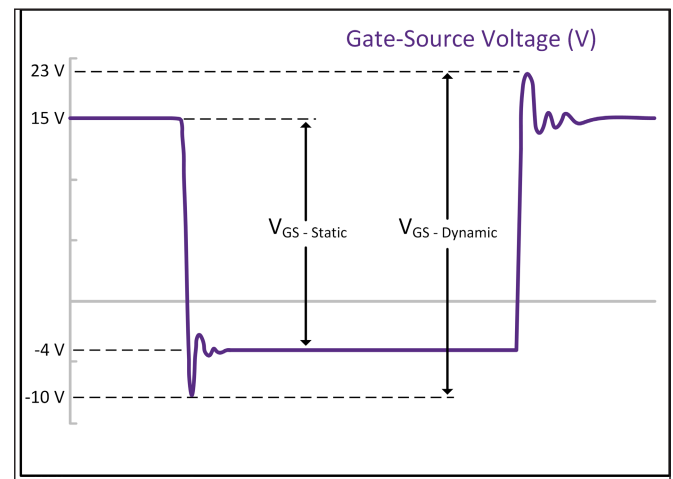
**Figure 30.** Turn-off Transient Definitions



**Figure 31.** Turn-on Transient Definitions



**Figure 32.** Reverse Recovery Definitions

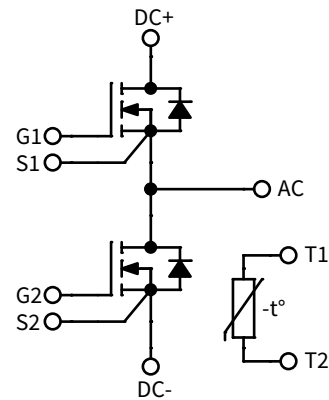
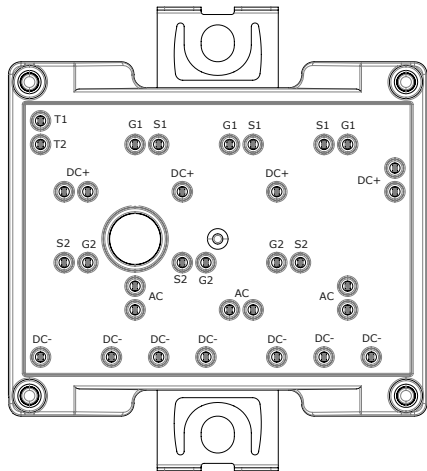


**Figure 33.**  $V_{GS}$  Transient Definitions

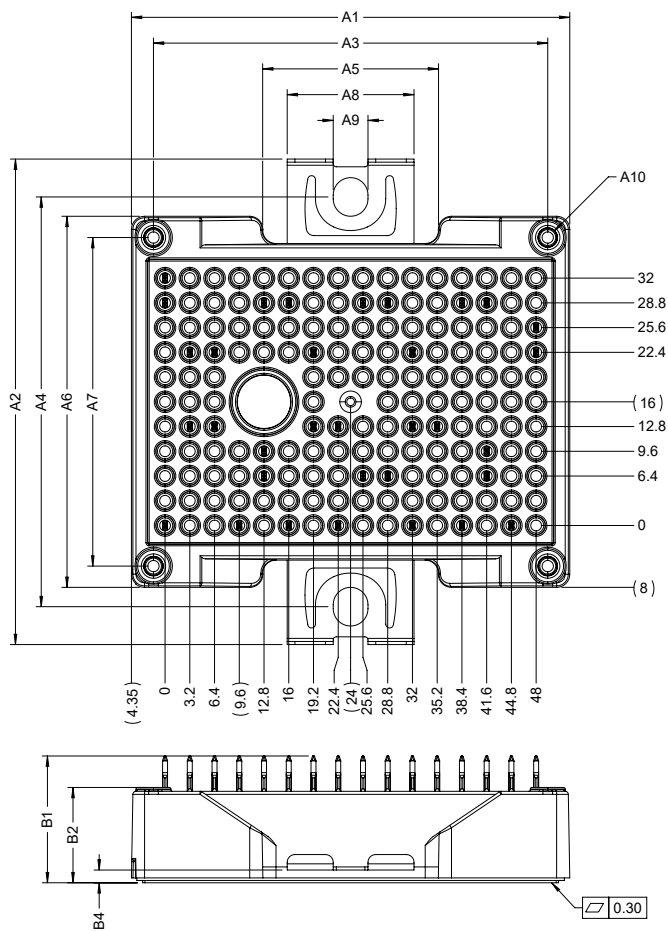
Note (7): The CGD1700HB2M-UNA, which features the UCC21710 gate driver IC, was used to evaluate dynamic performance. The typical driver high-state output resistance of  $2.5\ \Omega$  and low-state output resistance of  $0.3\ \Omega$  are not included in the  $R_{G(ext)}$  values on this datasheet.



Pinout



Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	56.7	±0.30
A2	62.8	±0.50
A3	51	±0.15
A4	(53)	REF.
A5	22.7	±0.30
A6	48	±0.30
A7	42.5	±0.15
A8	16.4	±0.20
A9	4.5	±0.10
A10	∅2.3 ∇8.5	∅: <sup>+0</sup> <sub>-0.10</sub> ∇: ±0.30
B1	16.4	±0.50
B2	12.33	±0.35
B4	1.65	±0.20
ALL PIN LOCATIONS		±0.40



## Product Ordering Code

Part Number	Description
CAB011A12GM3	Without Pre-Applied Phase Change Thermal Interface Material
CAB011A12GM3T	With Pre-Applied Phase Change Thermal Interface Material

## Supporting Links & Tools

### Simulation Tools & Support

- [All LTSpice Models](#)
- [All PLECS Models](#)
- [SpeedFit 2.0 Design Simulator™](#)
- [Technical Support Forum](#)

### Compatible Evaluation Hardware

- [EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board](#)
- [UCC21710QDWEVM-054: Texas Instruments® Gate Driver Board](#)
- [Si823H-AxWA-KIT: Skyworks® Gate Driver Board](#)
- [ACPL-355JC: Broadcom® Gate Driver Board](#)
- [CGD1700HB2M-UNA: Wolfspeed Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

### Application Notes

- [PRD-02302: Wolfpack Mounting Instructions and PCB Requirements](#)
- [PRD-06379: Environmental Considerations for Power Electronics](#)
- [PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility](#)
- [PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide](#)
- [PRD-07968: Wolfspeed WolfPACK™ Dynamic Performance](#)
- [PRD-08376: Thermal Characterization Methods and Applications](#)
- [PRD-08710: Measuring Stray Inductance in Power Electronics Systems](#)



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