

CA-IS3062 Isolated CAN Transceiver

1. Key Features

- Meets the ISO11898-2 Standard
- Isolation Rating up to 5.0kVrms
- 2.5V ~ 5V High Logical I/O Voltage Range
- High Data Rate: 1 Mbps
- High CMTI: $\pm 150\text{kV}/\mu\text{s}$ (Typical)
- Bus Fault Protection Voltage: $\pm 40\text{V}$
- Low Loop Delay:
 - 150 ns (Typical)
 - 210 ns (Maximum)
- Driver Dominant Time Out (TXD)
- Thermal Shutdown Protection
- Maximum Number of Nodes: 110
- Unpowered Nodes do not Interfere with the Bus
- Wide Operating Temperature Range: -40°C to 125°C
- Safety-Related Certification (Pending):
 - 61010-1 VDE Certification
 - IEC 60950-1, IEC 61010-1 and IEC 60601-1 Certification
 - TUV 5kV_{RMS} Reinforced Insulation Approved to EN/UL/CSA 60950-1
 - CQC Reinforced Insulation in accordance with GB4843.1-2011

2. Applications

- CAN Data Bus
- Industrial Field Network
- Building and Greenhouse Environmental Control Automation
- Security System
- Transport
- Medical
- Telecom

3. Description

The CA-IS3062 device is a galvanically-isolated controller area network (CAN) Physical Layer Transceiver that meets the specifications of the ISO11898-2 standard. This device uses on-chip silicon dioxide (SiO₂) capacitors as an isolation barrier to create a completely isolated interface between the CAN protocol controller and the physical layer bus. Used in conjunction with isolated power supplies, this device can prevent noises and interferences from the sensitive circuits.

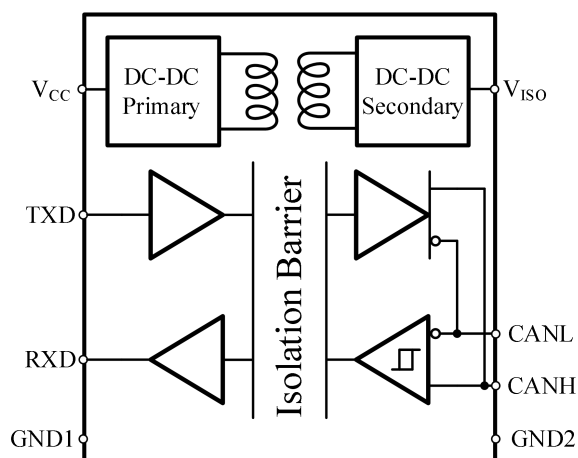
The CA-IS3062 device can provide differential transmission and reception capabilities for CAN protocol controller and physical layer bus respectively, with a data rate of up to 1Mbps. This device also has the functions of overcurrent protection, overvoltage protection, ground loss protection (-40V to 40V), thermal shutdown and short-circuit protection. Normally, the common mode voltage should be between -12V and 12V .

The CA-IS3062 device supports a wide ambient temperature range of -40°C to 125°C . The device is available in the wide-body SOIC16 packages.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
JM 3062	SOIC16-WB(W)	10.30mm ×7.50mm

Simplified Functional Block Diagram



4. Ordering Guide

Table 4- 1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	V _{CC} (V)	Data Rate (kbps)	Isolation Rating (V _{RMS})	Package
CA-IS3062	4.5~5.5	1000	5000	SOIC16-WB

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5. Revision History

Preliminary Version

6. PIN Descriptions and Functions

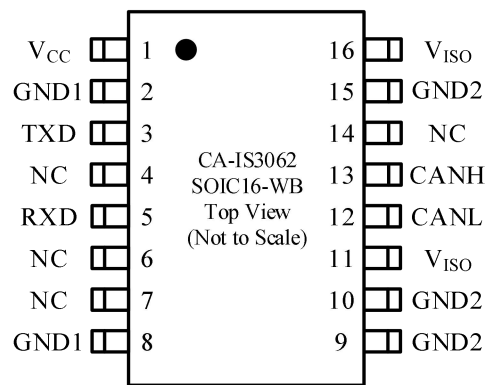


Figure 6-1 CA-IS3062 Pin Configuration

Table 6-1 CA-IS3062 Pin Description and Functions

Pin Name	Pin Number	Type	Description
	SOIC16		
V _{CC}	1	Supply	Digital-side Power Supply, Side A
GND1	2	Ground	Digital-side Ground Connection, Side A
TXD	3	Input	CAN Transmit Data Input
NC	4	–	Not Connected
RXD	5	Output	CAN Receive Data Output
NC	6	–	Not Connected
NC	7	–	Not Connected
GND1	8	Ground	Digital-side Ground Connection, Side A
GND2	9	Ground	Transceiver-side Ground Connection, Side B
GND2	10	Ground	Transceiver-side Ground Connection, Side B
V _{ISO}	11	Supply	Transceiver-side Power Supply, Side B, Please connect pin11 and pin16 together
CANL	12	Input / Output	Low-Level CAN Bus Line
CANH	13	Input / Output	High-Level CAN Bus Line
NC	14	–	Not Connected
GND2	15	Ground	Transceiver-side Ground Connection, Side B
V _{ISO}	16	Supply	Transceiver-side Power Supply, Side B, Please connect pin11 and pin16 together

7. Specifications

7.1. Absolute Maximum Ratings¹

		MIN	MAX	UNIT
V_{CC}, V_{ISO}	Supply Voltage ²	-0.5	6.0	V
V_I	Digital-Side Input Voltage (TXD)	-0.5	$V_{CC}+0.5^3$	V
V_{CANH} or V_{CANL}	Transceiver-Side Voltage (CANH or CANL)	-40	40	V
I_O	Receiver Output Current	-15	15	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

NOTE:

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All input/output digital voltage values are with respect to the digital-side ground terminal (GND1), and the differential I/O bus voltages are with respect to the transceiver-side ground terminal (GND2).
- Maximum voltage must not exceed 6 V.

7.2. ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹	±5000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ²	±1500	

NOTE:

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3. Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC}	Transceiver-Side Supply Voltage	4.5	5	5.5	V
V_I or V_{IC}	Transceiver-Side Bus Voltage	-12		12	V
V_{IH}	High-Level Input Voltage	Driver (TXD)		$V_{CC}+0.3$	V
V_{IL}	Low-Level Input Voltage	Driver (TXD)		0.8	V
V_{ID}	Differential Input Voltage	-7		7	V
I_{OH}	High-level Output Current	Driver			mA
		Receiver			
I_{OL}	Low-level Output Current	Driver		70	mA
		Receiver		2.5	
T_A	Ambient Temperature			125	°C
T_J	Junction Temperature			150	°C
P_D	Total Power Consumption	$V_{CC} = 5.5V, T_A = 125^{\circ}C, R_L = 60\Omega$, TXD Input is a 500kHz Square Wave (50% Duty)		900	mW
$T_{J(shutdown)}$	Thermal Shutdown Temperature ¹		165		°C

NOTE:

- Operation beyond thermal shutdown temperature may affect device reliability

7.4. Thermal Information

THERMAL METRIC	SOIC16-WB	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	86.5	°C/W

7.5. Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE	UNIT
			G/W	
CLR	External clearance ¹	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage ¹	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 400 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	
DIN V VDE V 0884-11:2017-01 ²				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	V _{PK}
V _{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDb) Test	600	V _{RMS}
		DC voltage	849	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t= 1 s (100% production)	7070	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ³	Test method per IEC 60065, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	6250	V _{PK}
q _{pd}	Apparent charge ⁴	Method a, After Input/Output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s	≤5	
		Method b1, At routine test (100% production) and preconditioning (type test) V _{ini} = 1.2 × V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s	≤5	
C _{IO}	Barrier capacitance, input to output ⁵	V _{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R _{IO}	Isolation resistance ⁵	V _{IO} = 500 V, T _A = 25°C	>10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	>10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	>10 ⁹	
	Pollution degree		2	
UL 1577				
V _{ISO}	Maximum withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5000	V _{RMS}
NOTE:				
1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.				
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.				
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.				
4. Apparent charge is electrical discharge caused by a partial discharge (pd).				
5. All pins on each side of the barrier tied together creating a two-terminal device.				

7.6. Safety-Related Certifications

VDE(Pending)	CSA(Pending)	UL(Pending)	CQC(Pending)	TUV(Pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4843.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013

7.7. Electrical Characteristics

Unless otherwise specified, all voltages are referenced to their respective grounds, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. All min / max specifications apply over the entire recommended working range. Unless otherwise specified, all typical specs are tested under $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$, $V_{CC} = 5\text{ V}$.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current							
I _{CC}	Digital-side Supply Current		V _I = 0 V , R _L = 60 Ω dominant timeout protection	14	20	29	mA
			V _I = V _{CC}	14	20	29	
Isolated Power Supply							
V _{ISO}	Output voltage	No Load	I _{ISO} =0mA	4.65	5.05	5.47	V
Driver							
V _{O(D)}	Bus Output Voltage (Dominant)	CANH	V _I = 0 V, R _L = 60 Ω, <i>See Figure 8- 1 Figure 8- 2</i>	2.9	3.4	4.5	V
		CANL		0.5		2	
V _{O(R)}	Bus Output Voltage (Recessive)		V _I = 2 V, R _L = 60 Ω, <i>See Figure 8- 1 Figure 8- 2</i>	2	2.5	3	V
V _{OD(D)}	Differential Output Voltage (Dominant)		V _I = 0 V, R _L = 60 Ω, <i>See Figure 8- 1 Figure 8- 2 Figure 8- 3</i>	1.5		3	V
			V _I = 0 V, R _L = 45 Ω, <i>See Figure 8- 1 Figure 8- 2 Figure 8- 3</i>	1.3		3	V
V _{OD(R)}	Differential Output Voltage (Recessive)		V _I = 3 V, R _L = 60 Ω, <i>See Figure 8- 1 Figure 8- 2</i>	-80		80	mV
			V _I = 3 V, No Load	-0.5		0.05	V
V _{OC(D)}	Common Mode Output Voltage (Dominant)		<i>See Figure 8- 7</i>	2	2.5	3	V
V _{OC(pp)}	Common Mode Output Voltage Peak to Peak				60		V
I _{IH}	High-level Input Current, TXD Input		V _I = 2 V			20	μA
I _{IL}	Low-level Input Current, TXD Input		V _I = 0.8 V	-20			μA
I _{OS(SS)}	Short-Circuit Steady State Output Current		V _{CANH} = -12 V, CANL = open, <i>See Figure 8- 10</i>	105	-72		mA
			V _{CANH} = 12 V, CANL = open, <i>See Figure 8- 10</i>		0.36	2	
			V _{CANL} = -12 V, CANH = open, <i>See Figure 8- 10</i>	-2	-0.5		
			V _{CANL} = 12 V, CANH = open, <i>See Figure 8- 10</i>		71	105	
CMTI	Common Mode Transient Immunity		V _I = 0 V or V _{CC} , <i>See Figure 8- 11</i>	100	150		kV/μs
Receiver							
V _{IT+}	Positive Input Threshold Voltage				0.8	0.9	V
V _{IT-}	Negative Input Threshold Voltage			0.5	0.65		V
V _{HYS}	Hysteresis Voltage for Input Voltage			50	125		mV
V _{OH}	High-Level Output Voltage, V _{CC} = 5V		I _{OH} = -4 mA, <i>See Figure 8- 6</i>	V _{CC} - 0.8	4.8		V
			I _{OH} = -20 μA, <i>See Figure 8- 6</i>	V _{CC} - 0.1	5		
V _{OL}	Low-Level Output Voltage		I _{OH} = -4 mA, <i>See Figure 8- 6</i>		0.2	0.4	V
			I _{OH} = -20 μA, <i>See Figure 8- 6</i>		0	0.1	
C _I	Input Capacitance to Ground (CANH or CANL)		TXD = 3V, V _I = 0.4xsin(2πft) + 2.5 V, f = 1MHz		13		pF
C _{ID}	Differential Input Capacitance (CANH - CANL)		TXD = 3V, V _I = 0.4xsin(2πft), f = 1MHz		5		pF
R _{IN}	Input Resistance (CANH or CANL)		TXD = 3V	28	32	36	kΩ
R _{ID}	Differential Input Resistance (CANH - CANL)		TXD = 3V	56	62	68	kΩ
R _{I(m)}	Input Resistance Matching (1 – [R _{IN(CANH)} / R _{IN(CANL)}])		V _{CANH} = V _{CANL}	-5%	0%	5%	
CMTI	Common Mode Transient Immunity		V _I = 0 V or V _{CC} , <i>See Figure 8- 11</i>	100	150		kV/μs

7.8. Timing Characteristics—Device

Unless otherwise specified, all voltages are referenced to their respective grounds, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. All min / max specifications apply over the entire recommended working range. Unless otherwise specified, all typical specs are tested under $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$, $V_{CC} = 5\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total Loop Delay, Driver Input TXD to Receiver RXD, Recessive to Dominant	See Figure 8- 8	110	150	210	ns
t_{loop2}	Total Loop Delay, Driver Input TXD to Receiver RXD, Dominant to Recessive		110	150	210	ns

7.9. Timing Characteristics—Driver and Receiver

Unless otherwise specified, all voltages are referenced to their respective grounds, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$. All min / max specifications apply over the entire recommended working range. Unless otherwise specified, all typical specs are tested under $T_A = -40^\circ\text{C} \sim 125^\circ\text{C}$, $V_{CC} = 5\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
t _{PLH}	Propagation Delay Time, Output Recessive to Dominant	See Figure 8- 4	35	75	130	ns
t _{PHL}	Propagation Delay Time, Output Dominant to Recessive		35	55	100	
t _r	Differential Output Signal Rise Time			40	60	
t _f	Differential Output Signal Fall Time			40	60	
t _{TXD_DTO} ¹	Dominant Time-Out	C _L = 100 pF, See Figure 8- 9	300	450	700	μs
Receiver						
t _{PLH}	Propagation Delay Time, Output Low to High	See Figure 8- 6	55	110	140	ns
t _{PHL}	Propagation Delay Time, Output High to Low		55	80	140	
t _r	Output Signal Rise Time			2.5	6	
t _f	Output Signal Fall Time			2.5	6	
NOTE:						
1. Once the time that driver enters the dominant state is longer than t _{TXD_DTO} , the dominant timeout function will shut down the driver to release the bus into recessive state, preventing the bus from being locked in the dominant state. The drive can recover the function of transmitting only after entering the recessive state.						

8. Parameter Measurement Information

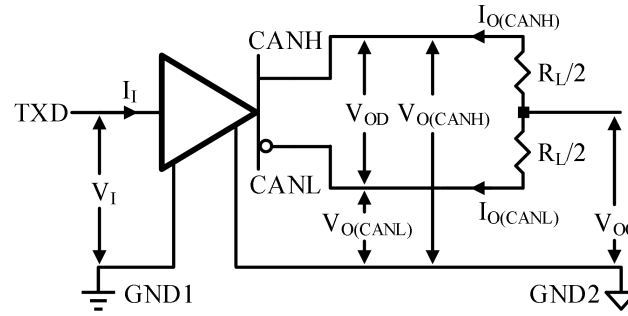


Figure 8- 1 Driver Voltage and Current Definition

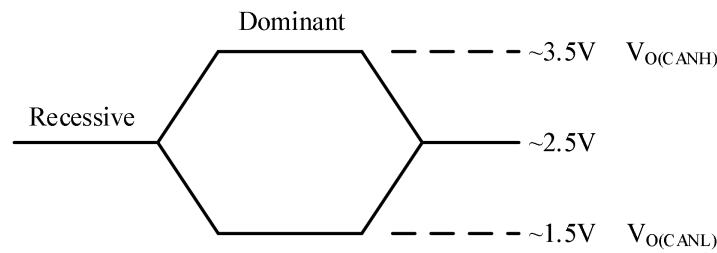


Figure 8- 2 Bus Logic State Voltage Definitions

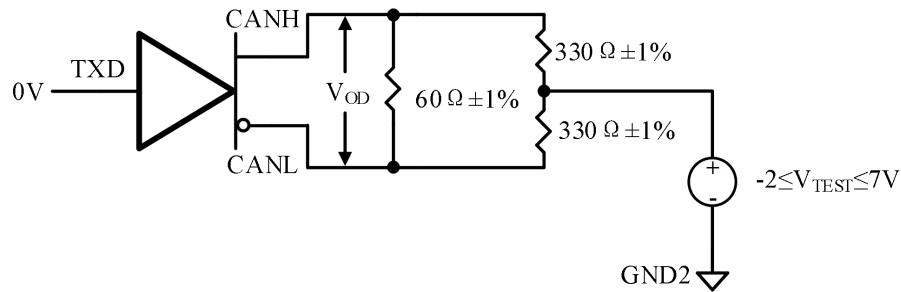
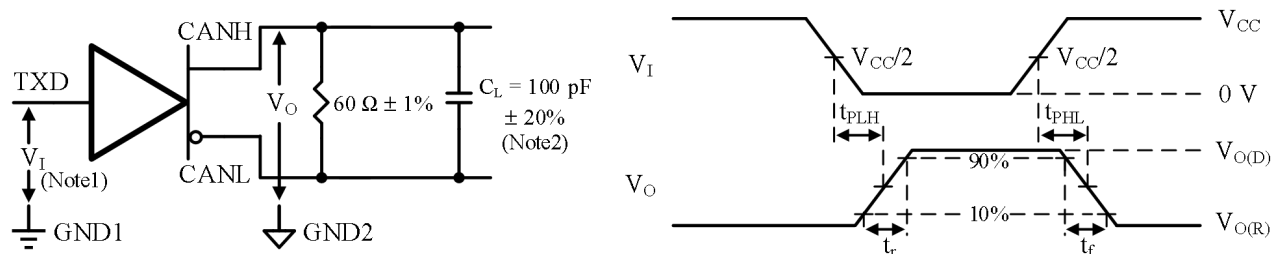


Figure 8- 3 Driver Output Voltage (V_{OD}) Test Circuits (Common Mode Load)



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: $PRR \leq 125 \text{ kHz}$, 50% duty cycle, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$, $Z_0 = 50 \Omega$.
2. C_L is the load capacitance about 100pF together with the instrumentation capacitance and the parasitic capacitance of the fixture.

Figure 8- 4 Driver Test Circuit and Voltage Waveform

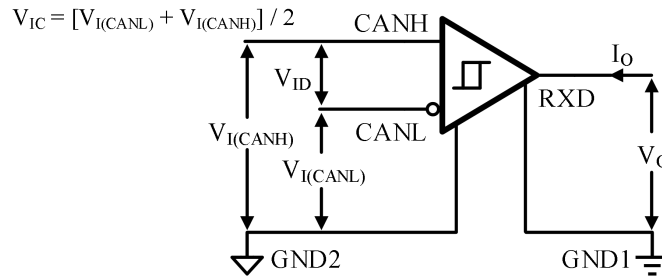
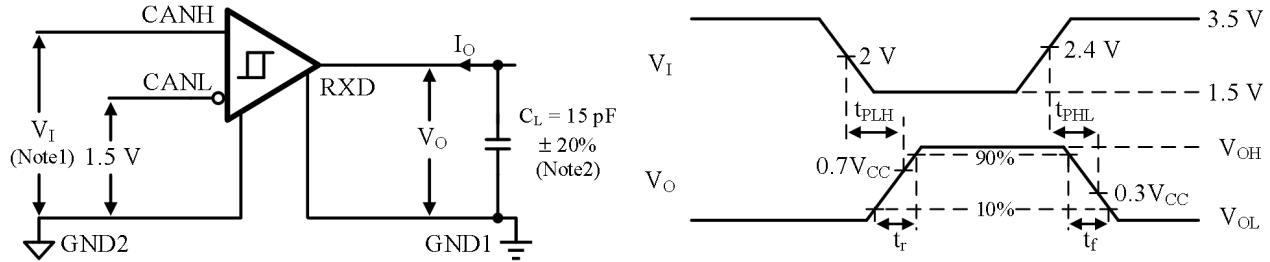


Figure 8- 5 Receiver Voltage and Current Definitions



NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: $PRR \leq 125 \text{ kHz}$, 50% duty cycle, $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$, $Z_0 = 50 \Omega$.
2. C_L is the load capacitance about 100pF together with the instrumentation capacitance and the parasitic capacitance of the fixture.

Figure 8- 6 Receiver Test Circuit and Voltage Waveform

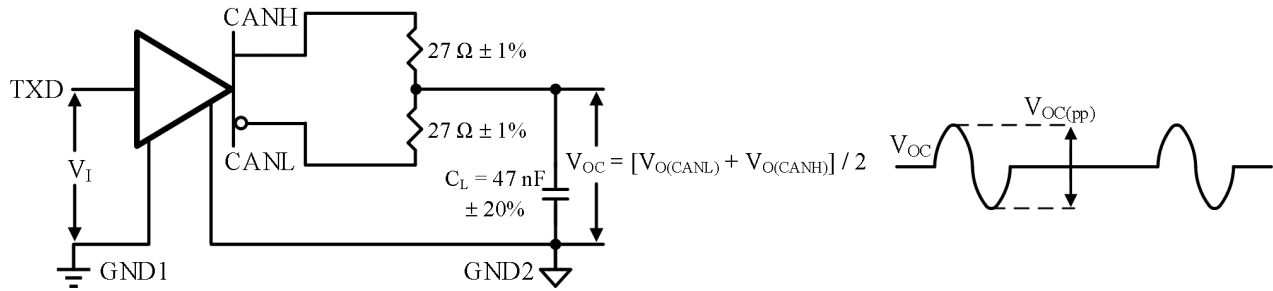


Figure 8- 7 Common Mode Output Peak-to-Peak Voltage Test Circuit and Waveform

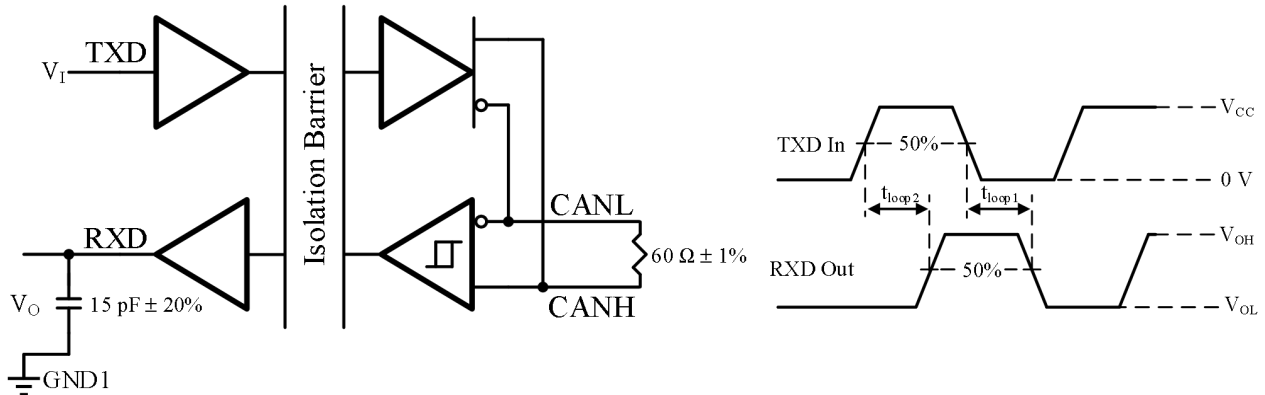


Figure 8- 8 t_{loop} Test Circuit and Voltage Waveform

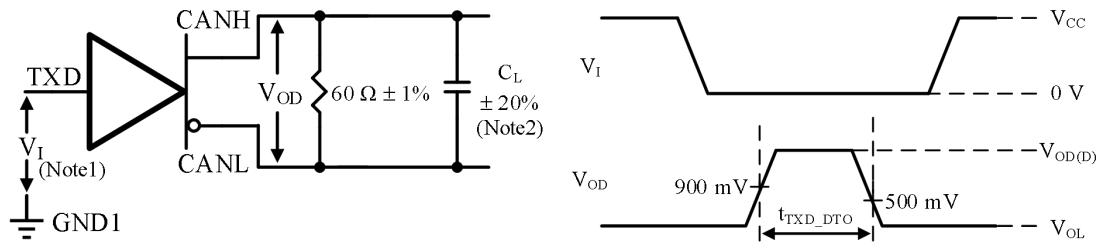


Figure 8-9 Dominant Time-out Test Circuit and Voltage Waveforms

NOTE:

1. A square wave generator generate the V_{IN} input signal with the following constraints: $t_r \leq 6\text{ns}$, $t_f \leq 6\text{ns}$, $Z_0 = 50 \Omega$.
2. C_L is the load capacitance about 100pF together with the instrumentation capacitance and the parasitic capacitance of the fixture.

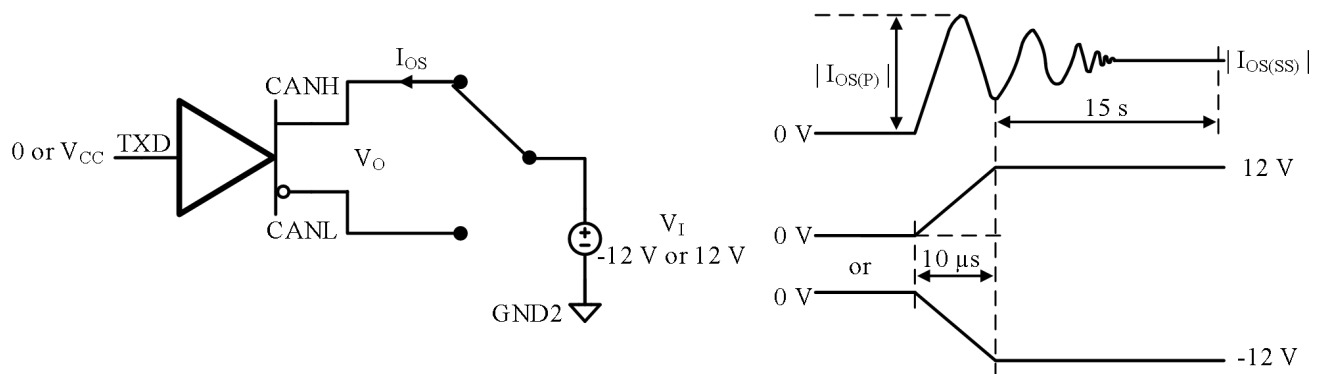


Figure 8-10 Driver Short-Circuit Current Test Circuit and Waveforms

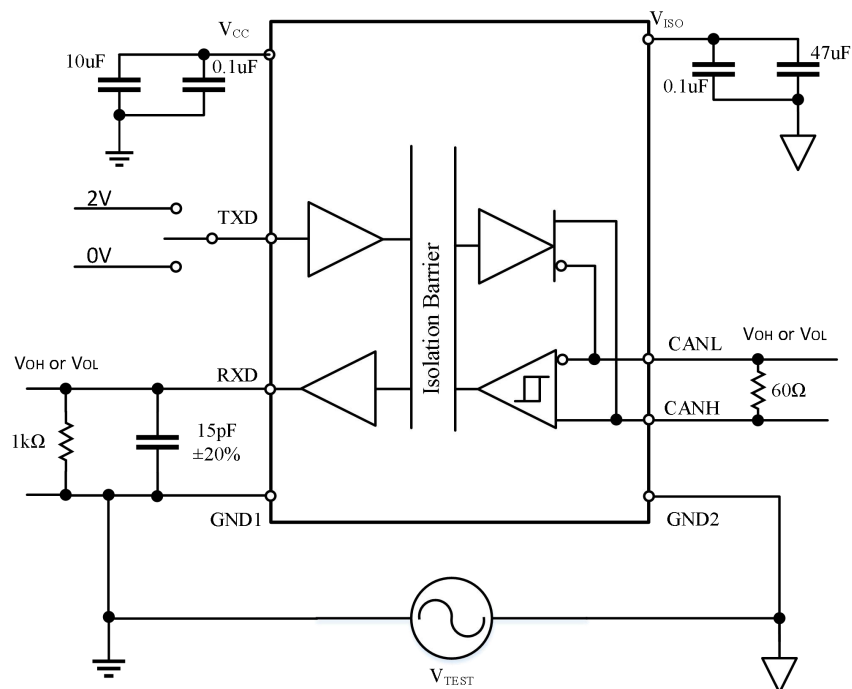


Figure 8-11 CMTI Test Circuit

9. Detailed Description

9.1. Theory of Operation

The CA-IS3062 device is an isolated controller area network (CAN) physical layer transceiver that offers 5 kV_{RMS} isolation rating and 150 kV / μ s CMTI, integrated with the dominant timeout and thermal shutdown functions. The digital side of this device can be powered by a 5V power supply while the bus side is powered by internal integrated 5 V power supply, which is very suitable for harsh industrial control applications.

9.2. Functional Block Diagram

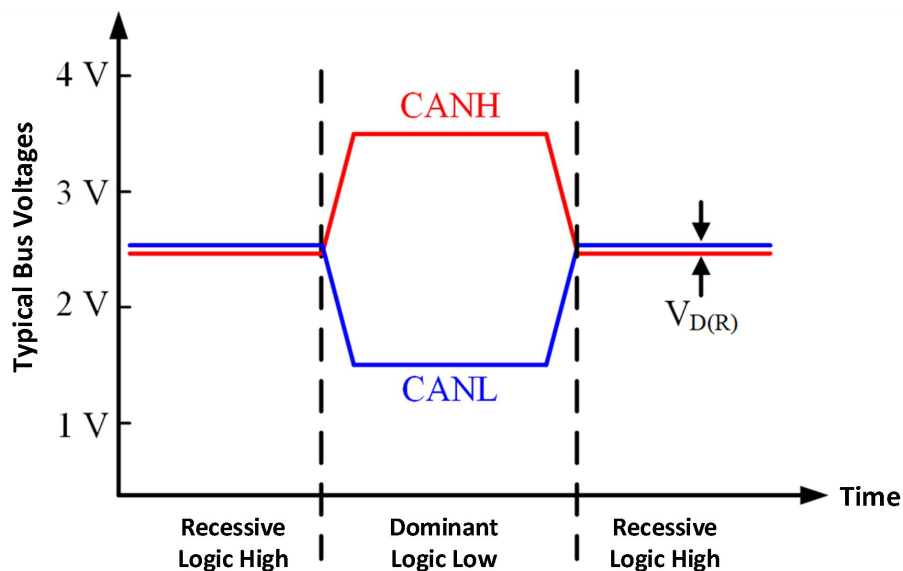


Figure 9-1 Typical Waveform of CAN Bus States

The CAN bus has two states during operation: dominant and recessive. When the differential voltage between CANH and CANL is greater than 0.9 V, the bus is in dominant state, and the CANH pin is logic high while the CANL pin is logic low. When the differential voltage between CANH and CANL is less than 0.5 V, the bus is in recessive state and the CANH and CANL pins are both in high impedance. A typical bus voltage waveform is shown in Figure 9- 1.

9.3. Protection Features

9.3.1. Signal Isolation

Signal isolation in the CA-IS3062 device is achieved by a digital isolator with capacitive isolation. On the digital side, the input signal is modulated to a high frequency by on-off key (OOK) modulation, and this high frequency signal propagates to the transceiver side through an on-chip silicon dioxide capacitor which can operate at a high voltage. At last, the digital isolator on transceiver side recovers the signal and then converts it into a standard level output to the CAN bus. Similarly, the transceiver side signal can also be modulated to high frequency and received by the digital side then output to RXD after demodulation and recovery. The ground on the digital side and the transceiver side can be completely separated. The isolation rating is up to 5 kV_{RMS}, ensuring the integrity and security of signal transmission between the microcontroller and the high-voltage bus in actual use.

9.3.2. Dominant Time-Out

The CA-IS3062 device has the dominant timeout function, which prevents TXD from being pulled down to a low level due to software or hardware failure. This failure may cause the bus to stuck in the dominant state and thus the whole network communication will be locked. The dominant timeout function is achieved by setting a counter, which counts the negative edge of the TXD input signal. When the low-level duration of TXD is longer than the dominant timeout time t_{TXD_DTO} , the transceiver will be turned off, and then the bus is released to the recessive state. The counter is set during the positive edge of the TXD input signal.

9.3.3. Thermal Shutdown

The CA-IS3062 device has integrated thermal shutdown protection function, which can protect the internal circuit of the device under over-temperature conditions. If the junction temperature of the device exceeds the thermal shutdown temperature $T_{J(shutdown)}$, the driver will be disabled, thereby blocking the signal transmission path from TXD to the bus. The typical thermal shutdown temperature is 165 °C. When the device junction temperature is lower than the thermal shutdown temperature, the driver will be re-enabled.

9.3.4. Current Limiting

The CA-IS3062 device has integrated current limiting function, which can prevent the device from being damaged by the large current when the transceiver side short-circuit occurs. Note that once the current-limiting protection occurs, it will be a large current in the device, which results in a larger loss.

9.4. Device Function Modes

Table 9-1 Function Table Abbreviation

Word	Description
H	High-Level
L	Low-Level
X	Unrelated
Z	High Impedance
?	Uncertain
Open	Open Circuit

Table 9-2 Driver Function Table

Input TXD	Output		Bus State
	CANH	CANL	
L	H	L	Dominant
H or Open	Z	Z	Recessive

Table 9-3 Receiver Function Table

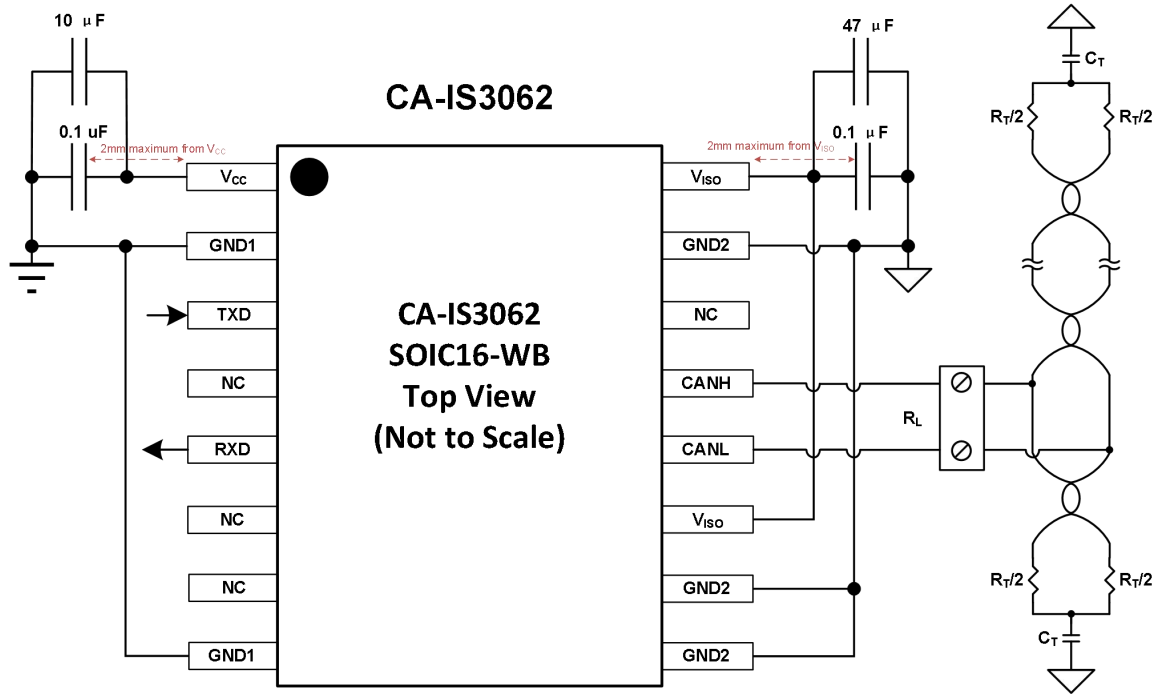
CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD
$0.9\text{ V} \leq V_{ID}$	Dominant	L
$0.5\text{ V} < V_{ID} < 0.9\text{ V}$	?	?
$V_{ID} \leq 0.5\text{ V}$	Recessive	H
Open ($V_{ID} \approx 0\text{ V}$)	Open	H

Table 9-4 Transceiver Function Table

Driver				Receiver		
Inputs	Outputs		Bus State	Differential Inpus $V_{ID} = V_{CANH} - V_{CANL}$	RXD Outputs	Bus State
TXD	CANH	CANL				
L	H	L	Dominant	$0.9\text{ V} \leq V_{ID}$	L	Dominant
H	Z	Z	Recessive	$0.5\text{ V} < V_{ID} < 0.9\text{ V}$	?	?
Open	Z	Z	Recessive	$V_{ID} \leq 0.5\text{ V}$	H	Recessive
X	Z	Z	Recessive	Open	H	Recessive

10. Application Information

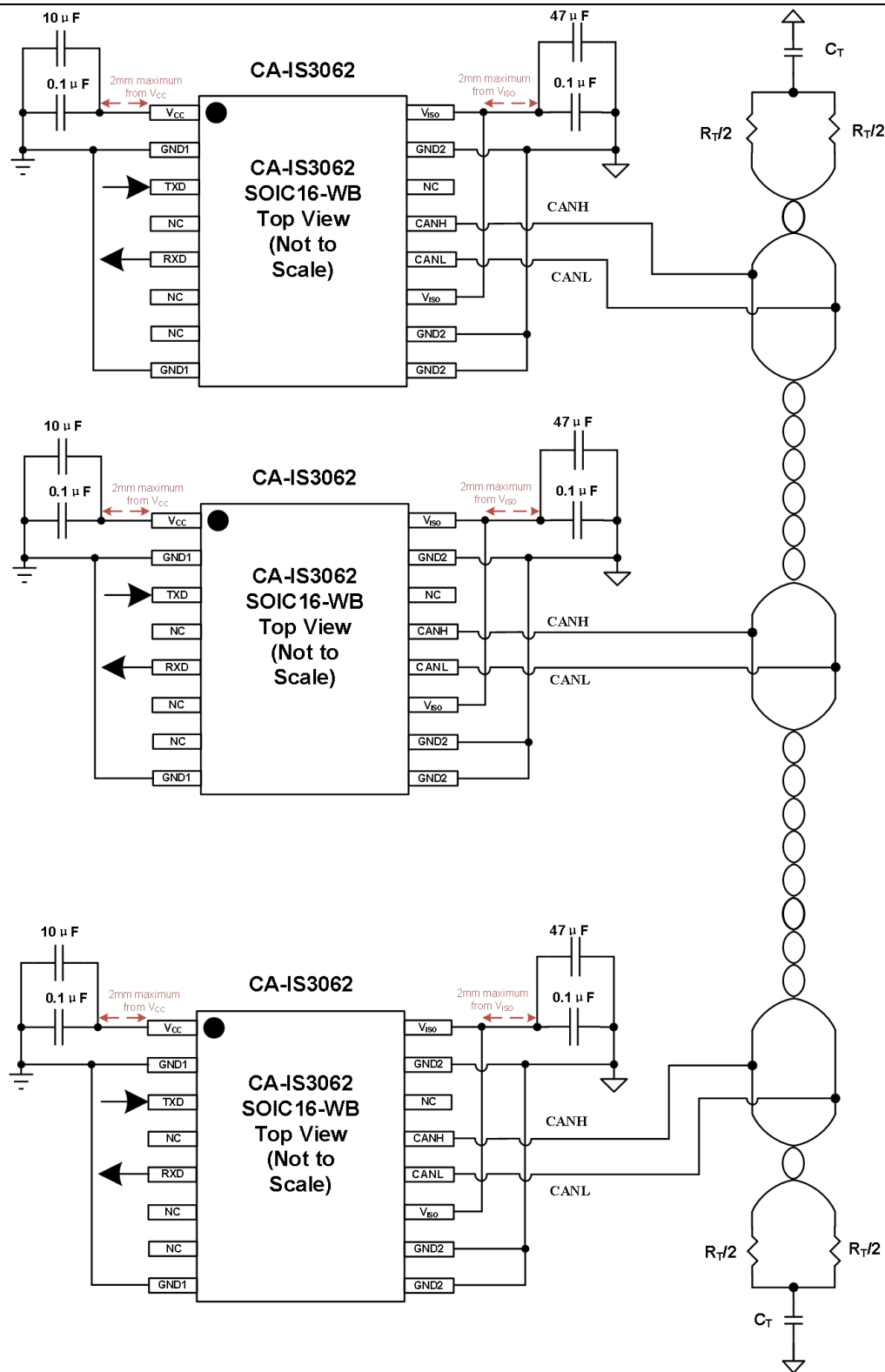
A $10\mu\text{F}$ capacitor between V_{CC} and GND1, and a $47\mu\text{F}$ capacitor between V_{ISO} and GND2, the CA-IS3062 can work normally. In the design the circuit, it is recommended to place a $47\mu\text{F}$ capacitor between the V_{ISO} and GND2. Figure 10- 1and Figure 10-2 are typical application diagrams of the CA-IS3062.



Note:

1. Termination resistor R_T should be equal to the characteristic impedance of the cable

Figure10- 1 CA-IS3062 Typical CAN Node



Note:

1. Termination resistor R_T should be equal to the characteristic impedance of the cable.
2. The CA-IS3062 device can support up to 110 nodes.

Figure10- 2 CA-IS3062 Typical CAN Bus

11. Package Information

SOIC16-WB Package

The figure below illustrates the package details and the recommended land pattern details for the CA-IS3062 isolated CAN transceiver in a 16-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.

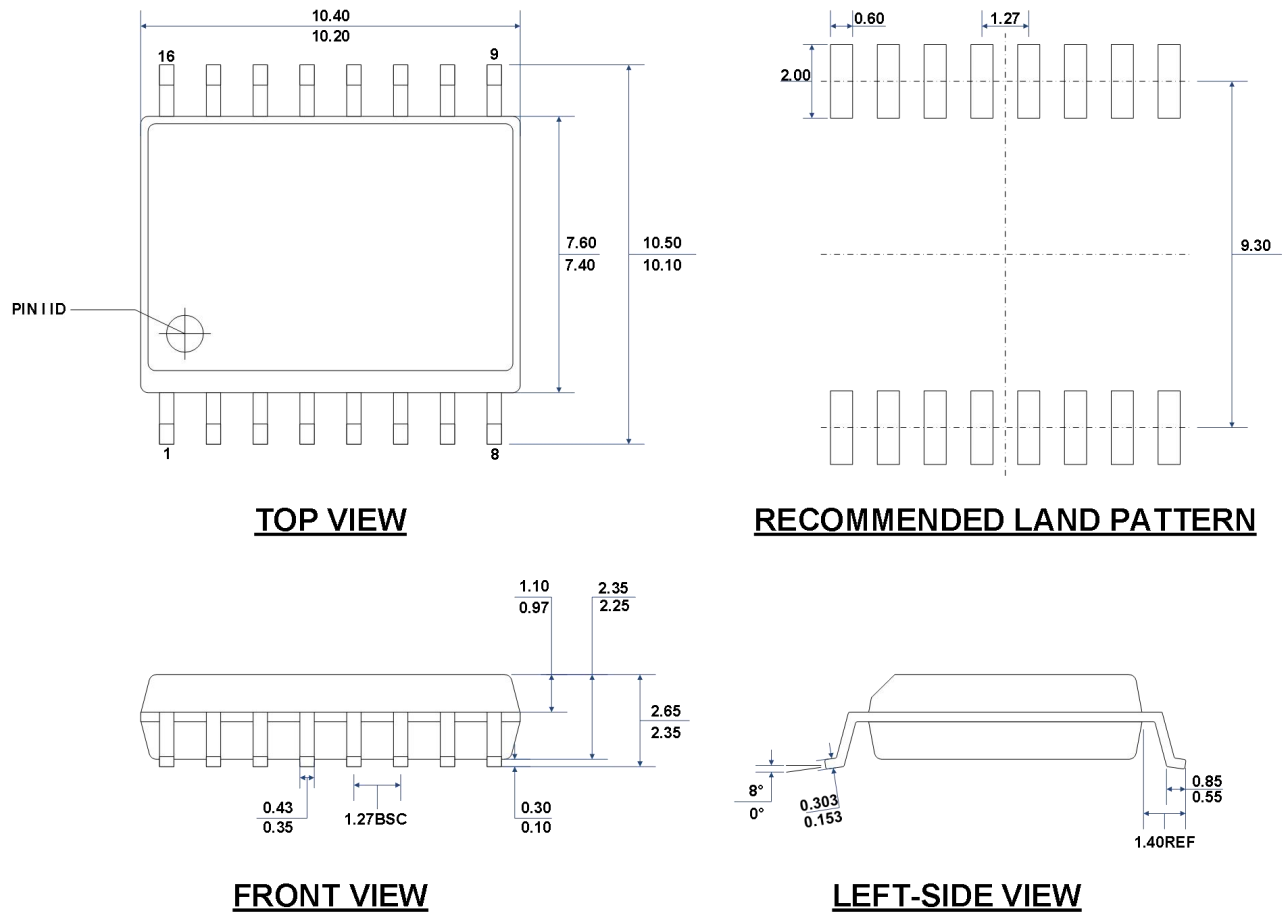
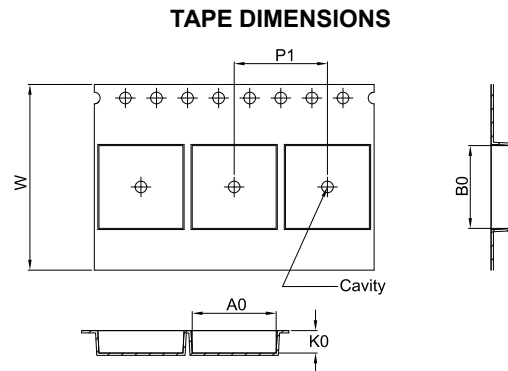
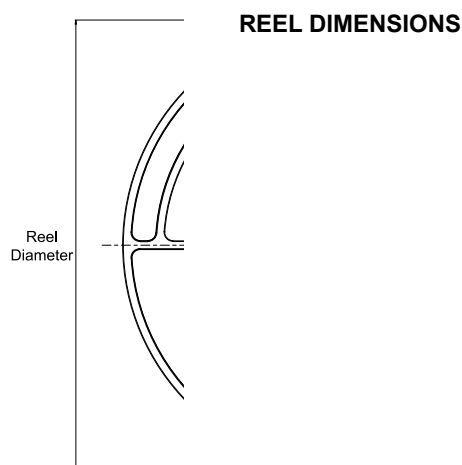


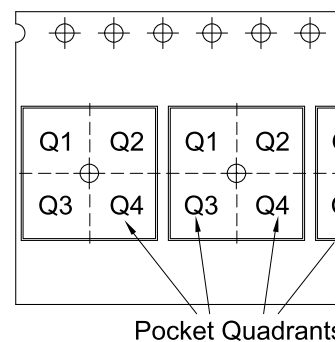
Figure 11-1 CA-IS3062 SOIC16-WB Package

12. TAPE

AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3062W	SOIC	W	16	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1

13. Ordering Information

Orderable Device	Status ¹	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp(°C)	Device Marking	Samples
CA-IS3062W	PREVIEW	SOIC	W	16	1000				-40 to 125		
1. The marketing status values are defined as follows: ACTIVE: Product device recommended for new designs. LIFEBUY:CA has announced that the device will be discontinued, and a lifetime-buy period is in effect. NRND: Not recommended for new designs. Device is in production to support existing customers, but CA does not recommend using this part in new design. PREVIEW: Device has been announced but is not in production. Samples may or may not be available. OBSOLETE:CA has discontinued the production of the device.											

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