C3M0900170M

1700V 900mΩ Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- Fully isolated package for simplified assembly
- High-speed switching with low capacitances
- High blocking voltage with low $R_{DS(on)}$
- 12V..18V / 0V V_{GS} compatible with most flyback controllers
- Ultra-low drain-gate capacitance
- Halogen free, RoHS compliant

Benefits

- Smooth switching waveforms
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increase system switching frequency
- Increase system reliability

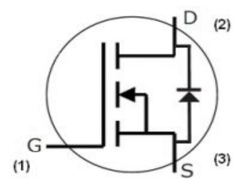
Typical Applications

- Auxillary power supplies
- Switch mode power supplies
- High-voltage capacitive loads

Package

Halogen-Free

RoHS COMPLIANT



Orderable Part Number	Package	Marking
C3M0900170M	TO-3PF 3L	C3M0900170M

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1700	V	$T_C = 25°C$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+20	V	Transient	
Operational Turn-On Gate - Source Voltage	$V_{GS\ op}$		+12...+18		V		
Operational Turn-Off Gate - Source Voltage	$V_{GS\ op}$		-4...0		V		
DC Continuous Drain Current	I_D			4.0	A	$V_{GS} = 15V$, $T_C = 25\ °C$, $T_J \leq 175\ °C$	Note 2
				2.9	A	$V_{GS} = 15V$, $T_C = 100\ °C$, $T_J \leq 175\ °C$	
Pulsed Drain Current	I_{DM}			15	A	t_{Pmax} limited by T_{jmax} $V_{GS} = 15V$, $T_C = 25\ °C$	Fig. 22
Power Dissipation	P_D			33	W	$T_C = 25\ °C$, $T_J = 175\ °C$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +175	°C		
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Review Application Note PRD-04814 for additional details
Note (2): Verified by design

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	3.1	4.2	V	V_{DS} = V_{GS}, I_D = 0.55 mA	Fig. 11
			2.6		V	V_{DS} = V_{GS}, I_D = 0.55 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 1700 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		900	1250	mΩ	V_{GS} = 15 V, I_D = 1.99 A	Fig. 4, 5, 6
			1938			V_{GS} = 15 V, I_D = 1.99 A, T_J = 175ºC	
g_{fs}	Transconductance		1		S	V_{DS}= 20 V, I_{DS}= 1.99 A	Fig. 7
			1			V_{DS}= 20 V, I_{DS}= 1.99 A, T_J = 175ºC	
C_{iss}	Input Capacitance		202		pF	V_{GS} = 0 V, V_{DS} = 1200 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		8				
C_{rss}	Reverse Transfer Capacitance		1.4				
E_{oss}	C_{oss} Stored Energy		8		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		10		pF	V_{GS} = 0 V, V_{DS} = 0 to 1200V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		13				
E_{ON}	Turn-On Switching Energy (External Diode)		154		μJ	V_{DS}=1200V, V_{GS}=-4V/15V, I_D=1.99A, $R_{G(ext)}$=2.5 Ω, L=1707μH, T_J=175ºC FWD= External SiC DIODE	Fig 26, 28
E_{OFF}	Turn-Off Switching Energy (External Diode)		15				
$t_{d(on)}$	Turn-On Delay Time		23		ns	V_{DS}=1200V, V_{GS}=-4V/15V I_D=1.99A, $R_{G(ext)}$=2.5 Ω T_J=175ºC L=1707μH Timing relative to V_{DS} Inductive load	Fig 27, 28
t_r	Rise Time		18				
$t_{d(off)}$	Turn-Off Delay Time		19				
t_f	Fall Time		43				
$R_{G(int)}$	Internal Gate Resistance		31		Ω	f=1MHz, V_{AC}=25mV	
Q_{gs}	Gate to Source Charge		4		nC	V_{DS} = 1200 V, V_{GS} = -4 V/15 V I_D = 1.99 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		4				
Q_g	Total Gate Charge		10				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 1200V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 1200V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.7		V	V_{GS} = -4 V, I_{SD} = 1 A	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 1 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current	5		A	V_{GS} = -4 V	
I_{SM}	Diode pulse Current		15	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	40		ns	V_{GS}=-4V, Is=1.99A, V_{SD}=1200V dif/dt=546A/μs , T_J=25 °C	
Q_{rr}	Reverse Recovery Charge	72		nC		
I_{rrm}	Reverse Recovery Current	3		A		
t_{rr}	Reverse Recovery Time	40		ns	V_{GS}=-4V, Is=1.99A, V_{SD}=1200V dif/dt=246A/μs , T_J=25 °C	
Q_{rr}	Reverse Recovery Charge	57		nC		
I_{rrm}	Reverse Recovery Current	2		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	3.4	4.5	°C/W		

Typical Performance

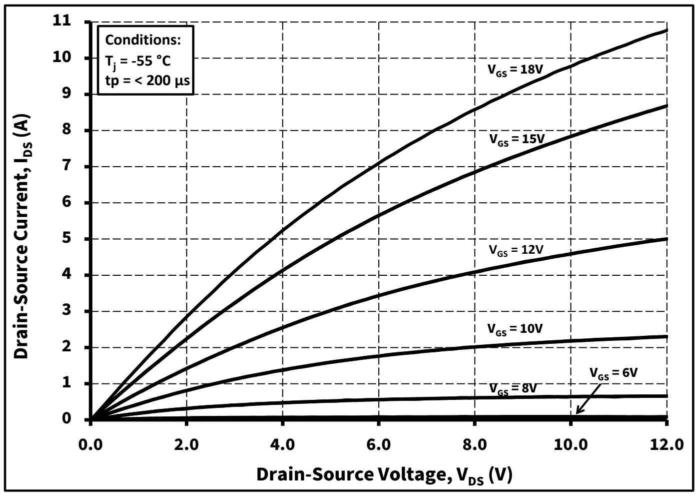


Figure 1. Output Characteristics T_J = -55 ºC

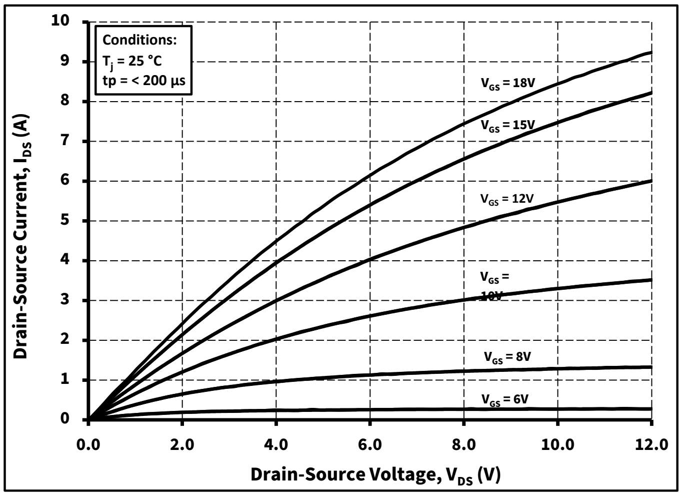


Figure 2. Output Characteristics T_J = 25 ºC

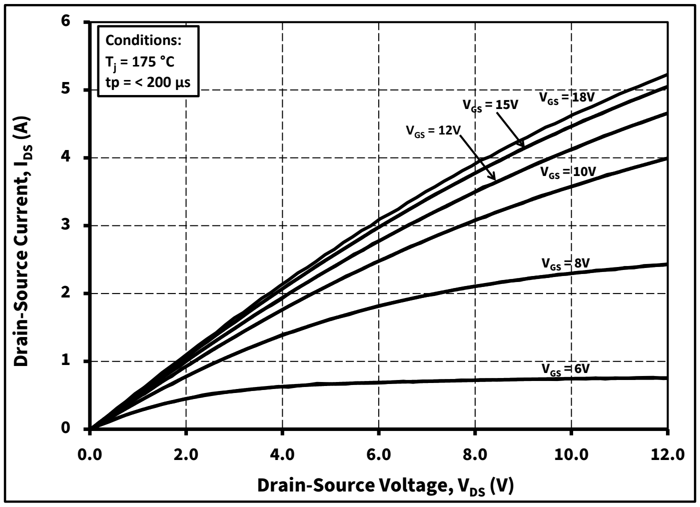


Figure 3. Output Characteristics T_J = 175 ºC

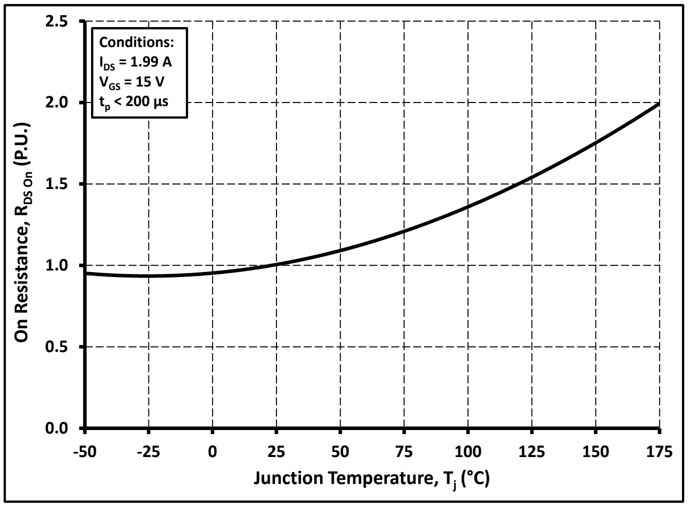


Figure 4. Normalized On-Resistance vs. Temperature

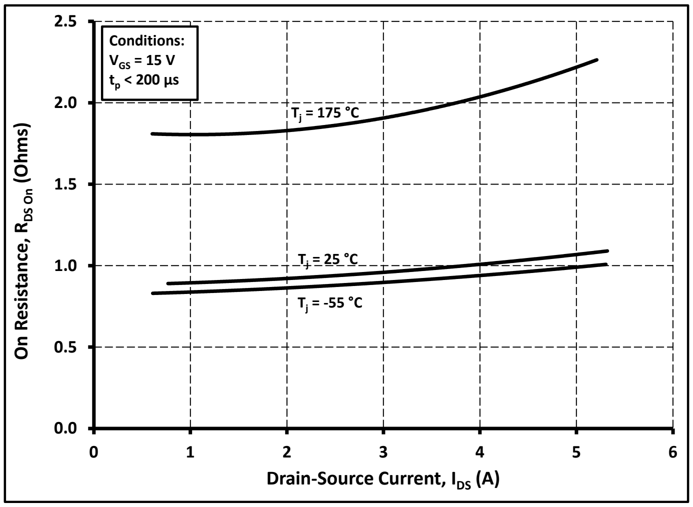


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

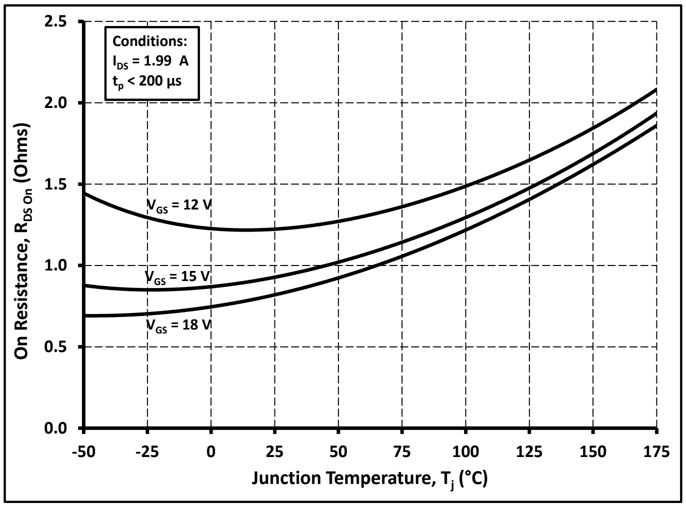


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

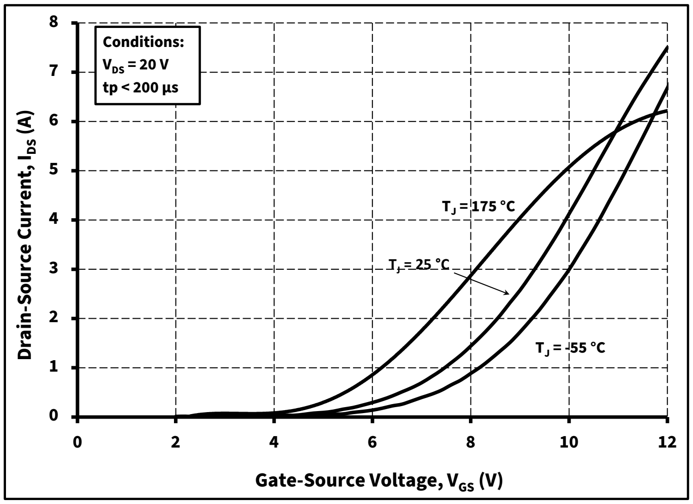


Figure 7. Transfer Characteristic for Various Junction Temperatures

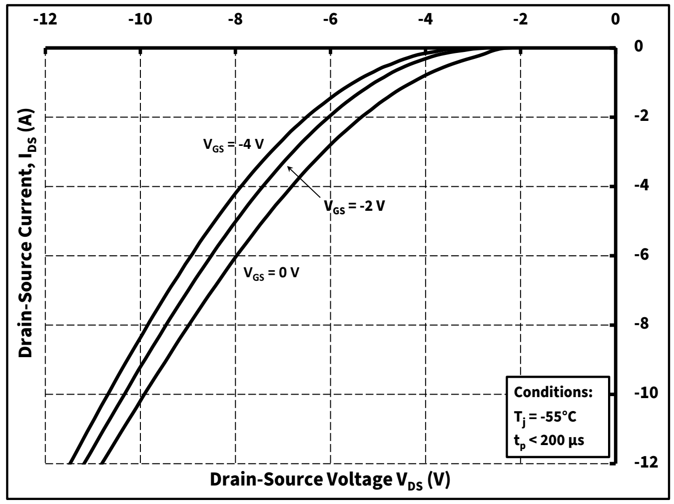


Figure 8. Body Diode Characteristic at -55 ºC

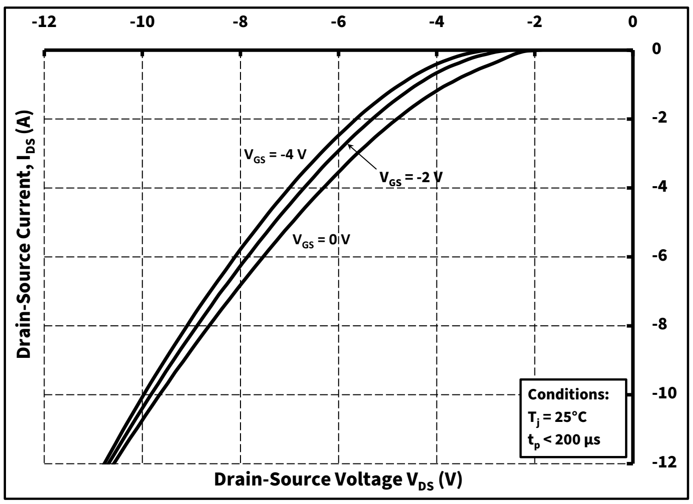


Figure 9. Body Diode Characteristic at 25 ºC

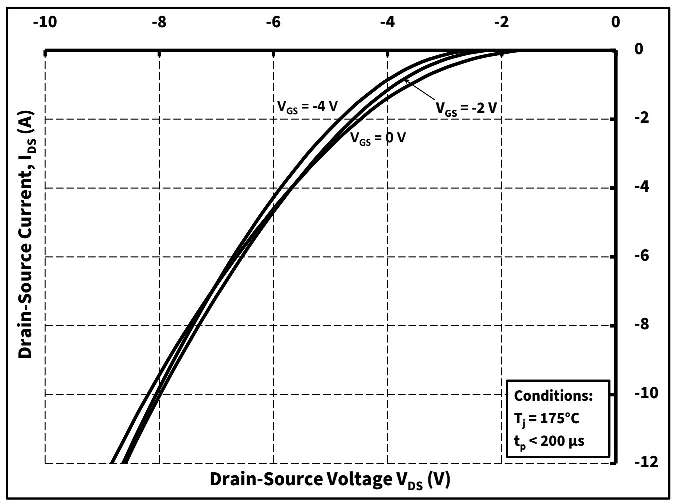


Figure 10. Body Diode Characteristic at 175 ºC

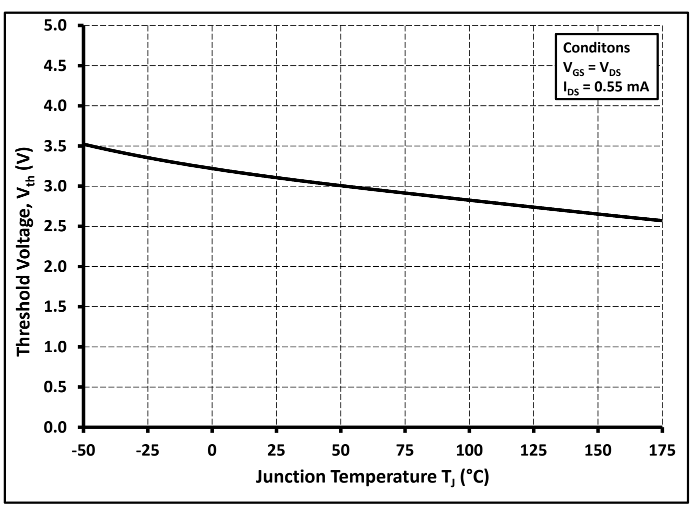


Figure 11. Threshold Voltage vs. Temperature

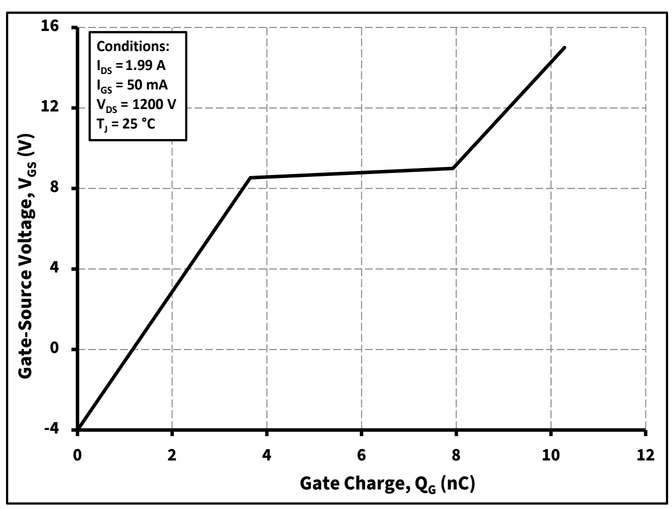


Figure 12. Gate Charge Characteristics

Typical Performance

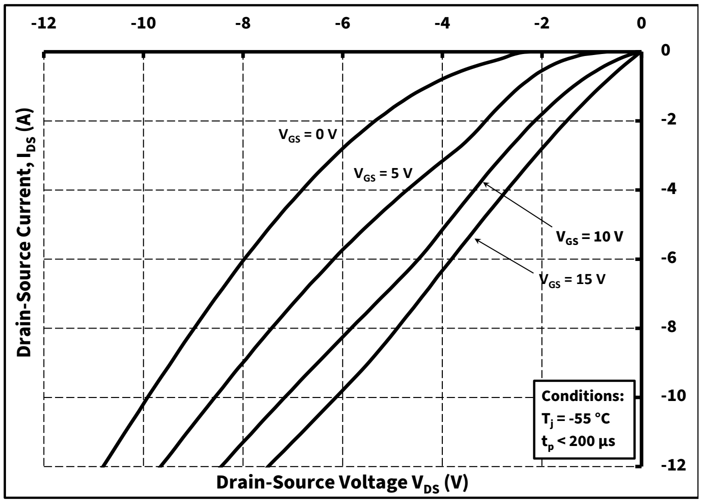


Figure 13. 3rd Quadrant Characteristic at -55 °C

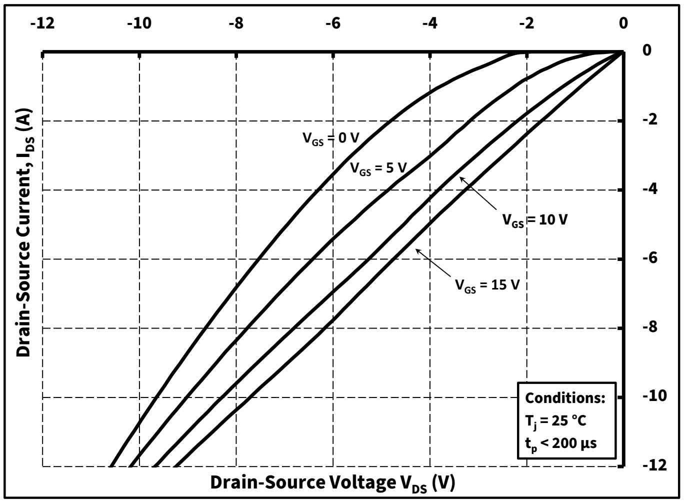


Figure 14. 3rd Quadrant Characteristic at 25 °C

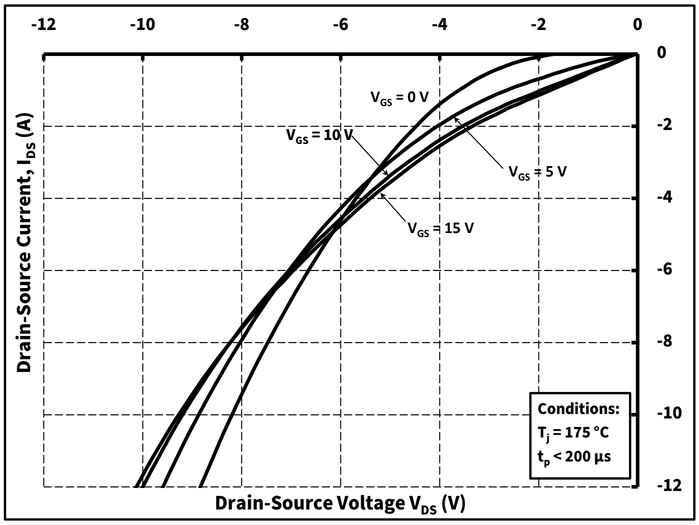


Figure 15. 3rd Quadrant Characteristic at 175 °C

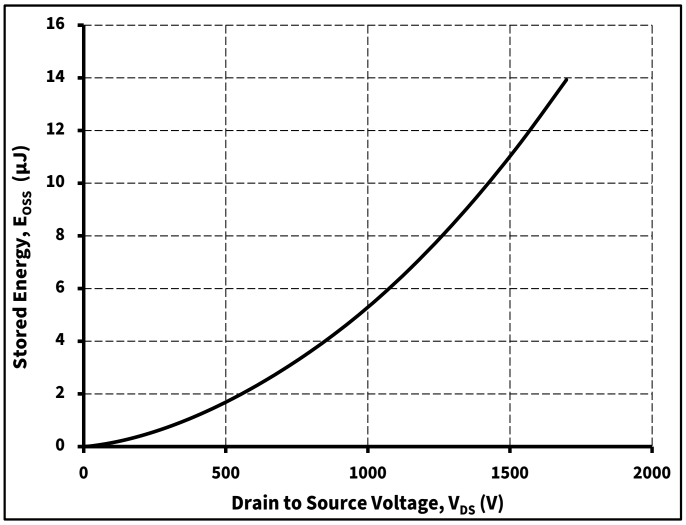


Figure 16. Output Capacitor Stored Energy

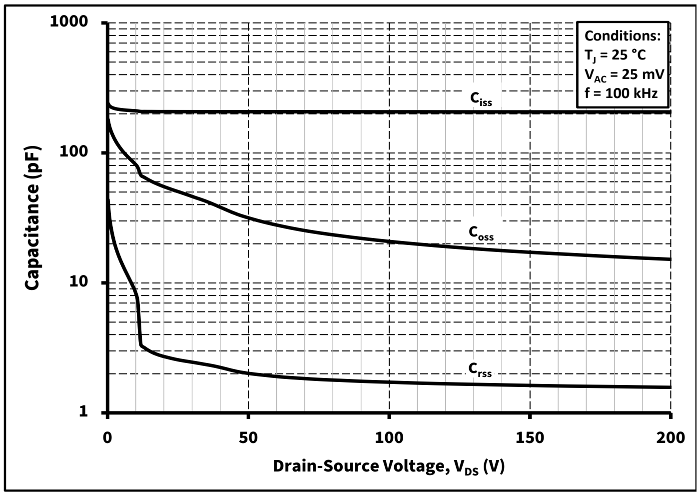


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

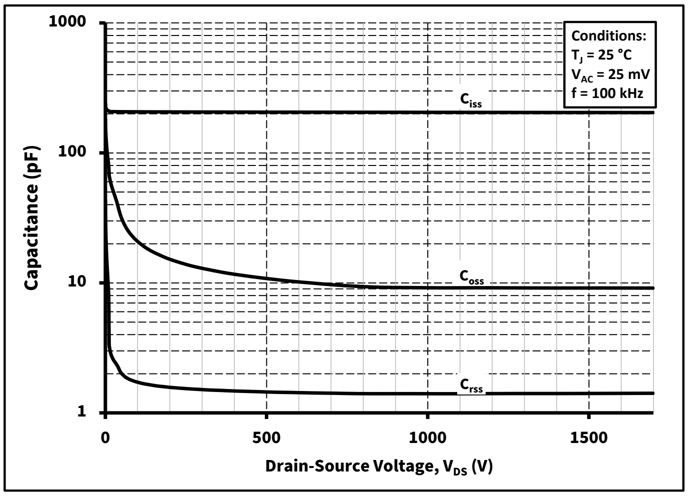


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1700V)

Typical Performance

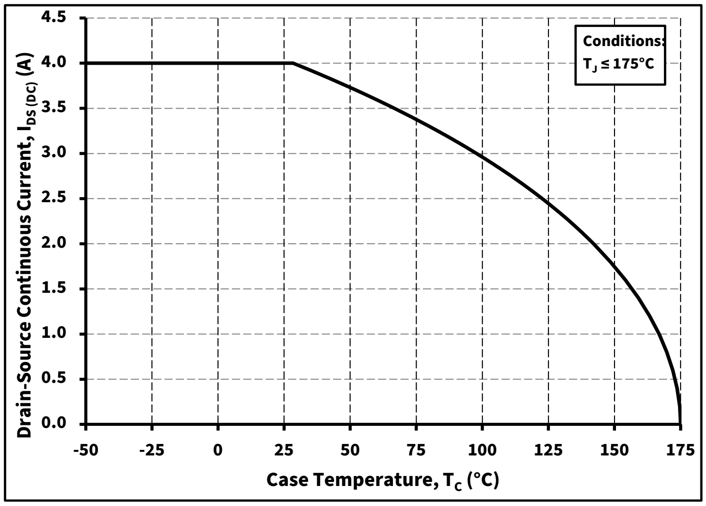


Figure 19. Continuous Drain Current Derating vs. Case Temperature

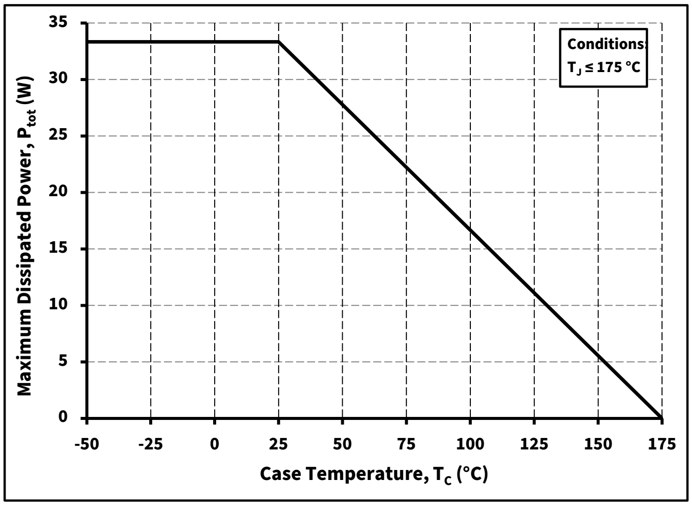


Figure 20. Max Power Dissipation vs. Case Temperature

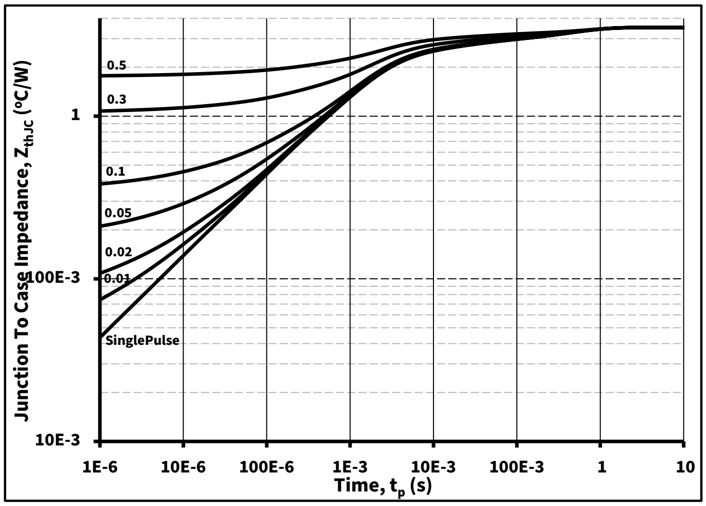


Figure 21. Transient Thermal Impedance (Junction-Case)

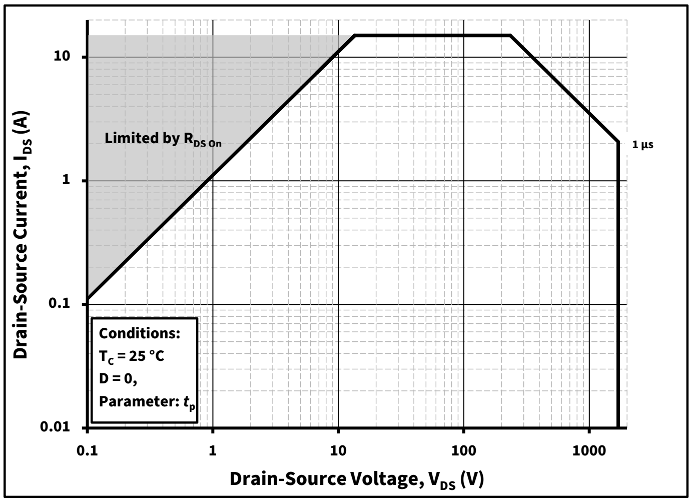


Figure 22. Safe Operating Area

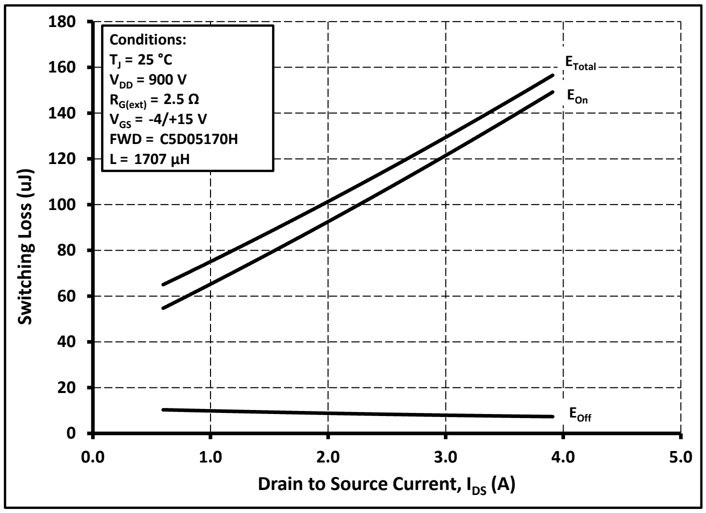


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD}=900V)

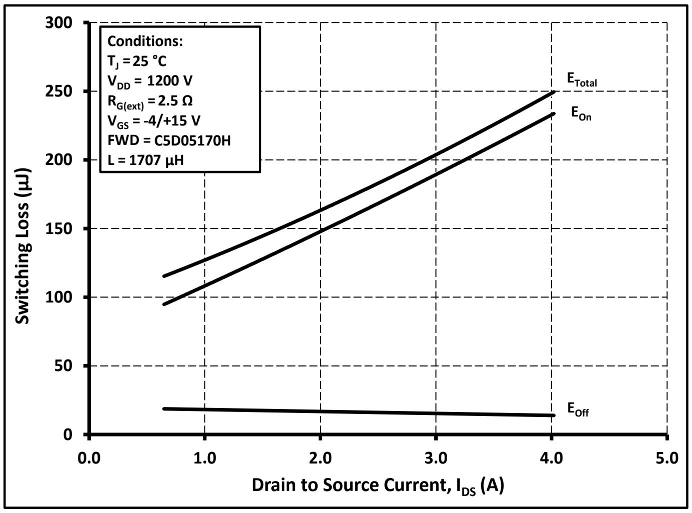


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD}=1200V)

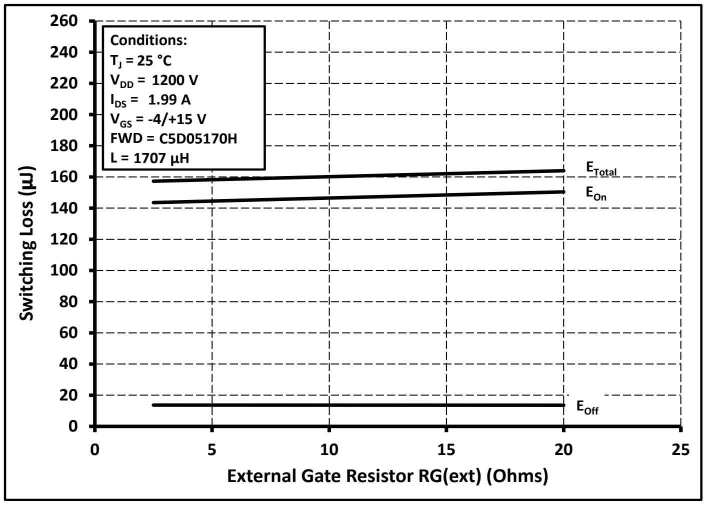


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

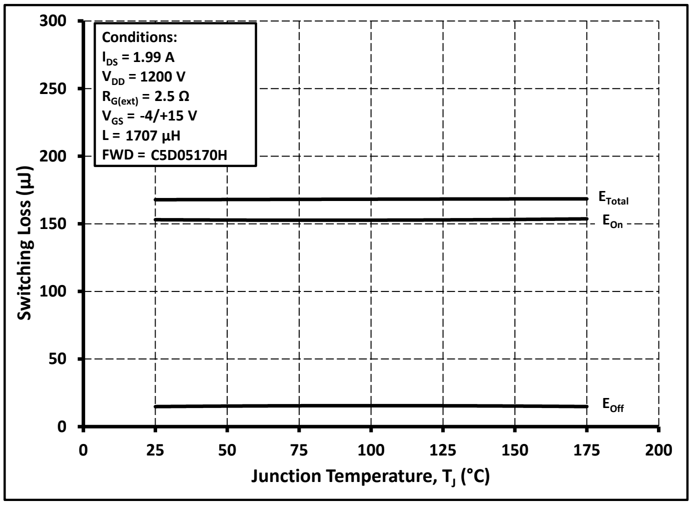


Figure 26. Clamped Inductive Switching Energy vs. Temperature

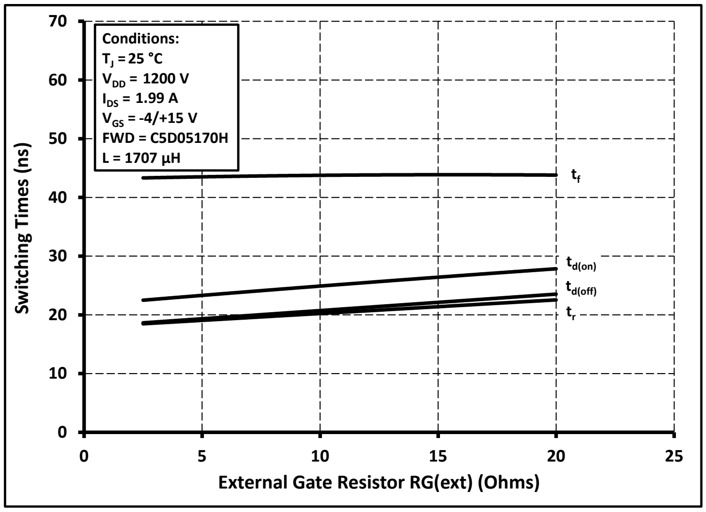


Figure 27. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

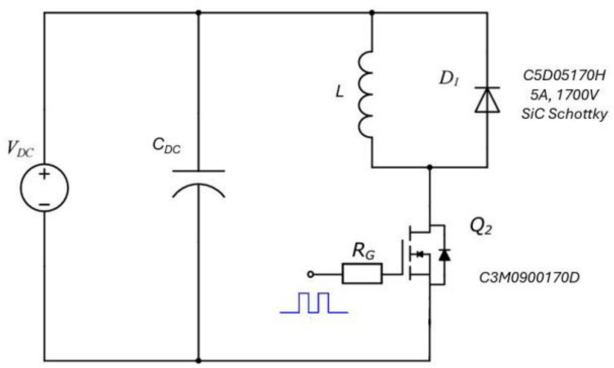
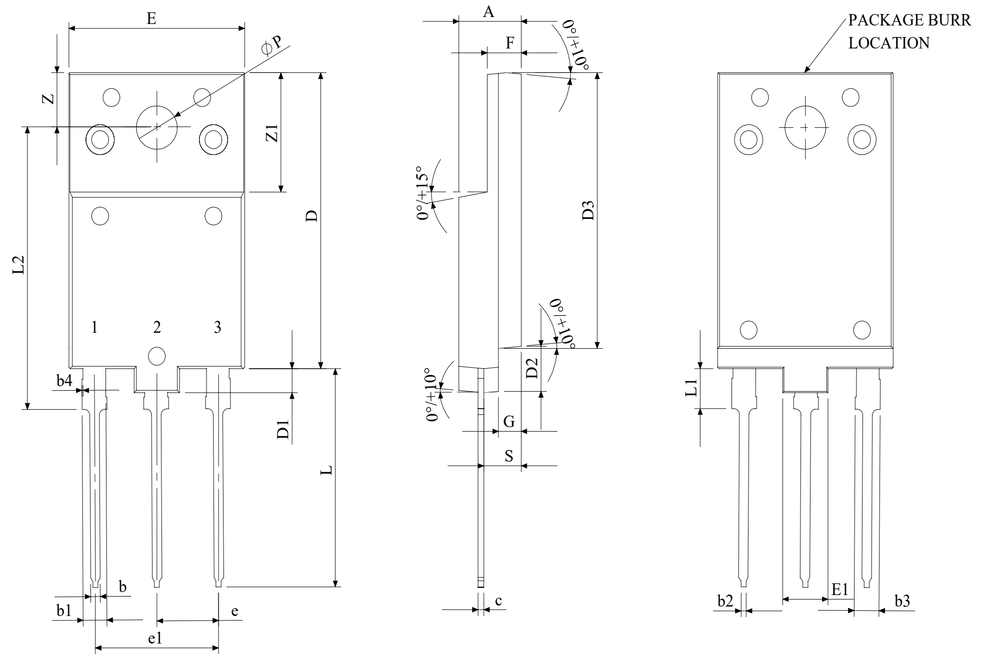


Figure 28. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	5.30	5.70
b	0.65	0.95
b1	1.81	2.19
b2	0.30	0.70
b3	1.81	2.40
b4	-	0.20
c	0.80	1.00
D	24.20	24.80
D1	1.80	2.20
D2	3.30	3.70
D3	22.65	23.25
E	15.30	15.70
E1	3.80	4.20
F	2.80	3.20
e	5.45 BSC	
e1	10.30	11.50
L	19.00	19.60
L1	4.20	4.80
L2	24.20	24.80
P	3.40	3.80
Z	4.30	4.70
Z1	9.70	10.30
G	1.80	2.20
S	3.10	3.50

1	GATE
2	DRAIN
3	SOURCE

NOTE:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

TITLE: PACKAGE OUTLINE DRAWING: TO-3PF-3L

Date: 1/22/25

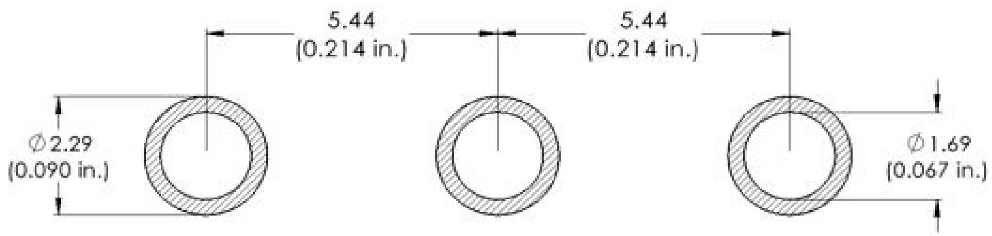
REVISION NO. 01

A4

PRD 09121 | SCALE:1:1 | SHEET 1 OF 1

Recommended Solder Pad Layout

All dimensions in mm



Revision history

Document Version	Date of release	Descriptiion of changes
1	February 2025	Initial release

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REACh Compliance

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