Single-Inductor Six-Output PMIC for Rader and Camera Modules

1 General Description

The BV8002 is a highly integrated power solution with a 4-ouput SIMO buck converter and 2 LDOs to generate six positive output voltages with only a inductor. The PMIC can achieve much smaller PCB area and lower BOM cost than traditional multi-channel PMIC which needs more inductors. The overall power conversion efficiency of BV8002 is also comparable with that of a traditional PMIC integrating several dc/dc converters and LDOs. The output voltages and power sequence of the voltage output rails can be adjusted by IIC interface and be preset by built-in NVM based on application requirement. Its normal operating input voltage range is 4.5V to 17V. Therefore, BV8002 is an optimized power solution for Rader and Automotive Camera Module. BV8002 is available in the Wettable QFN-24P 4mmx4mm package.

2 Features

- Input Voltage Range 4.5 to 17V
- SIMO Buck Converter output
  - The Highest Output Voltage VO0 Setting: 5.0V, 4.2V, 3.6V, or 3.3V. Max loading is 300mA with 5.0V as default.
  - The 1st Output Voltage VO1 Range: 0.6V to 3.6V, step is 0.1V and Max loading is 600mA with 3.3V as default.
  - The 2nd Output Voltage VO2 Range: 0.6V to 3.6V, step is 0.1V and Max loading is 1A with 1.8V as default.
  - The 3rd Output Voltage VO3 Range: 0.6V to 2.1V, step is 0.05V and Max loading is 1A with 1.5V as default
- LDO Output
  - The 4th Output Voltage VO4 Range: 0.6V to 3.6V, step is 0.1V and Max loading is 300mA with 2.8V as default.
  - The 5th Output Voltage VO5 Range: 0.6V to 3.6V, step is 0.1V and Max loading is 300mA with 1.8V as default.
- Built-in non-volatile memory (NVM) for presetting output voltages and power sequence
- Reset function with programmable delay time
- 1MHz/2.1MHz switching frequency for A/B
- Junction Temperature Reporting
- AEC-Q100 Qualified with the Following Results:
  Device Temperature Grade: –40°C to 125°C Operating Junction Temperature Range

3 Applications

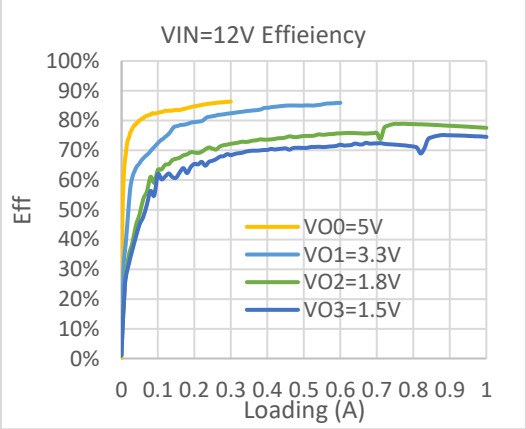
- Rader Module
- Automotive Camera Module

4 Ordering Information

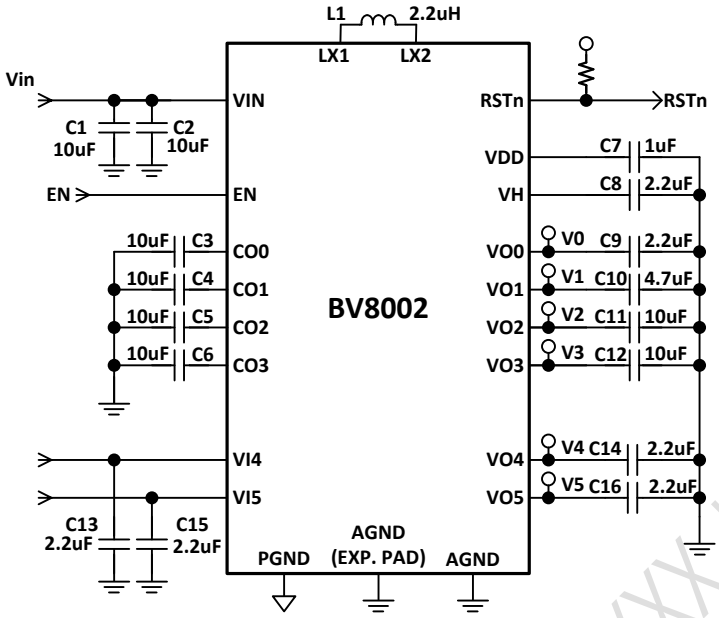
BV8002A/B-Q1

└Package Type
WQ: Wettable QFN-24P 4x4mm^2

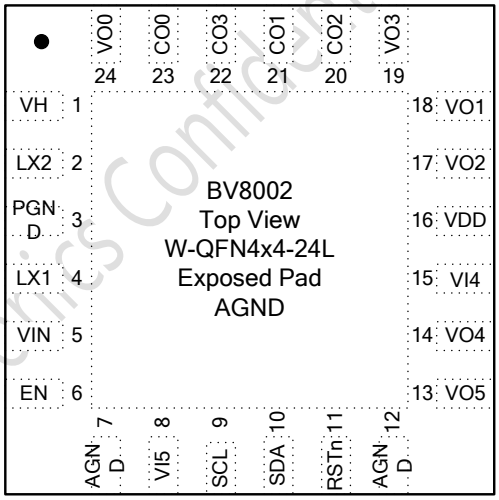
Note:
Bravotek products are RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020Package Information



5 Application Circuit



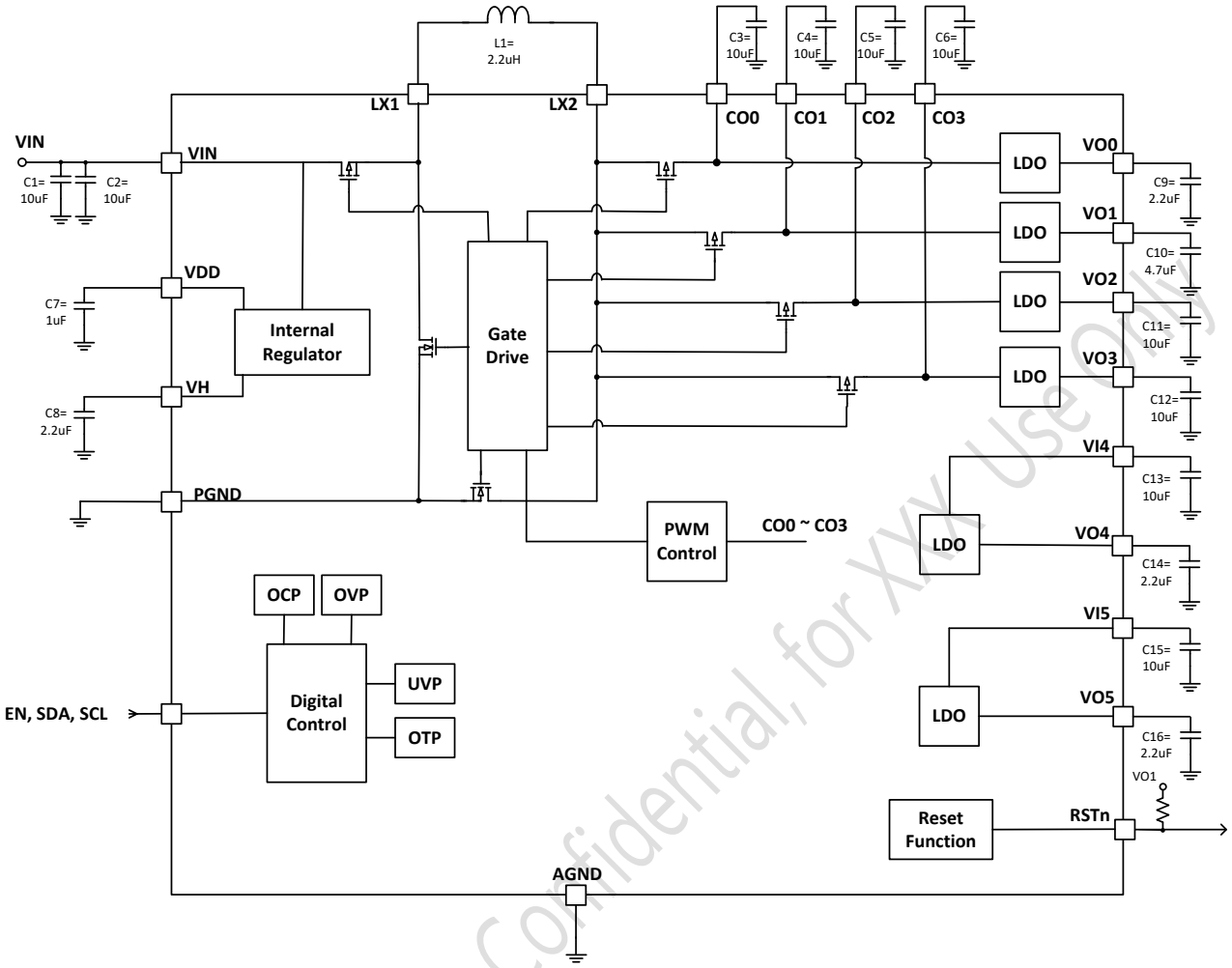
6 Pin Configuration and Function



Pin	Name	Function
1	VH	Power for internal circuit used
2	LX2	LX2 switching node for SIMO
3	PGND	Power ground
4	LX1	LX1 switching node for SIMO
5	VIN	Power Input for BV8002
6	EN	Chip enable pin
7	AGND	Analog Ground
8	VI5	LDO5 Input Power for VO5

9	SCL	IIC clock input
10	SDA	IIC data terminal
11	RSTn	Reset function
12	AGND	Analog Ground
13	VO5	LDO5 Output Power
14	VO4	LDO4 Output Power
15	VI4	LDO4 Input Power for VO4
16	VDD	Power for internal circuit used
17	VO2	LDO2 Output Power
18	VO1	LDO1 Output Power
19	VO3	LDO3 Output Power
20	CO2	SIMO 2nd Output Power
21	CO1	SIMO 1st Output Power
22	CO3	SIMO 3rd Output Power
23	CO0	SIMO Highest Output Power
24	VO0	LDO0 Output Power

7 Functional Block Diagram



8 Absolute Maximum Ratings

- Supply Input Voltage: EN, VIN, LX1 to ANGD, PGND.....-0.3V to 25V
- CO0, CO1, CO2, CO3, VO0, VO1, VO2, VO3 to AGND, PGND .....-0.3V to 6.0V
- VI4, VI5, LX2, VO4, VO5 to AGND, PGND .....-0.3V to 6.0V
- Power Dissipation, PD@ TA=25°C
  Wettable QFN-24P 4mmx4mm .....TBDW
- Package Thermal Resistance
  Wettable QFN-24P 4mmx4mm .....TBD°C/W
- Lead Temperature (Soldering, 10sec.) .....260°C
- Junction Temperature .....150°C
- Storage Temperature .....-65°C to 150°C
- ESD Susceptibility
  HBM(Human Body Model) 2KV

9 Recommended Operating Conditions

- Supply Input Voltage ..... 4.5v to 17V
- Junction Temperature Range .....-40°C to 125°C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The device is not guaranteed to function outside its recommended operating conditions.

10 Components Selection

10.1 Inductor

Reference	Value	Component supplier	Package	Isat / DCR
L1	2.2uH	NRS5030T2R2NMGJ	5mm x 5mm x 3.1mm	3.5A / 35mΩ
L1	2.2uH	DFE252012F-2R2M	2.5mm x 2mm x 1.2mm	3.3A / 82mΩ

10.2 Capacitor

Reference	Value	Component supplier	Package
C1, C2	10uF/25V	TMK107BBJ106MA-T	0603
C3, C4, C5, C6, C11, C12, C13, C16	10uF/10V	LMK107BBJ106MALT	0603
C7, C10	4.7uF/10V	LMK107BJ475MAHT	0603
C8, C9, C14, C16	2.2uF/10V	LMK107B7225KA-TR	0603

11 Electrical Characteristics

V_{IN}=12V, VO0=5V, VO1=3.3V, VO2=1.8V, VO3=1.5V, VO4=2.8V, VO5=1.8V, T_A=25°C, unless otherwise specified.						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Power Supply						
Input Supply Voltage	V_{IN}		4.5	12	17	V
Quiescent Current	I_Q		-	3		mA
Shutdown Current	I_{SHDN}		-	20		μA
Under-Voltage Lockout Threshold	V_{UVLOH}	VIN Rising	--	4.2	4.3	V
	V_{UVLOL}	VIN falling	2.7	2.8	2.9	V
Thermal Shutdown	T_{SD}		--	160	--	˚C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	25	--	˚C
EN Threshold Voltage	V_{IH}			1.2		V
	V_{IL}			0.4		V
SIMO						
Switching Frequency	F_{SW}	BV8002A		1		MHz
		BV8002B		2.1		MHz
Over Current Protection	I_{OCP}		2.4	3	3.6	A
VO0 LDO						
Output Voltage Range	V_{VO0_RANGE}		-	5	-	V
Output Voltage Accuracy	V_{VO0_ACC}		-2	-	2	%
Output Current Capability	I_{VO0}		-	0.3	-	A
Current Limit	I_{OC}		0.31	0.4	0.49	A
Line Regulation	V_{VO0_LINE}	V_{IN}=6.5 to 17V, I_{VO0}=10mA	-10	-	10	mV
Load Regulation	V_{VO0_LOAD}	I_{VO0} = 0 to 250mA	-	10	-	mV
Dropout Voltage	V_{VO0_DROP}		100			mV
SS Time	T_{SS_VO0}			300		uS
Under Voltage Protection				50		%
UVP Detection Time				10		us
VO1 LDO						
Output Voltage Range	V_{VO1_RANGE}		0.6	3.3	3.6	V
Output Voltage Accuracy	V_{VO1_ACC}		-2	-	2	%
Output Current Capability	I_{VO1}		-	0.6	-	A
Current Limit	I_{OC}		0.61	0.75	0.89	A
Line Regulation	V_{VO1_LINE}	V_{IN}=4.5 to 17V, I_{VO1}=10mA	-10	-	10	mV

Load Regulation	V_{VO1_LOAD}	I_{VO1} = 0 to 250mA	-	10	-	mV
Dropout Voltage	V_{VO1_DROP}		100			mV
SS Time	T_{SS_VO1}			300		uS
Under Voltage Protection				50		%
UVP Detection Time				10		us
VO2 LDO						
Output Voltage Range	V_{VO2_RANGE}		0.6	1.8	3.6	V
Output Voltage Accuracy	V_{VO2_ACC}		-2	-	2	%
Output Current Capability	I_{VO2}		-	1	-	A
Current Limit	I_{OC}		1.01	1.25	1.49	A
Line Regulation	V_{VO2_LINE}	V_{IN}=4.5 to 17V, I_{VO2}=10mA	-10	-	10	mV
Load Regulation	V_{VO2_LOAD}	I_{VO2} = 0 to 250mA	-	10	-	mV
Dropout Voltage	V_{VO2_DROP}		100			mV
SS Time	T_{SS_VO2}			300		uS
Under Voltage Protection				50		%
UVP Detection Time				10		us
VO3 LDO						
Output Voltage Range	V_{VO3_RANGE}		0.6	1.5	2.1	V
Output Voltage Accuracy	V_{VO3_ACC}		-2	-	2	%
Output Current Capability	I_{VO3}		-	1	-	A
Current Limit	I_{OC}		1.01	1.25	1.49	A
Line Regulation	V_{VO3_LINE}	V_{IN}=4.5 to 17V, I_{VO3}=10mA	-10	-	10	mV
Load Regulation	V_{VO3_LOAD}	I_{VO3} = 0 to 250mA	-	10	-	mV
Dropout Voltage	V_{VO3_DROP}		100			mV
SS Time	T_{SS_VO3}			300		uS
Under Voltage Protection				50		%
UVP Detection Time				10		us
VO4 LDO						
Input Voltage Range	V_{I4}		1.5		5.5	V
Output Voltage Range	V_{VO4_RANGE}		0.6	2.8	3.6	V
Output Voltage Accuracy	V_{VO4_ACC}		-2	-	2	%
Output Current Capability	I_{VO4}		-	0.3	-	A
Current Limit	I_{OC}		0.31	0.4	0.49	A
Line Regulation	V_{VO4_LINE}	V_{IN}=4.5 to 17V, I_{VO3}=10mA	-10	-	10	mV
Load Regulation	V_{VO4_LOAD}	I_{VO3} = 0 to 250mA	-	10	-	mV

Dropout Voltage	V_{VO4_DROP}		100			mV
SS Time	T_{SS_VO3}			300		uS
Under Voltage Protection				50		%
UVP Detection Time				10		us
VO5 LDO						
Input Voltage Range	V_{I5}		1.5		5.5	V
Output Voltage Range	V_{VO5_RANGE}		0.6	1.8	3.6	V
Output Voltage Accuracy	V_{VO5_ACC}		-2	-	2	%
Output Current Capability	I_{VO5}		-	0.3	-	A
Current Limit	I_{OC}		0.31	0.4	0.49	A
Line Regulation	V_{VO5_LINE}	V_{IN}=4.5 to 17V, I_{VO3}=10mA	-10	-	10	mV
Load Regulation	V_{VO5_LOAD}	I_{VO3} = 0 to 250mA	-	10	-	mV
Dropout Voltage	V_{VO5_DROP}		100			mV
SS Time	T_{SS_VO5}			300		uS
Under Voltage Protection				50		%
UVP Detection Time				10		us
Reset						
Reset Detect Delay		UVLOL to Reset pull low		10		us
Reset Input Rising Delay	Trst	UVLOH to Reset pull High		32		ms
Reset pull low Resistance				TBD		ohm
IIC Interface						
Logic-Input Low Voltage	V_{IL}	SDA, SCL			1	V
Logic-Input High Voltage	V_{IH}	SDA, SCL	2			V
SCL Frequency	f_{CLK}				400	kHz
SDA, SCL Input Leakage Current			-2		2	uA
SDA_ACK ON Voltage	V_{ACK}	I_{SDA}=3mA			0.4	V
SCL High Period	t_{HIGH}		0.3			us
SCL Low Period	t_{LOW}		0.4			us
SCL Rising Time	t_R				0.12	us
SCL Fall Time	t_F				0.12	us
Start Condition Hold Time			0.25			us
Start Condition Setup Time			0.25			us
SDA Hold Time			50			ns
SCL Hold Time			50			ns
ACK Delay Time					0.35	us

ACK Hold Time				0.1		us
Stop Condition Setup Time			0.25			us
Bus Free Time			0.5			us

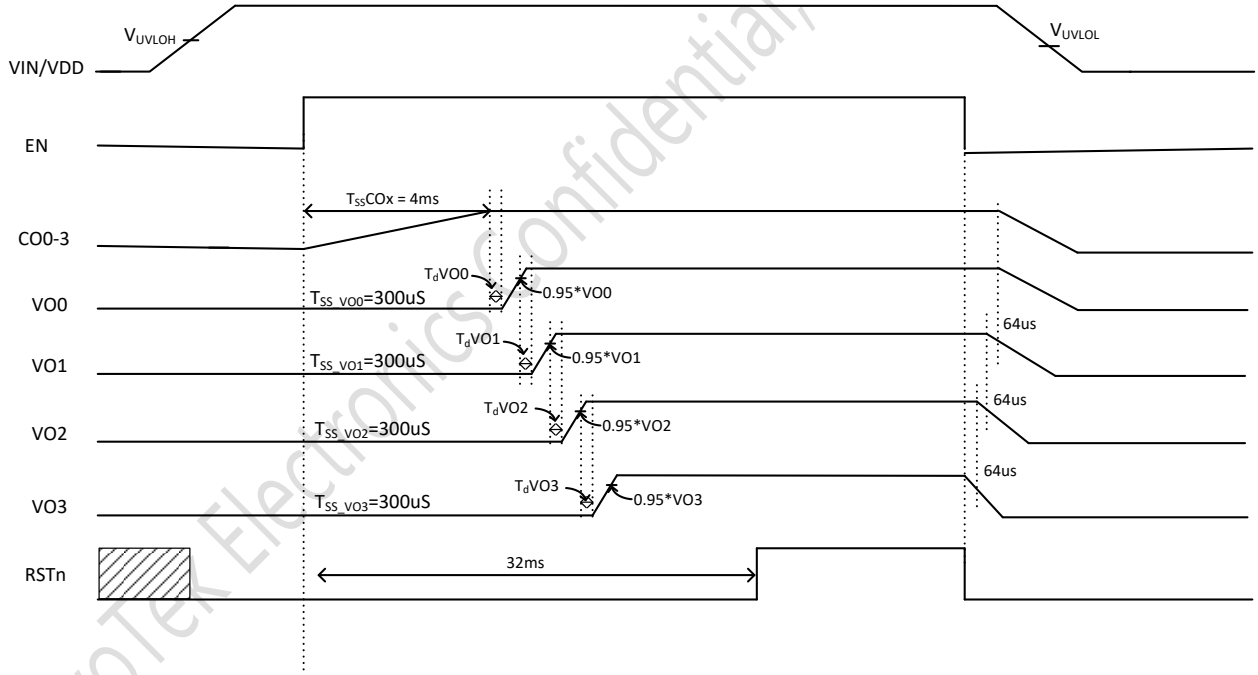
12 Detail Descriptions

The BV8002 operates with a seven-switch SIMO converter topology to generation four positive output voltage with a single inductor, which also integrates 2 LDOs. The IC is the best solution to driving Automotive Camera or Radar module, etc. The output voltage (VO0 to VO5) can be set by Register, detail description can be reference at I2C Register Map.

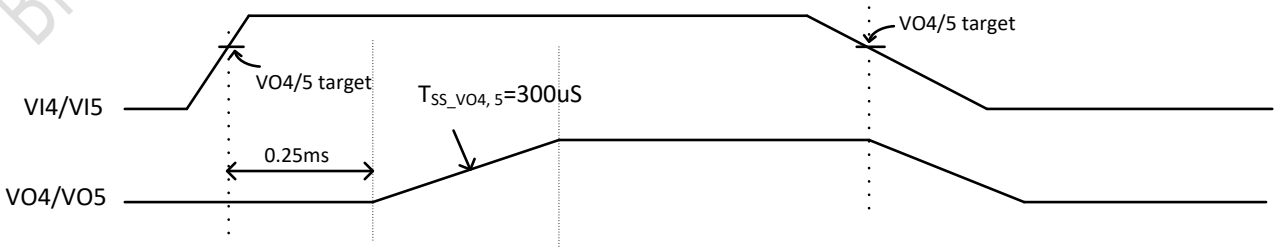
BV8002 provides the Under-Voltage Protection (UVP), Over-Temperature Protection (OTP), Over-Voltage Protection (OVP) and Over-Current Protection (OCP).

12.1 Power Sequence

12.1.1 VO0 to VO3 power on off sequence



12.1.2 VO4, and VO5 power on off sequence



12.2 Protection Functions

12.2.1 Under-Voltage Protection

Each output channel VO0-VO5 is protected against short circuit either to GND or against the other output by Under-Voltage Protection (UVP). The IC will enter shutdown mode when the output voltage (VOx) is under the limit level (50% and keep 10us). The IC can only restart normal operation after re-power on.

The four SIMO output terminals CO0-CO3 shall have specified values as V(COn)>=V(COn+1). The IC will into shutdown mode when V(COn)-V(COn+1) <= -0.3V and keep 1us.

12.2.2 Over-Temperature Protection

The BV8002 includes an over temperature protection circuit to prevent overheating. All outputs of the IC, excluding VDD and VH, will be disabled and discharged to ground level when the junction temperature exceeds 160°C. Once the Junction temperature cools down to approximately 135°C, IC will automatically re-soft-start and go into a normal operation.

12.2.3 VIN Over-Voltage Protection

The device will monitor the VIN voltage. The IC will disable the VIN exceeds 19V. The output voltages will recovery automatic after VIN voltage drop to under 18V.

12.2.4 Over-Current Protection

The BV8002 includes a cycle-by-cycle current limit function which monitor the inductor current during Phase 1 period. The power switch will be forced off to avoid large current damage IC when the current is over the limit level 3A.

Each output channel VO0-VO5 provides over-current detection. The current limit is a fixed value based on their current capability. If any channel's current limit is exceeded for longer than 64ms, the IC will enter shutdown mode.

12.2.5 Shut-Down Mode

Once the IC enters shutdown mode, all output channels will be discharged to ground with specified power off sequence. The IC can enter normal operation by re-power-on Vin. After the IC re-enter into normal operation, all output channels will operate again with the specified power on sequence.

12.2.6 Hiccup Mode

Once the IC enters Hiccup mode, all output channels will be discharged to ground with specified power off sequence. The IC can enter normal operation automatically by 250ms delay. After the IC re-enter into normal operation, all output channels will operate again with the specified power on sequence.

12.3 IIC Interface

12.3.1 I2C Device Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-Bit Device Slave ID	0x74	1110100
Write Address	0xE8	11101000
Read Address	0xE9	11101001

12.3.2 I2C Register Map

IIC Address	Port Name	Default Value	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
0x00	VO0	0x83	VO0EN	x	VDO0<1>	VDO0<0>	X	X	VO0S<1>	VO0S<0>
0x01	VO1	0xBB	VO1EN	VDO1<1>	VDO1<0>	VO1S<4>	VO1S<3>	VO1S<2>	VO1S<1>	VO1S<0>
0x02	VO2	0xAC	VO2EN	VDO2<1>	VDO2<0>	VO2S<4>	VO2S<3>	VO2S<2>	VO2S<1>	VO2S<0>
0x03	VO3	0xB2	VO3EN	VDO3<1>	VDO3<0>	VO3S<4>	VO3S<3>	VO3S<2>	VO3S<1>	VO3S<0>
0x04	VO4	0x96	VO4EN	tDVO4	x	VO4S<4>	VO4S<3>	VO4S<2>	VO4S<1>	VO4S<0>
0x05	VO5	0x8C	VO5EN	tDVO5	x	VO5S<4>	VO5S<3>	VO5S<2>	VO5S<1>	VO5S<0>
0x06	NA	NA	Reserved							
0x07	TimS	0x10	tSSOSCm<1>	tSSOSCm<0>	tSSOSC<1>	tSSOSC<0>	tDVO3	tDVO2	tDVO1	tDVO0
0x08	PwrSq	0x40	tRST<1>	tRST<0>	XAOS<1>	XAOS<0>	x	PwrSqS<2>	PwrSqS<1>	PwrSqS<0>
0x09	NA	NA	Reserved							
0x0A	NA	NA	Reserved							
0x0B	VO6MISC	0x00	Reserved				HCCPEn	Reserved		

Note: 0x06 is reserved and can be not used by user mode.

I2C Register Descriptions

Table. VO0 (0x00)

Address	0x00							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	VO0EN	x	VDO0<1>	VDO0<0>	X	X	VO0S<1>	VO0S<0>
VO0EN	VO0EN=0, Disable VO0 VO0EN=1, Enable VO0							
VDO0<1:0>	Dropout voltage from CO0 to VO0 VDO0<1:0>= {11, 10, 01, 00} = {0.25V, 0.2V, 0.15V, 0.1V}							
VO0S<1:0>	VO0 output voltage setting VO0S<1:0>= {11, 10, 01, 00} = {5V, 4V, 3.6V, 3.3V}							

Table. VO1 (0x01)

Address	0x01							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	VO1EN	VDO1<1>	VDO1<0>	VO1S<4>	VO1S<3>	VO1S<2>	VO1S<1>	VO1S<0>
VO1EN	VO1EN=0, Disable VO1 VO1EN=1, Enable VO1							
VDO1<1:0>	Dropout voltage from CO1 to VO1 VDO1<1:0>= {11, 10, 01, 00} = {0.2V, 0.15V, 0.1V, 0.05V}							
VO1S<4:0>	VO1 output voltage setting VO1S<4:0>= 5'h00~5'h1E= 0.6V~3.6V with 0.1V step							

00h	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**
0.6V	0.7V	0.8V	0.9V	1.0V	1.1V	1.2V	1.3V
08h	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**
1.4V	1.5V	1.6V	1.7V	1.8V	1.9V	2.0V	2.1V
10h	**11h**	**12h**	**13h**	**14h**	**15h**	**16h**	**17h**
2.2V	2.3V	2.4V	2.5V	2.6V	2.7V	2.8V	2.9V
18h	**19h**	**1Ah**	**1Bh**	**1Ch**	**1Dh**	**1Eh**	**1Fh**
3.0V	3.1V	3.2V	3.3V	3.4V	3.5V	3.6V	OFF

Table. VO2 (0x02)

Address	0x02							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	VO2EN	VDO2<1>	VDO2<0>	VO2S<4>	VO2S<3>	VO2S<2>	VO2S<1>	VO2S<0>
VO1EN	VO2EN=0, Disable VO2 VO2EN=1, Enable VO2							
VDO2<1:0>	Dropout voltage from CO2 to VO2 VDO2<1:0>= {11, 10, 01, 00} = {0.2V, 0.15V, 0.1V, 0.05V}							
VO2S<4:0>	VO2 output voltage setting VO2S<4:0>= 5'h00~5'h1E= 0.6V~3.6V with 0.1V step							

00h	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**
0.6V	0.7V	0.8V	0.9V	1.0V	1.1V	1.2V	1.3V
08h	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**
1.4V	1.5V	1.6V	1.7V	1.8V	1.9V	2.0V	2.1V
10h	**11h**	**12h**	**13h**	**14h**	**15h**	**16h**	**17h**
2.2V	2.3V	2.4V	2.5V	2.6V	2.7V	2.8V	2.9V
18h	**19h**	**1Ah**	**1Bh**	**1Ch**	**1Dh**	**1Eh**	**1Fh**
3.0V	3.1V	3.2V	3.3V	3.4V	3.5V	3.6V	OFF

Table. VO3 (0x03)

Address	0x03							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	VO3EN	VDO3<1>	VDO3<0>	VO3S<4>	VO3S<3>	VO3S<2>	VO3S<1>	VO3S<0>
VO3EN	VO3EN=0, Disable VO3 VO3EN=1, Enable VO3							
VDO3<1:0>	Dropout voltage from CO3 to VO3 VDO3<1:0>= {11, 10, 01, 00} = {0.2V, 0.15V, 0.1V, 0.05V}							
VO3S<4:0>	VO3 output voltage setting VO3S<4:0>= 5'h00~5'h1E= 0.6V~3.6V with 0.1V step							

00h	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**
0.6V	0.65V	0.7V	0.75V	0.8V	0.85V	0.9V	0.95V
08h	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**
1.0V	1.05V	1.1V	1.15V	1.2V	1.25V	1.3V	1.35V
10h	**11h**	**12h**	**13h**	**14h**	**15h**	**16h**	**17h**
1.4V	1.45V	1.5V	1.55V	1.6V	1.65V	1.7V	1.75V

	18h	**19h**	**1Ah**	**1Bh**	**1Ch**	**1Dh**	**1Eh**	**1Fh**
	1.8V	1.85V	1.9V	1.95V	2.0V	2.05V	2.1V	OFF

Table. VO4 (0x04)

Address	0x04							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	VO4EN	tDVO4	x	VO4S<4>	VO4S<3>	VO4S<2>	VO4S<1>	VO4S<0>
VO4EN	VO4EN=0, Disable VO4 VO4EN=1, Enable VO4							
tDVO4	Delay time from VI4(Power-Good) to VO4 tDVO4= {1, 0} = {0.25ms, 0ms}							
VO4S<4:0>	VO4 output voltage setting VO4S<4:0>= 5'h00~5'h1E= 0.6V~3.6V with 0.1V step							

00h	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**
0.6V	0.7V	0.8V	0.9V	1.0V	1.1V	1.2V	1.3V
08h	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**
1.4V	1.5V	1.6V	1.7V	1.8V	1.9V	2.0V	2.1V
10h	**11h**	**12h**	**13h**	**14h**	**15h**	**16h**	**17h**
2.2V	2.3V	2.4V	2.5V	2.6V	2.7V	2.8V	2.9V
18h	**19h**	**1Ah**	**1Bh**	**1Ch**	**1Dh**	**1Eh**	**1Fh**
3.0V	3.1V	3.2V	3.3V	3.4V	3.5V	3.6V	OFF

Table. VO5 (0x05)

Address	0x05							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	VO5EN	tDVO5	x	VO5S<4>	VO5S<3>	VO5S<2>	VO5S<1>	VO5S<0>
VO5EN	VO5EN=0, Disable VO5 VO5EN=1, Enable VO5							
tDVO5	Delay time from VI5(Power-Good) to VO5 tDVO5= {1, 0} = {0.25ms, 0ms}							
VO5S<4:0>	VO5 output voltage setting VO5S<4:0>= 5'h00~5'h1E= 0.6V~3.6V with 0.1V step							

00h	**01h**	**02h**	**03h**	**04h**	**05h**	**06h**	**07h**
0.6V	0.7V	0.8V	0.9V	1.0V	1.1V	1.2V	1.3V
08h	**09h**	**0Ah**	**0Bh**	**0Ch**	**0Dh**	**0Eh**	**0Fh**

	1.4V	1.5V	1.6V	1.7V	1.8V	1.9V	2.0V	2.1V
	10h	**11h**	**12h**	**13h**	**14h**	**15h**	**16h**	**17h**
	2.2V	2.3V	2.4V	2.5V	2.6V	2.7V	2.8V	2.9V
	18h	**19h**	**1Ah**	**1Bh**	**1Ch**	**1Dh**	**1Eh**	**1Fh**
	3.0V	3.1V	3.2V	3.3V	3.4V	3.5V	3.6V	OFF

Table. TimS (0x07)

Address	0x07							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	tSSOSCm<1>	tSSOSCm<0>	tSSOSC<1>	tSSOSC<0>	tDVO3	tDVO2	tDVO1	tDVO0
tSSOSCm	Spread Spectrum OSC modulation index tSSOSCm<1:0>= {11, 10, 01, 00} = {4, 2, 1, 0}							
tSSOSC	Spread Spectrum OSC modulation percentage tSSOSC<1:0>= {11, 10, 01, 00} = {15%, 10%, 5%, 0%}							
tDVO3	Delay time from the previous Power-Good to VO3 tDVO3= {1, 0} = {0.25ms, 0ms}							
tDVO2	Delay time from the previous Power-Good to VO2 tDVO2= {1, 0} = {0.25ms, 0ms}							
tDVO1	Delay time from the previous Power-Good to VO1 tDVO1= {1, 0} = {0.25ms, 0ms}							
tDVO0	Delay time from the previous Power-Good to VO0 tDVO0= {1, 0} = {0.25ms, 0ms}							

Table. PwrSq (0x08)

Address	0x08							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	tRST<1>	tRST<0>	XAOS<1>	XAOS<0>	x	PwrSqS<2>	PwrSqS<1>	PwrSqS<0>
tRST	nRST delay time tRST<1:0>= {11, 10, 01, 00} = {128ms, 64ms, 32ms, 16ms}							
XAOS	Power off vin trigger voltage XAOS<1:0>= {11, 10, 01, 00} = {10V, 6V, 4V, UVLO}							
PwrSqS	Here shown is power on sequence. Power off sequence is the reverse sequence of the power on one.							

PwrSq <2:0>	Power On Sequence	Power Off Sequence
3'b000	VO0 -> VO1 -> VO2 -> VO3	VO3 -> VO2 -> VO1 -> VO0

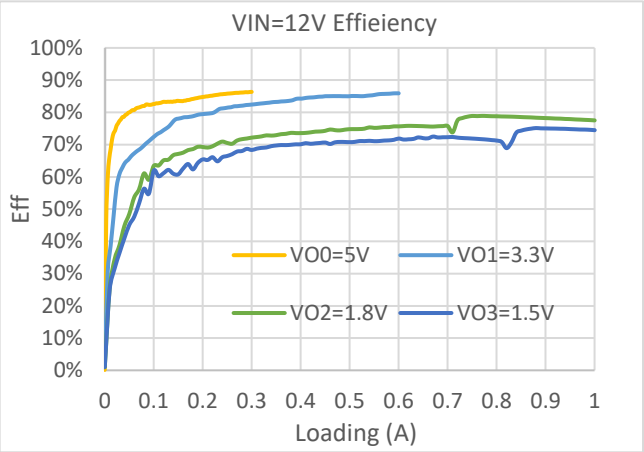
	3'b001	VO0 -> VO1 -> VO3 -> VO2	VO2 -> VO3 -> VO1 -> VO0
	3'b010	VO0 -> VO2 -> VO1 -> VO3	VO3 -> VO1 -> VO2 -> VO0
	3'b011	VO0 -> VO2 -> VO3 -> VO1	VO1-> VO3 -> VO2 -> VO0
	3'b100	VO3 -> VO2 -> VO1-> VO0	VO0 -> VO1 -> VO2 -> VO3
	3'b101	VO0 -> VO1 -> VO2 -> VO3	VO3 -> VO2 -> VO1 -> VO0
	3'b110	VO0 -> VO1 -> VO2 -> VO3	VO3 -> VO2 -> VO1 -> VO0
	3'b111	VO0 -> VO3 -> VO2 -> VO1	VO1 -> VO2 -> VO3 -> VO0

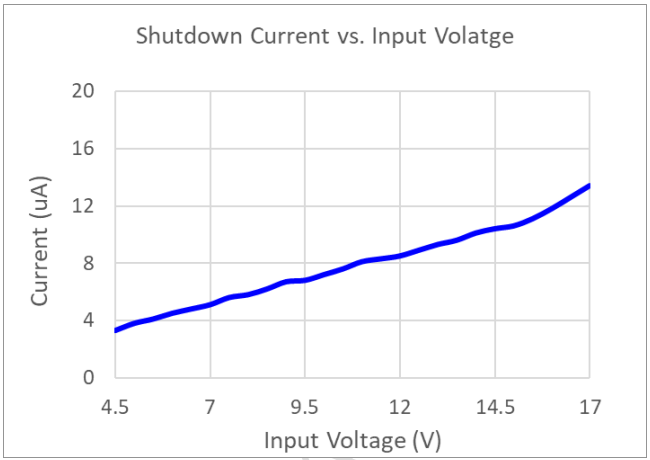
Table. DVSMISC (0x0B)

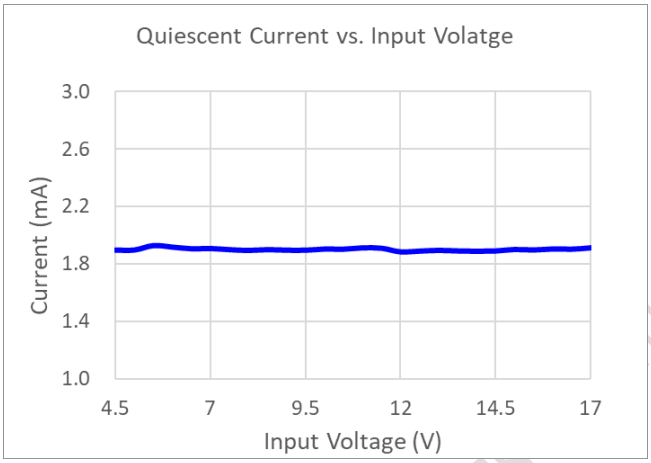
Address	0x0B							
BIT	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
NAME	x				HCCPEn	x		
HCCPEn	0: Disable (Hiccup function will be Disable) 1: Enable (Hiccup function will be Active)							

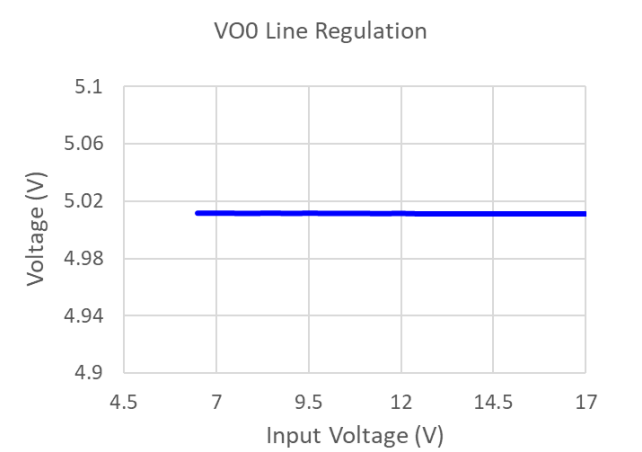
13 Typical Operating Curve

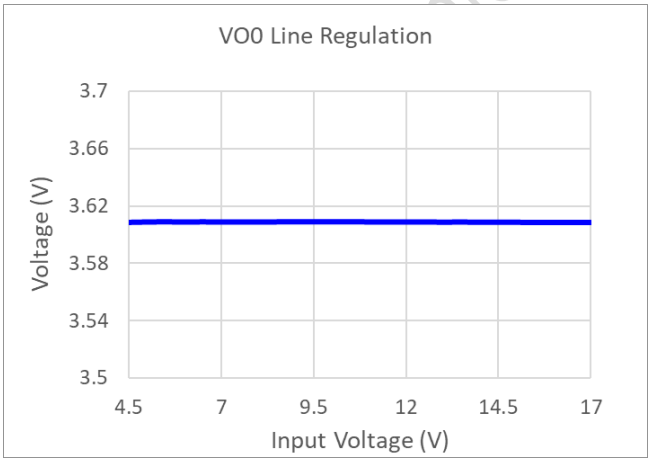
V_{IN}=12V, VO0=5V, VO1=3.3V, VO2=1.8V, VO3=1.5V, VO4=2.8V, VO5=1.8V, T_A=25°C, unless otherwise specified.

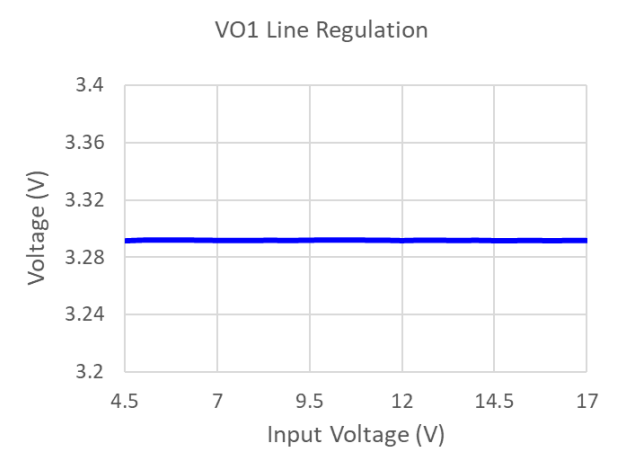


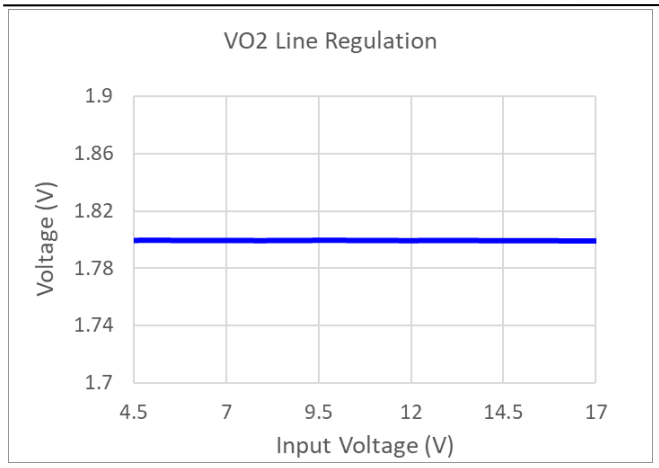


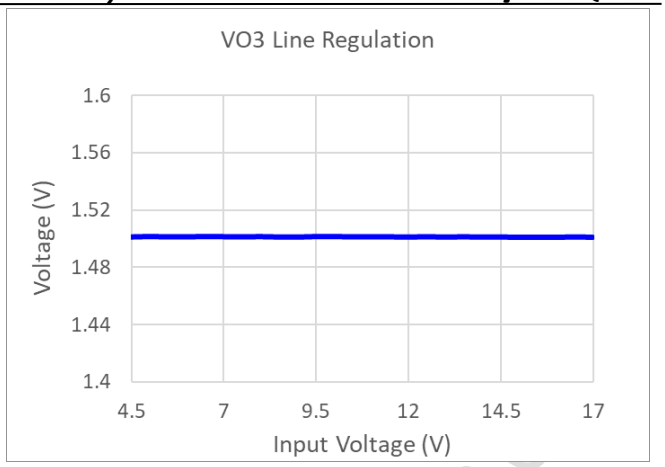


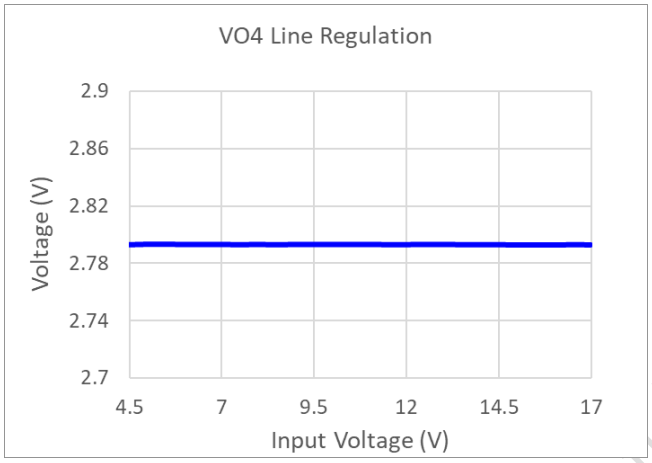


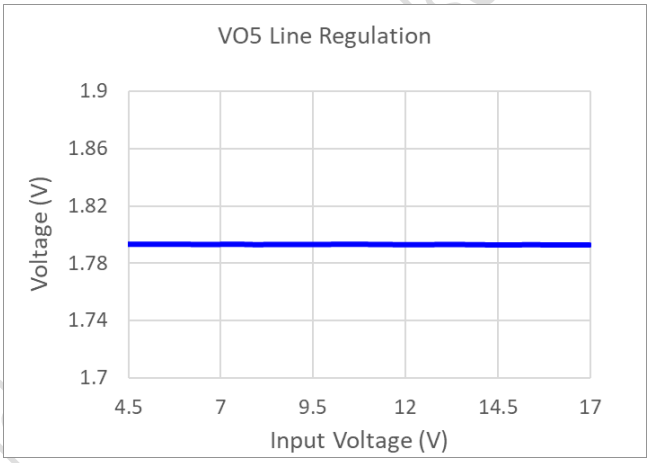


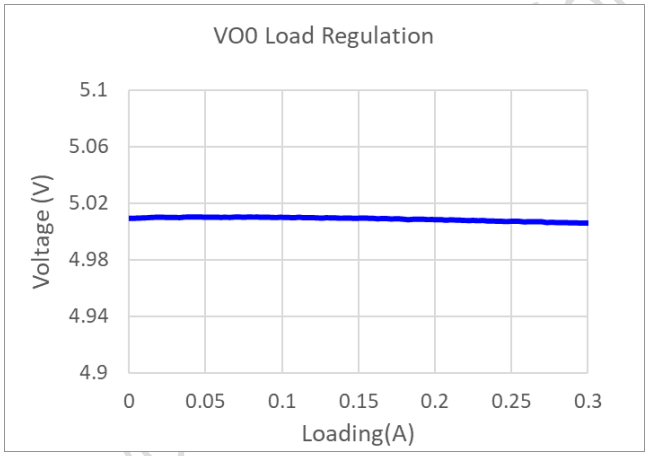


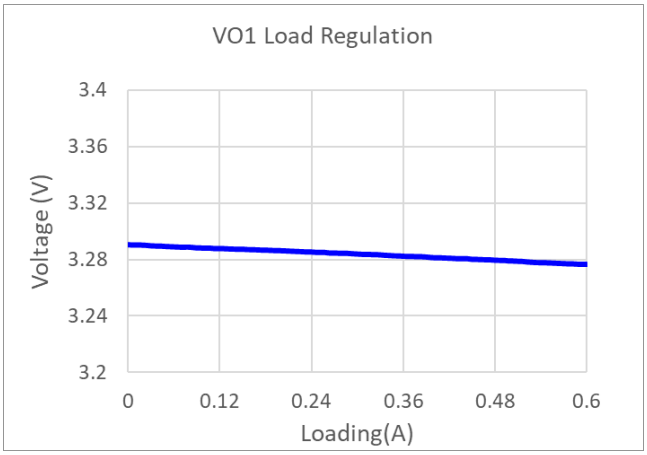


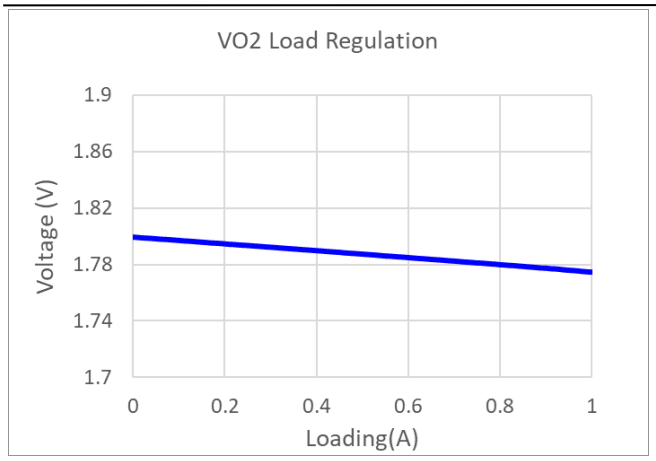


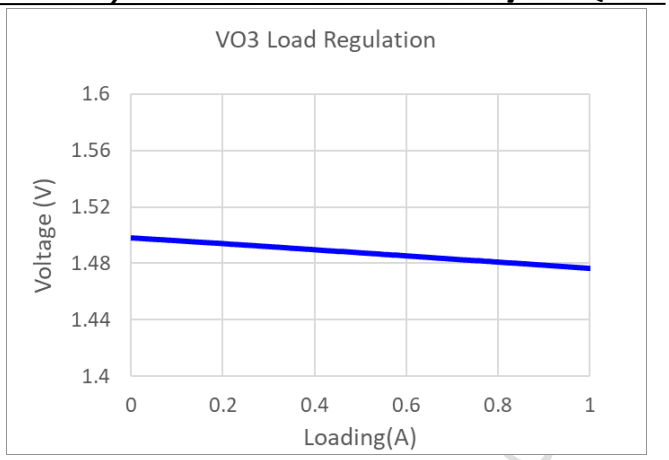


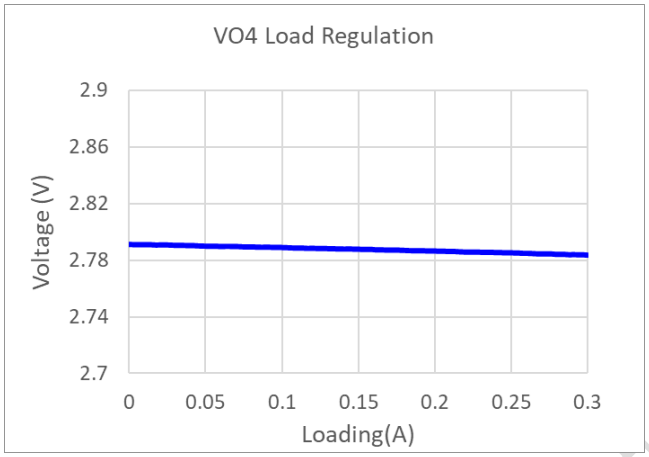


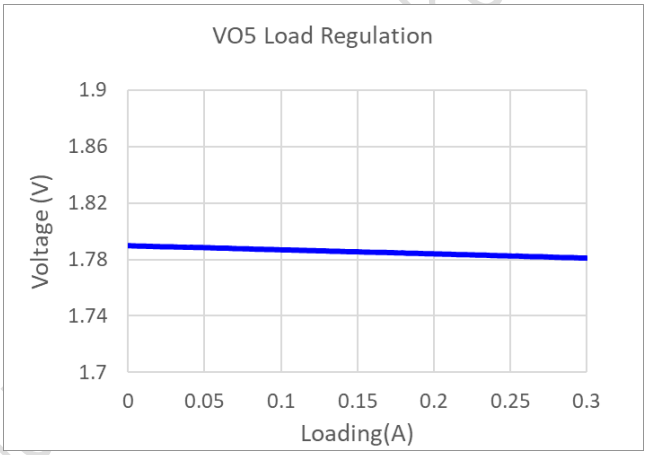


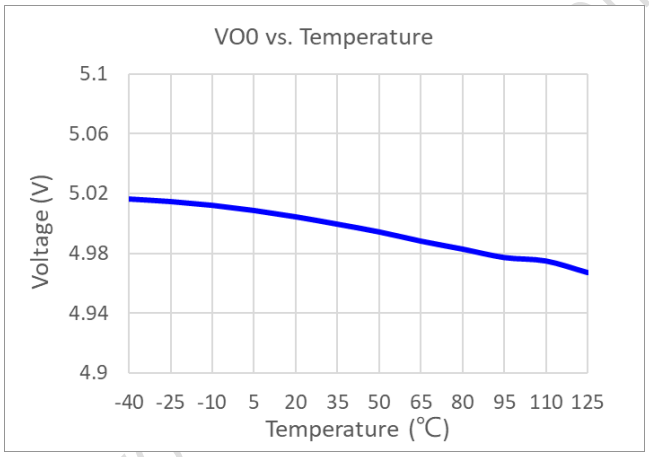


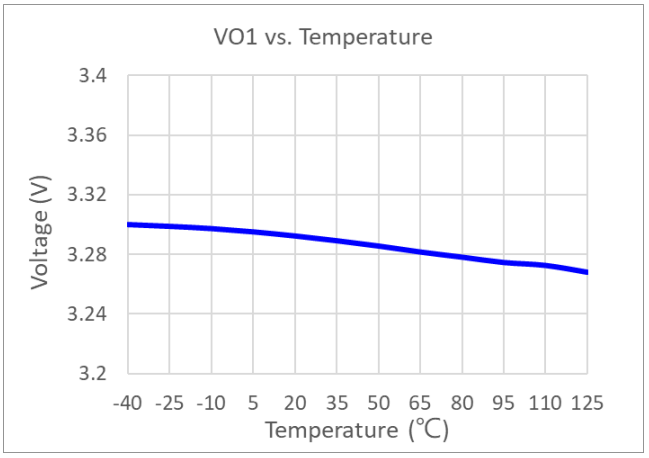


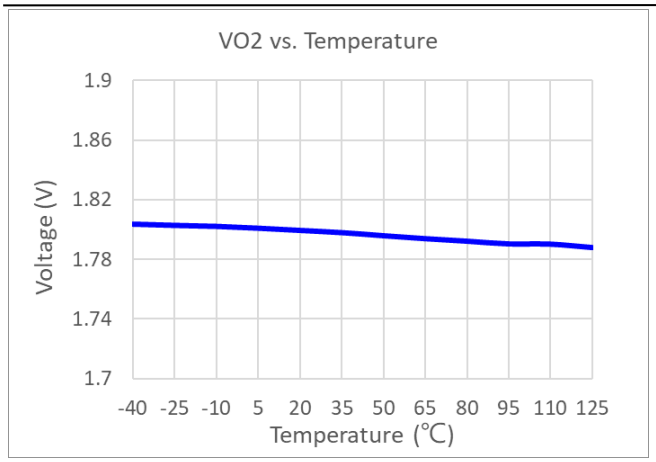


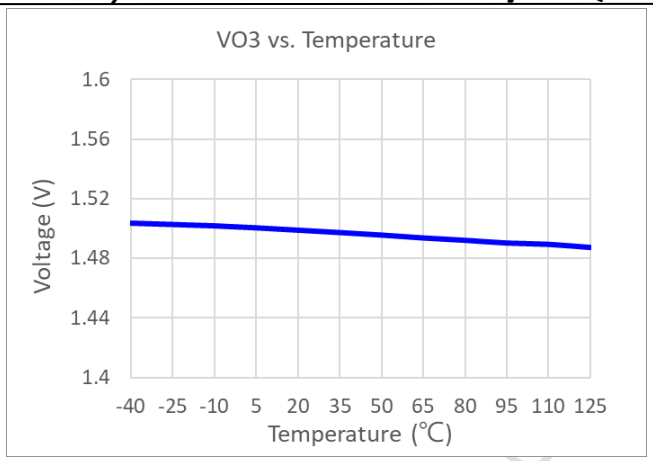


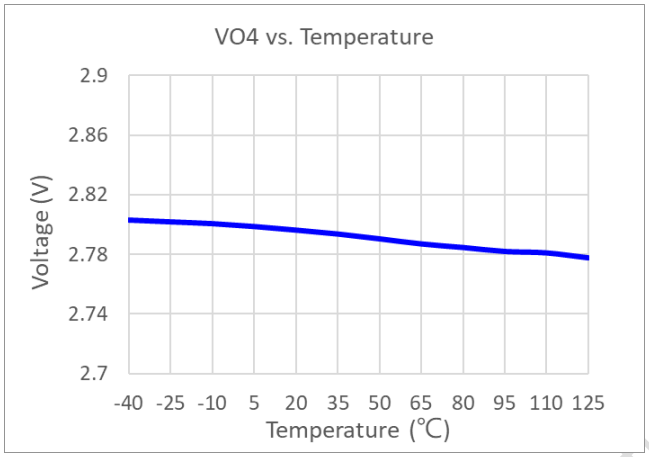


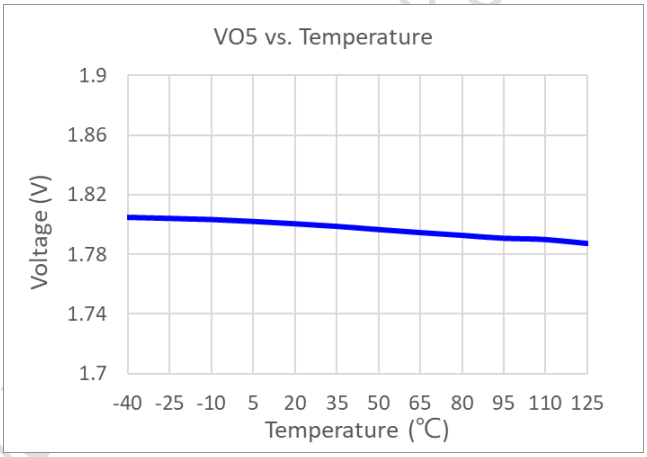


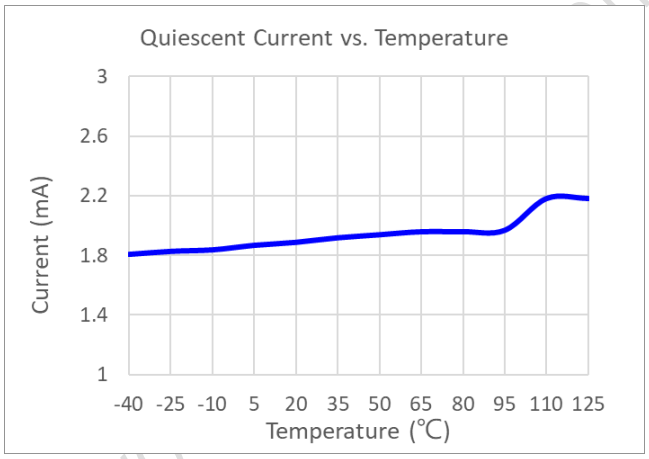


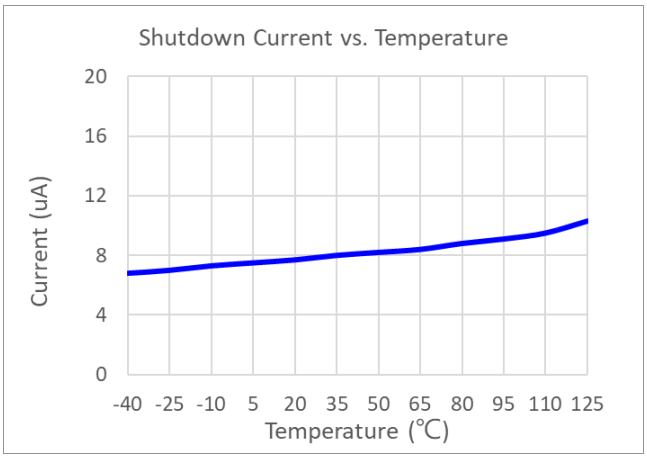




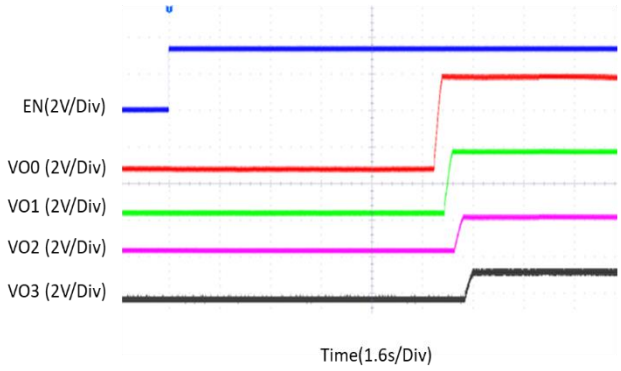




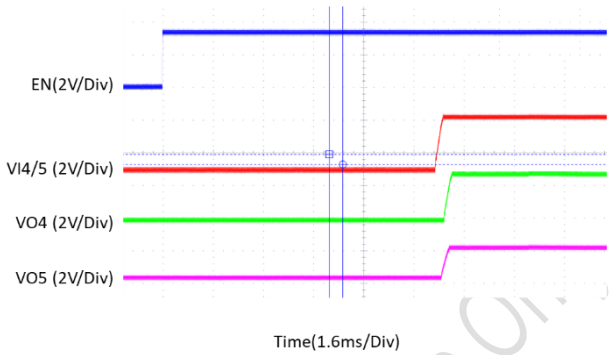




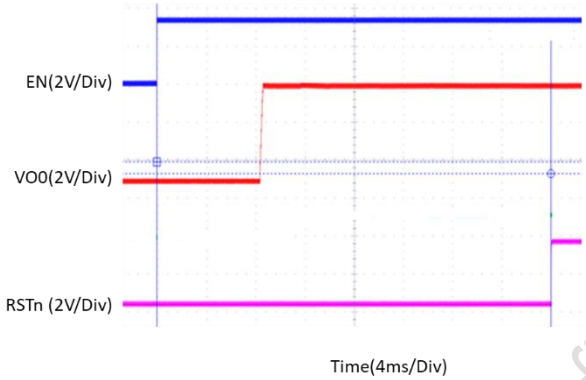
VO0~VO3, VO6 Power on Sequence with EN



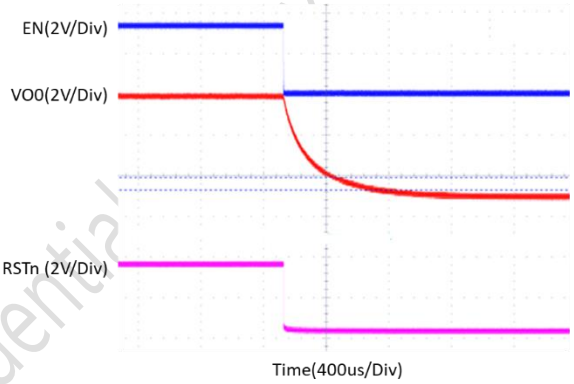
VO4~VO5 Power on Sequence with EN



RSTn Signal when Power On Sequence



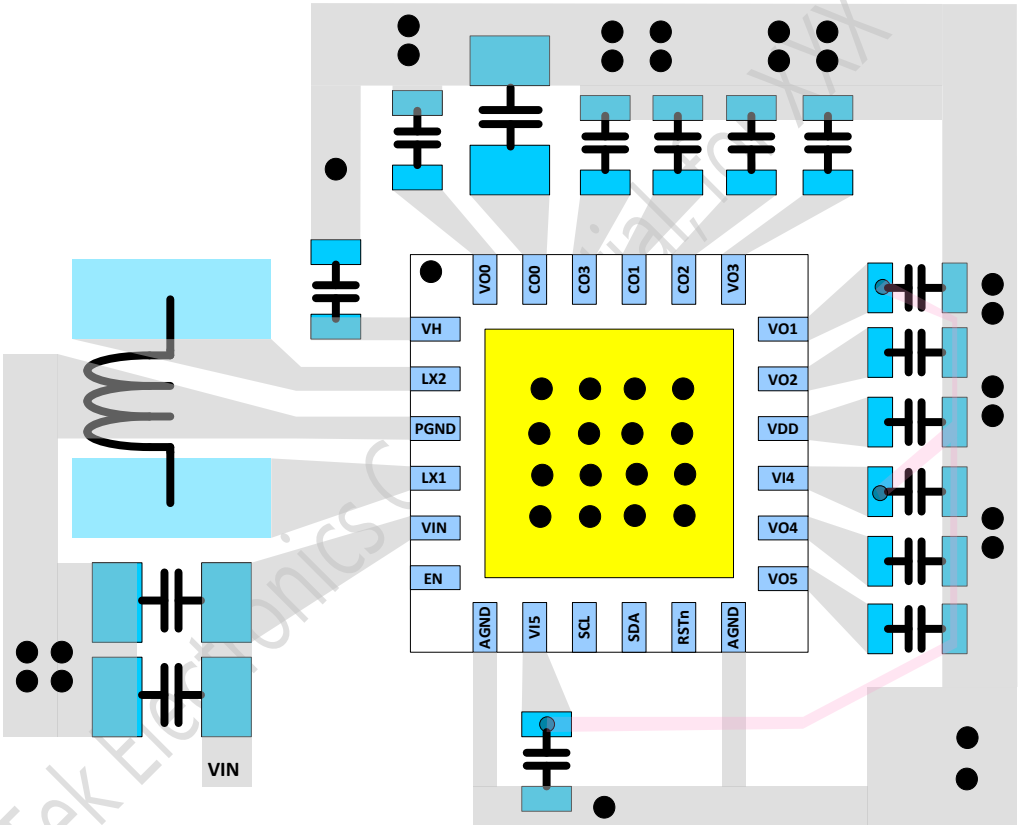
RSTn Signal when Power Off Sequence



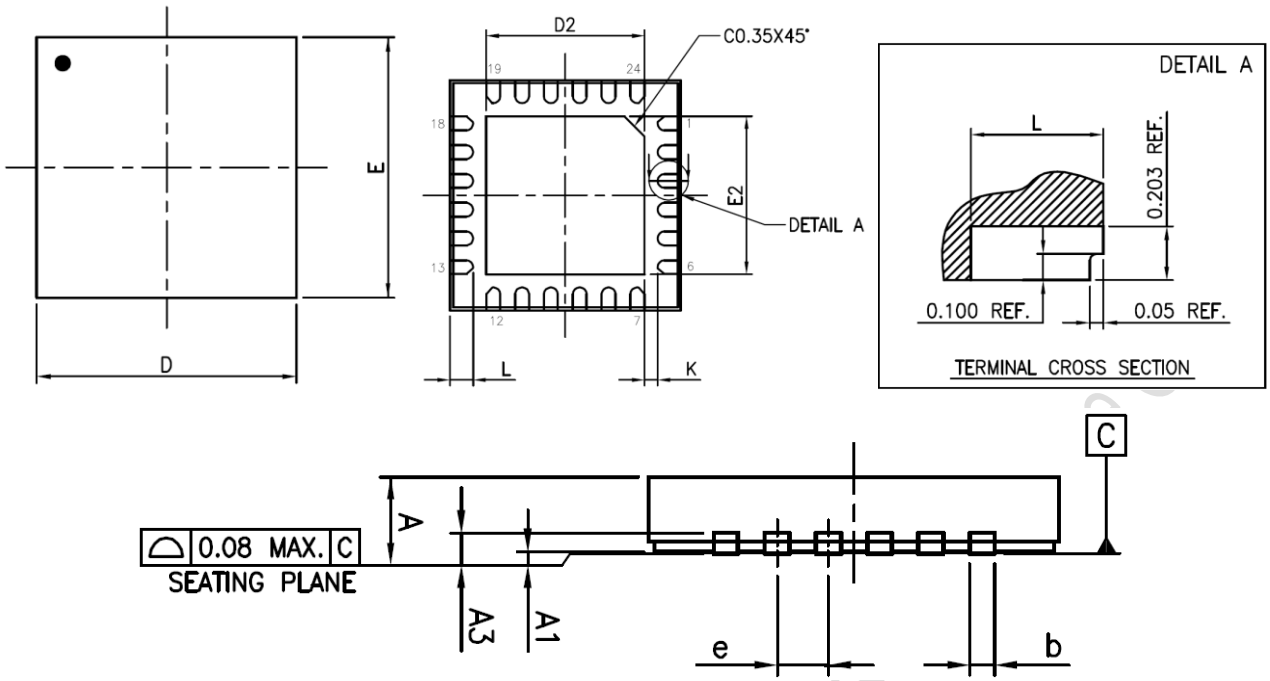
14 Layout Guidelines

For the best performance of the BV8002, the basic principles listed should be strictly followed.

- Place C1 and C2 as close as possible to the VIN pins respectively
- Place C7 and C8 as close as possible to the VDD and VH pins respectively
- Place C3 to C6 as close as possible to the CO0 to CO3 pins respectively
- Place C9 to C12 as close as possible to the VO0 to VO3 pins respectively
- Place C13 and C14 as close as possible to the VI4 and VO4 pins respectively
- Place C15 and C16 as close as possible to the VI5 and VO5 pins respectively
- Place L1 as close as possible to the LX1 and LX2 pins
- For good regulation, the power traces should be wide and short especially for the high current output loop



15 Outline Dimension



PKG CODE	Wettable WQFN(X4W3) (mm)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.8
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
L	0.35	0.4	0.45
K	0.20	-	-

	E2			D2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
115x115 MIL	2.45	2.50	2.55	2.45	2.50	2.55

16 VERSION HISTORY

Version #	Implemented By	Revision Date	Approved By	Approval Date	Reason
0.1	Stanley	12.11.2020			Initial Design Definition draft

Template Version: 06/05, 2019