



BUK9Y2R4-40H

N-channel 40 V, 2.4 mΩ logic level MOSFET in LPAK56

14 January 2025

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- LPAK copper clip technology:
 - Improved reliability, with reduced R_{th} and R_{DSon}
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

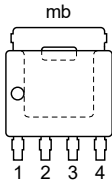
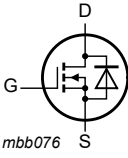
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$		-	-	163	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}; \text{Fig. 10}$		1.35	1.93	2.4	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		-	5.9	11.7	nC
Source-drain diode							
Q _r	recovered charge	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; [2]		-	24.9	-	nC
S	softness factor	V _{DS} = 20 V		-	0.85	-	

- [1] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature
- [2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y2R4-40H	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y2R4-40H	92H440

8. Limiting values

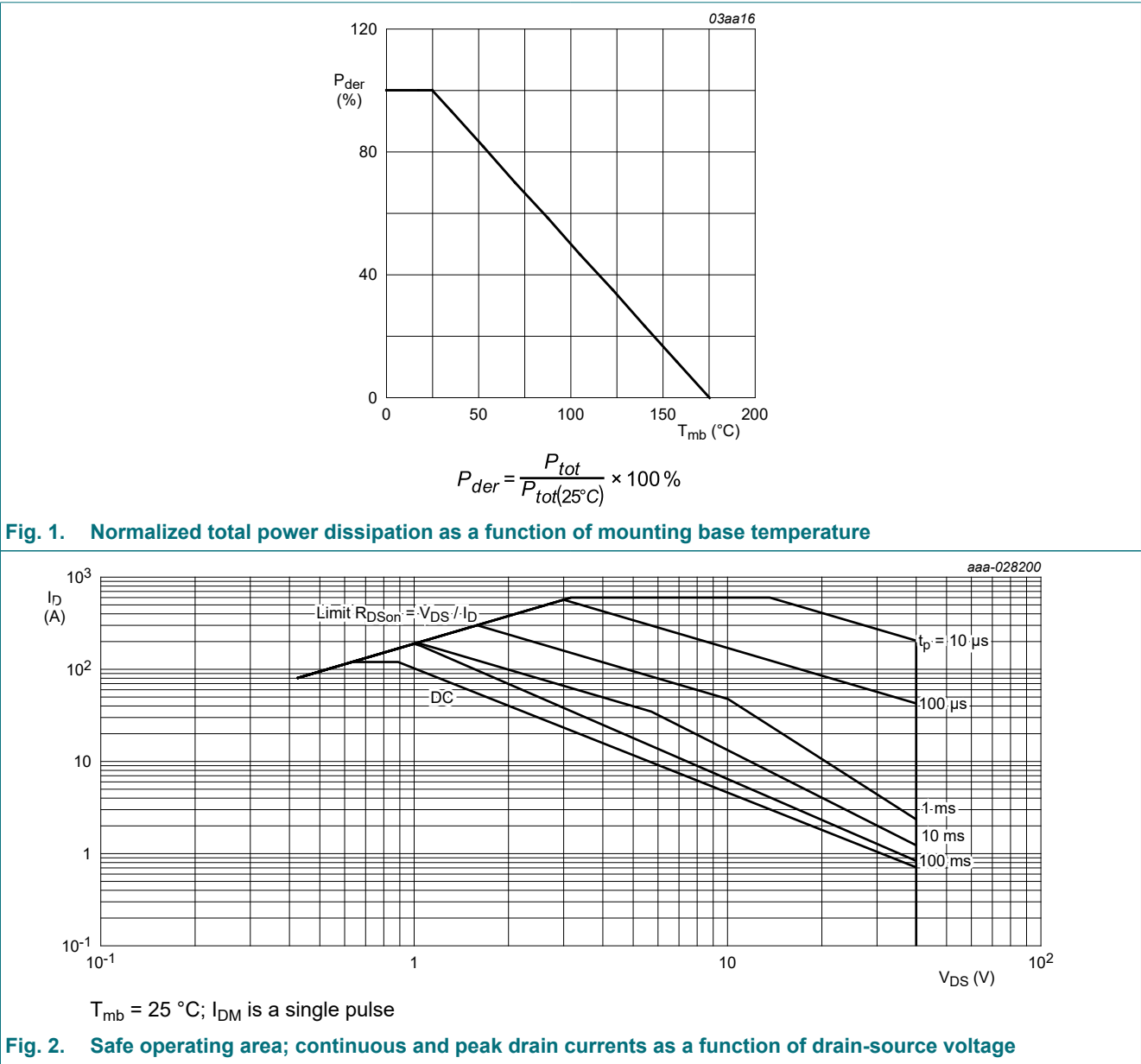
Table 5. Limiting values

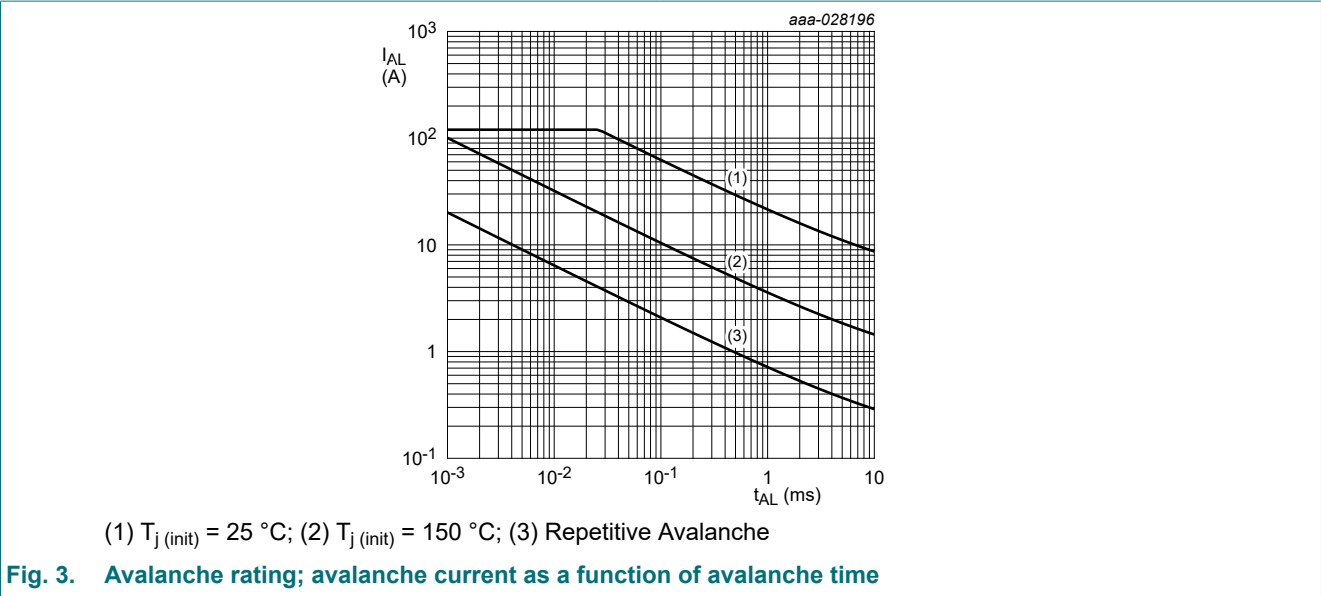
In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V _{GS}	gate-source voltage		[1]	-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	163	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	[2]	-	120	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 2		-	600	A

Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	600	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 3	[3] [4]	-	81.5	mJ

- [1] Refer to application note AN90001 for further information.
- [2] 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

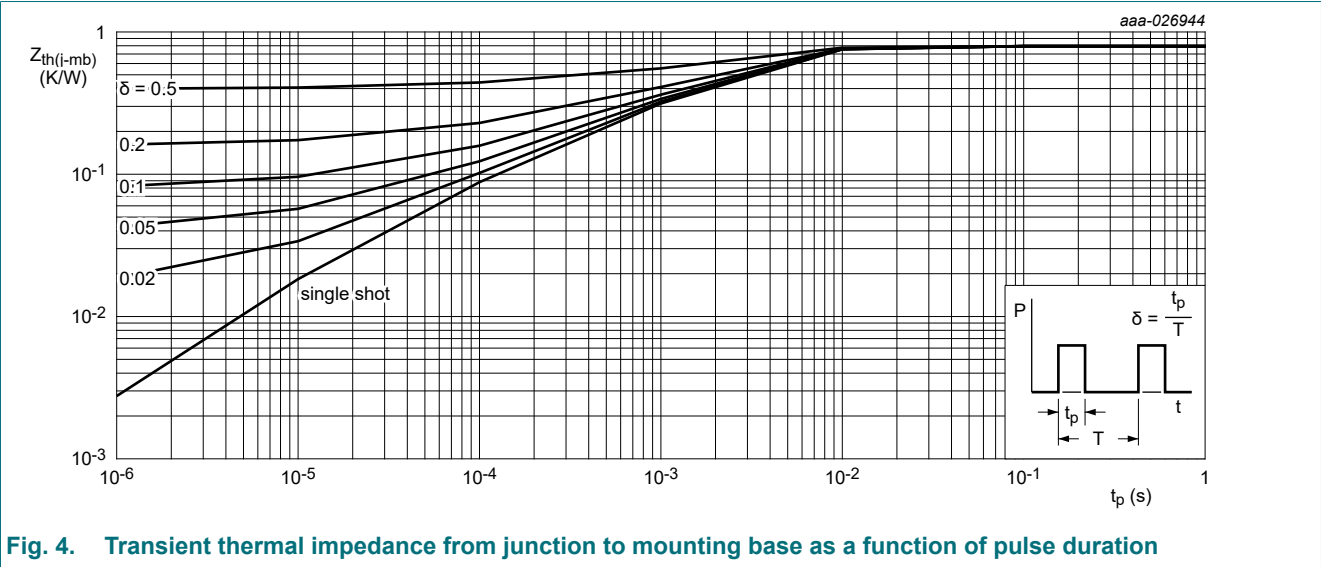




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.63	0.79	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	40	43	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -40\ ^\circ C$	-	40.5	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -55\ ^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = 25\ ^\circ C$; Fig. 8 ; Fig. 9	1.35	1.66	2.05	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = 175\ ^\circ C$; Fig. 9	0.6	-	-	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = -55\ ^\circ C$; Fig. 9	-	-	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	-	0.06	5	μA
		$V_{DS} = 16\ V$; $V_{GS} = 0\ V$; $T_J = 125\ ^\circ C$	-	1.2	10	μA
		$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $T_J = 175\ ^\circ C$	-	142	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	2	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_J = 25\ ^\circ C$; Fig. 10	1.35	1.93	2.4	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_J = 105\ ^\circ C$; Fig. 11	2	2.95	3.8	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_J = 125\ ^\circ C$; Fig. 11	2.2	3.2	4.2	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_J = 175\ ^\circ C$; Fig. 11	2.8	4.11	5.2	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_J = 25\ ^\circ C$; Fig. 10	1.68	2.4	3.2	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_J = 105\ ^\circ C$; Fig. 11	2.5	3.67	5	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_J = 125\ ^\circ C$; Fig. 11	2.8	4	5.7	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_J = 175\ ^\circ C$; Fig. 11	3.5	5.11	7	mΩ
R_G	gate resistance	$f = 1\ MHz$; $T_J = 25\ ^\circ C$	0.29	0.72	1.8	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ A$; $V_{DS} = 20\ V$; $V_{GS} = 10\ V$; Fig. 12 ; Fig. 13	-	55.8	78.2	nC
		$I_D = 25\ A$; $V_{DS} = 20\ V$; $V_{GS} = 4.5\ V$; Fig. 12 ; Fig. 13	-	25.3	35.4	nC
Q_{GS}	gate-source charge		-	9.9	14.9	nC
Q_{GD}	gate-drain charge		-	5.9	11.7	nC
C_{iss}	input capacitance	$V_{DS} = 25\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_J = 25\ ^\circ C$; Fig. 14	-	3960	5544	pF
C_{oss}	output capacitance		-	859	1203	pF
C_{rss}	reverse transfer capacitance		-	140	308	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\ V$; $R_L = 0.8\ \Omega$; $V_{GS} = 4.5\ V$; $R_{G(ext)} = 5\ \Omega$	-	23.1	-	ns
t_r	rise time		-	26.3	-	ns
$t_{d(off)}$	turn-off delay time		-	27.2	-	ns
t_f	fall time		-	16.4	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 15		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	31	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	[1]	-	24.9	-	nC
S	softness factor			-	0.85	-	
		$I_S = 25\text{ A}$; $dI_S/dt = -500\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$;		-	0.67	-	
		$V_{DS} = 20\text{ V}$					

[1] includes capacitive recovery

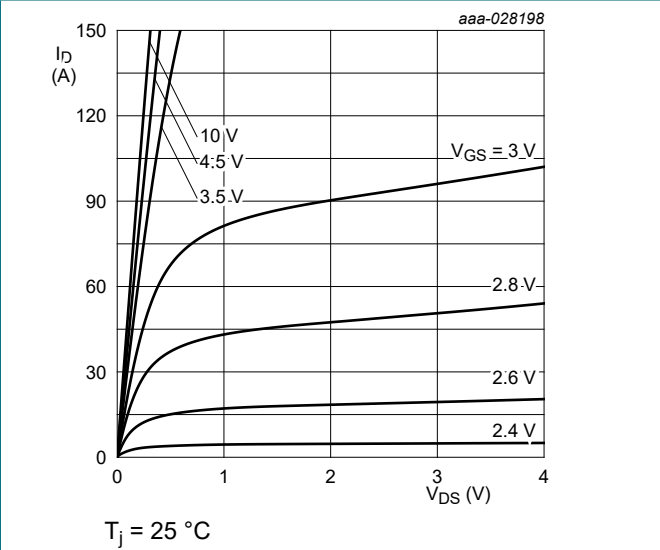


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

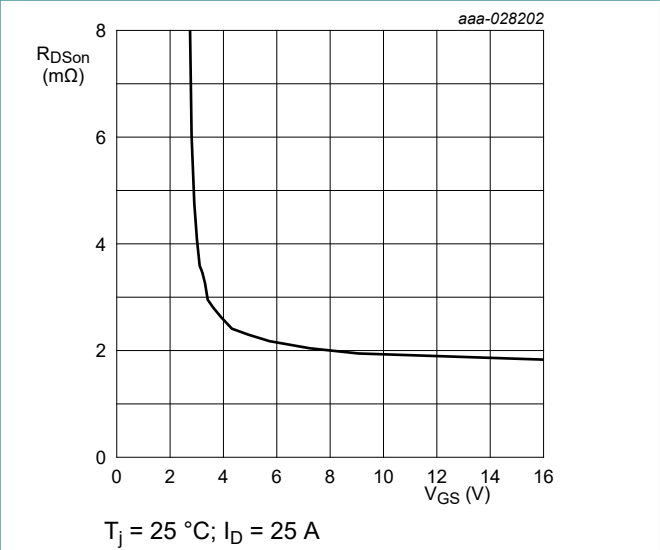


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

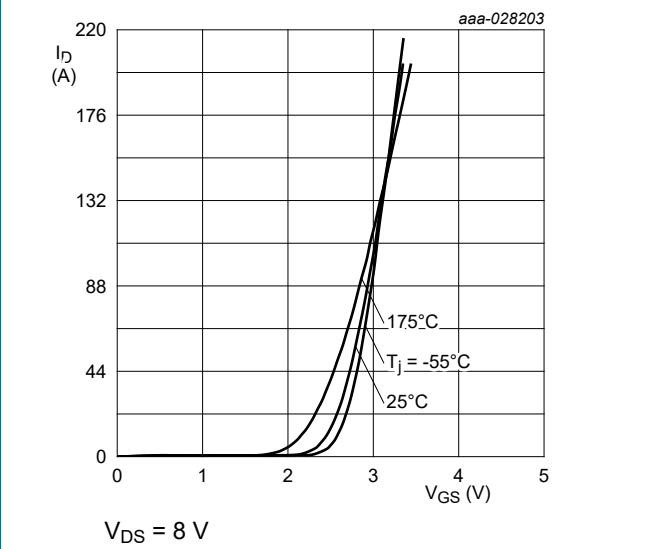


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

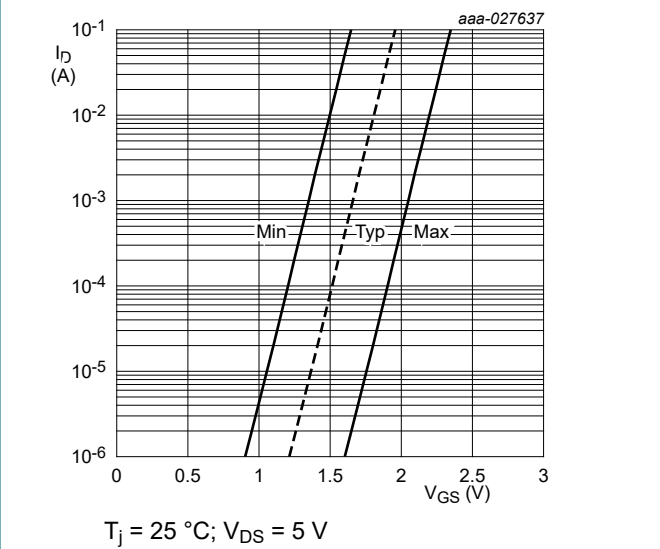


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

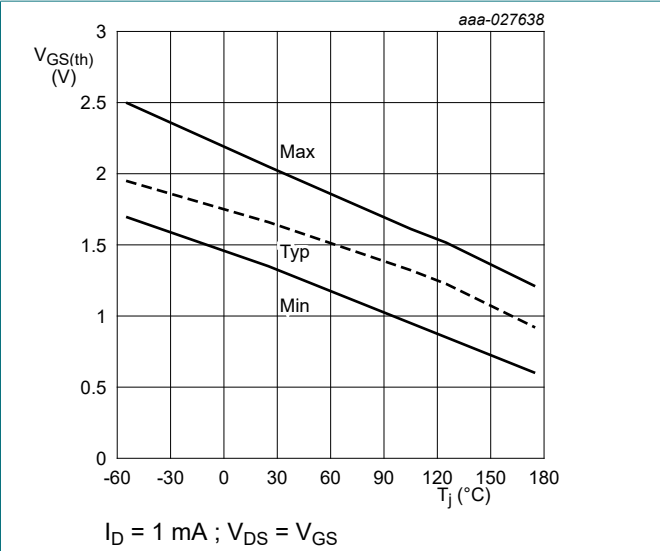


Fig. 9. Gate-source threshold voltage as a function of junction temperature

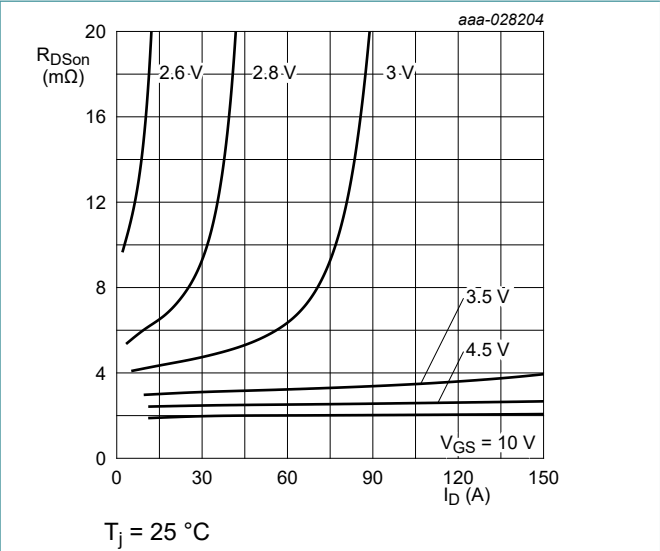


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

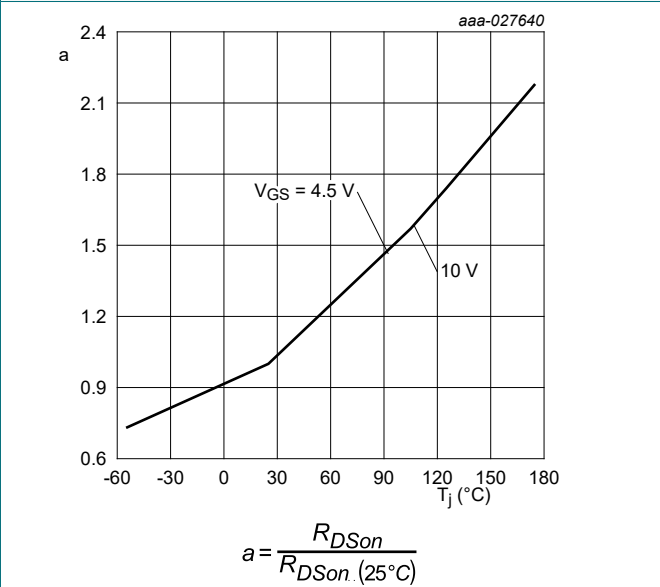


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

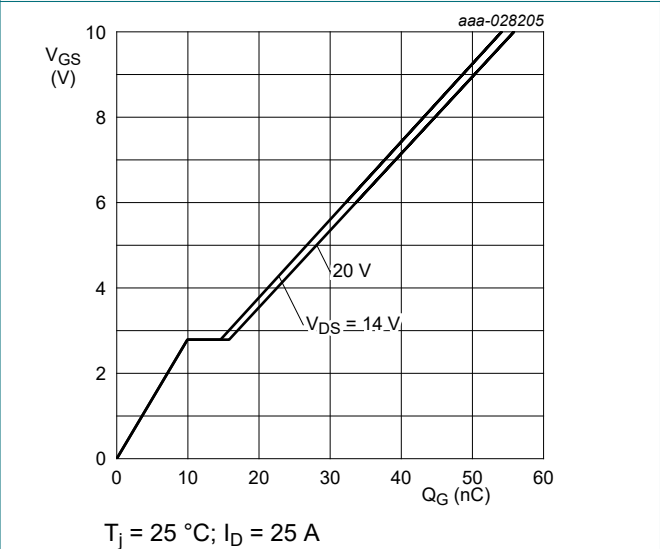


Fig. 12. Gate-source voltage as a function of gate charge; typical values

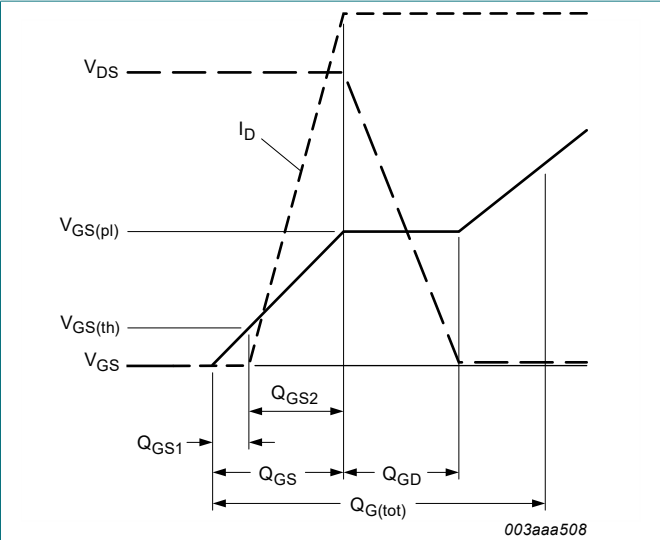


Fig. 13. Gate charge waveform definitions

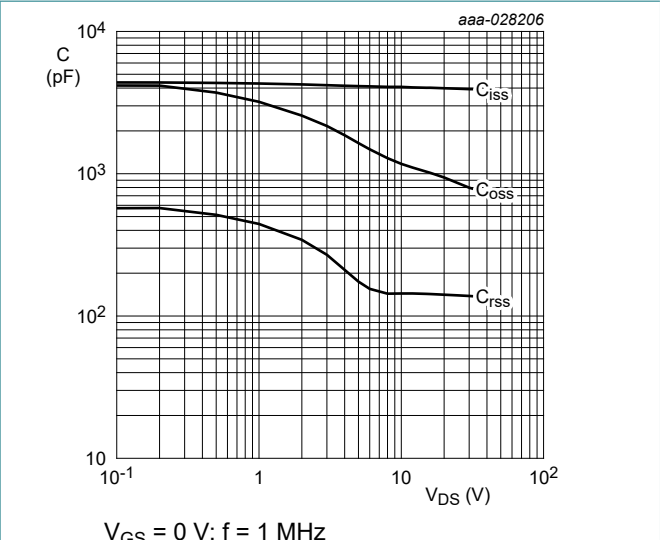


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

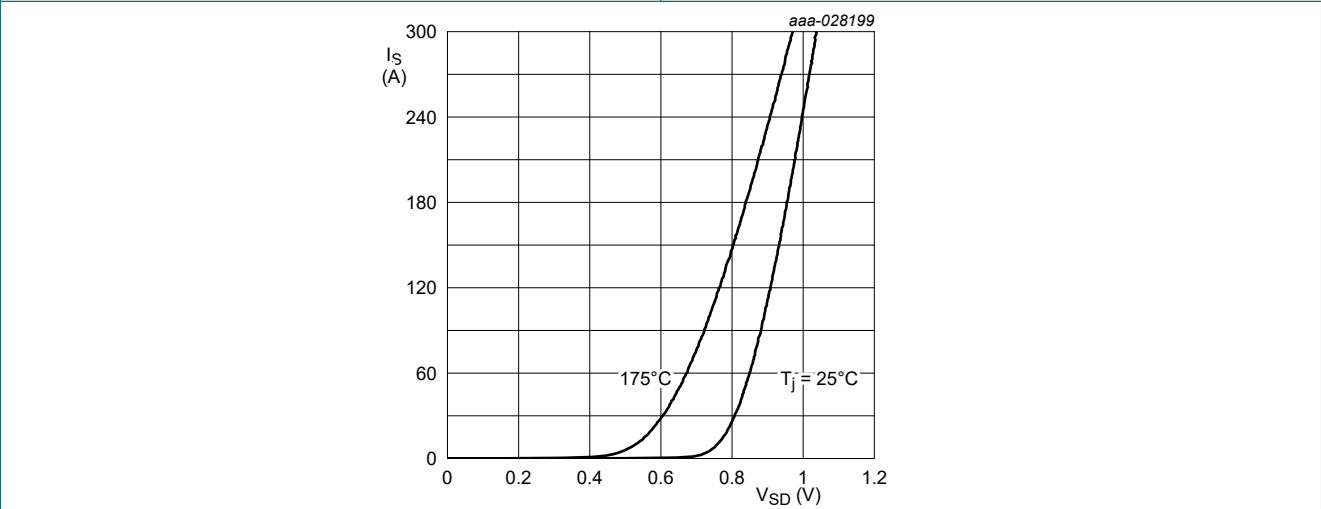


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

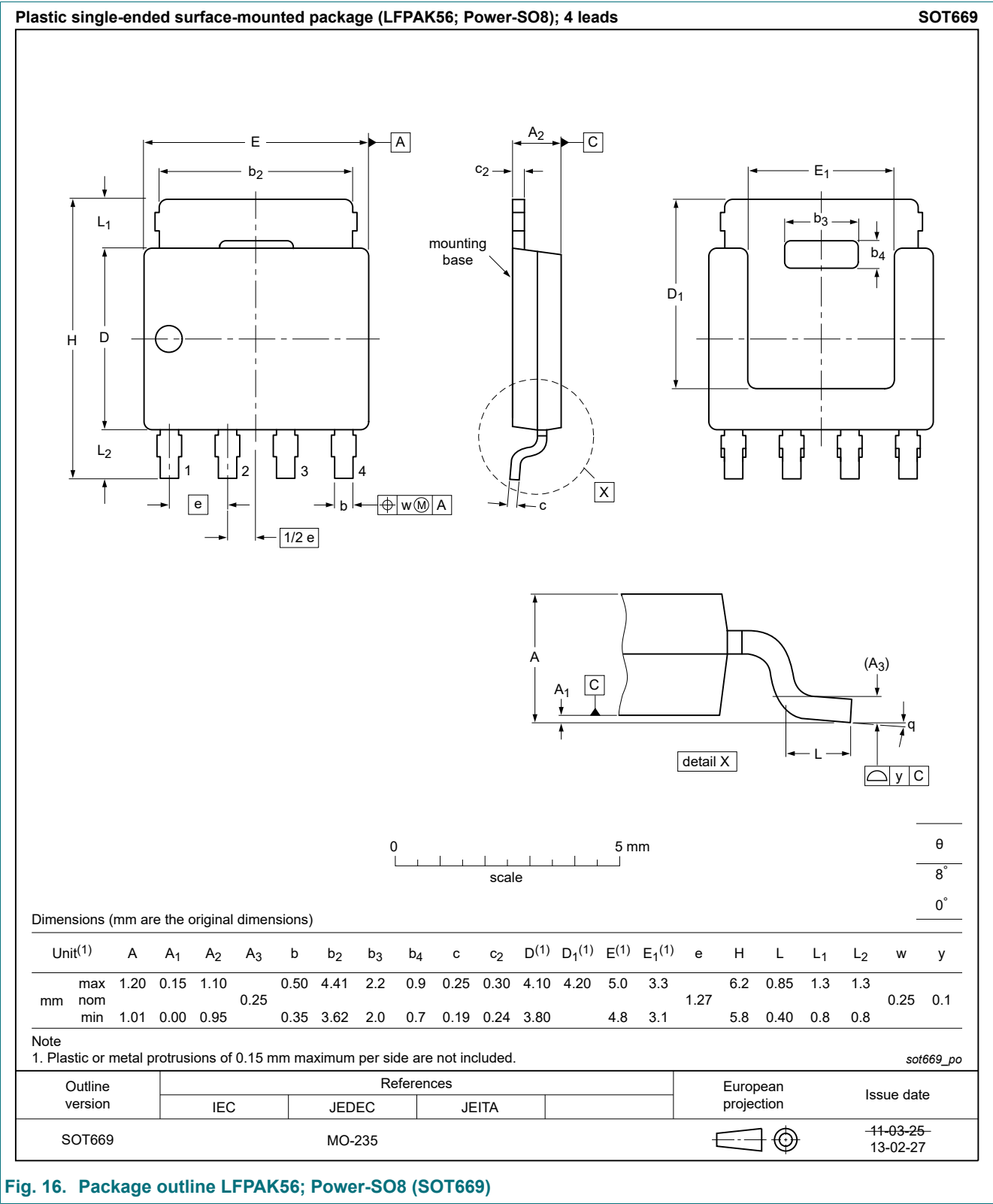


Fig. 16. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

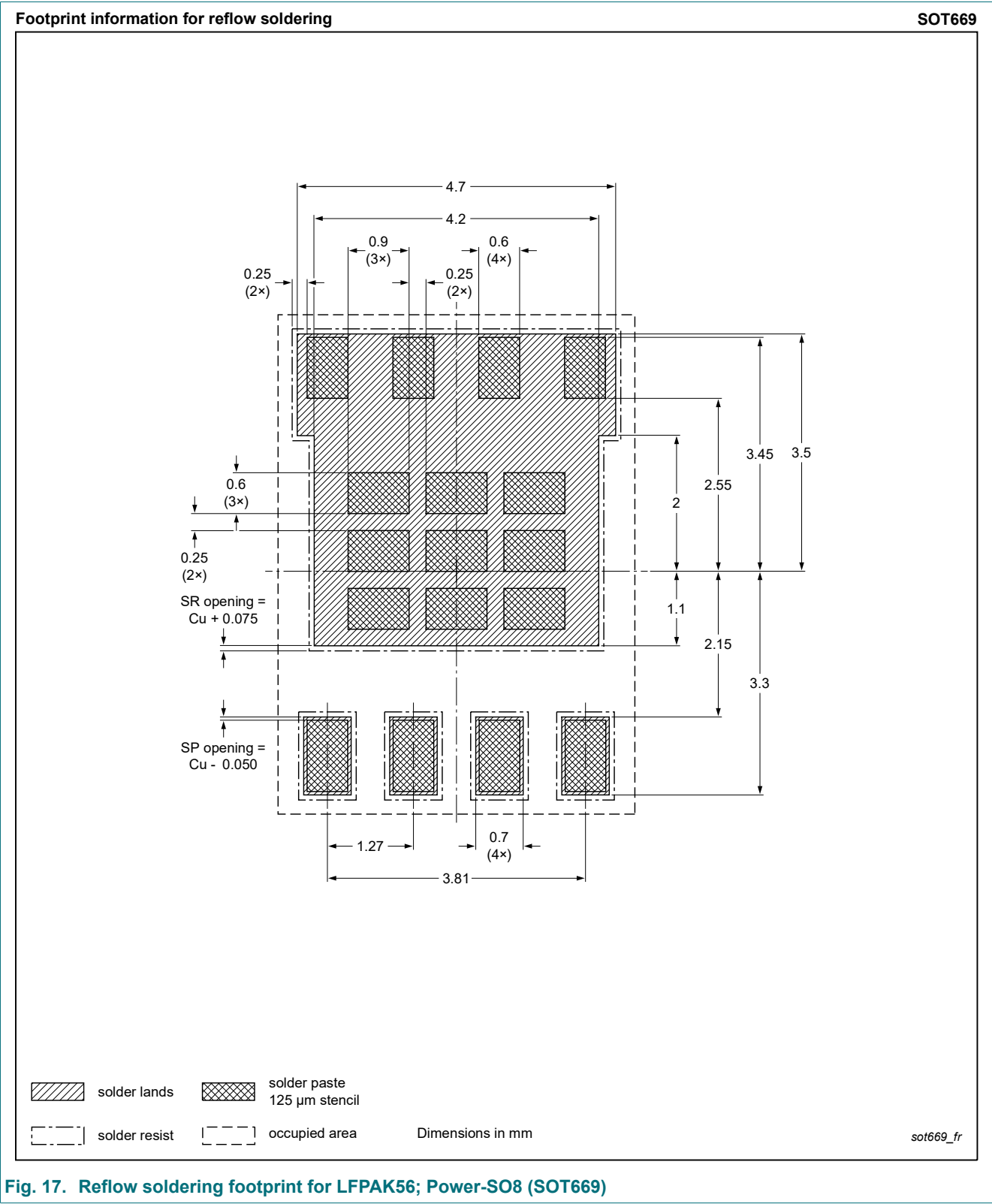


Fig. 17. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

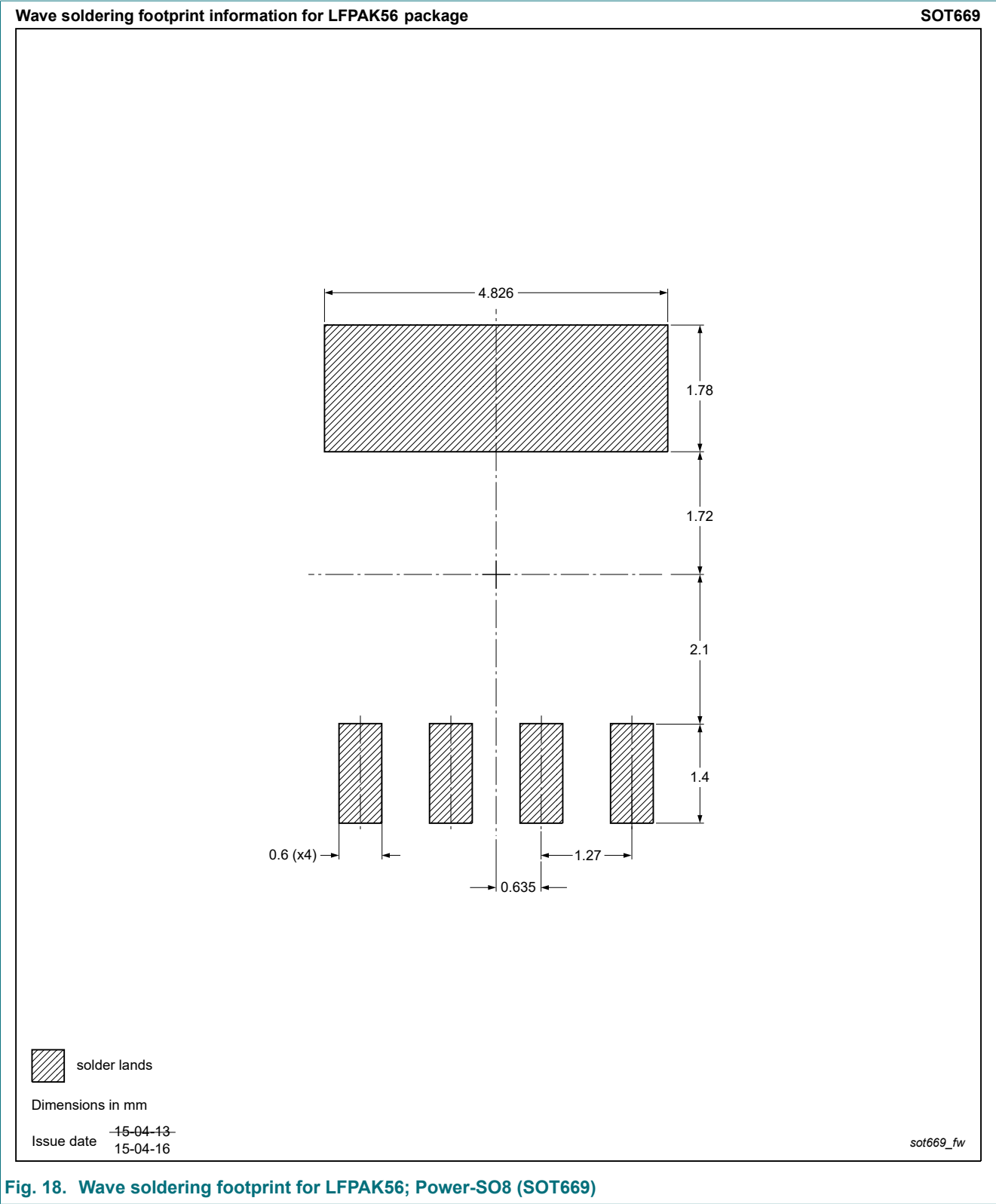


Fig. 18. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 14 January 2025