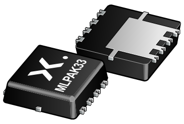


BUK9Q4R6-40H

Logic level N-Channel MOSFET in MLPAK33-WF (SOT8002-3D)

7 May 2025 Product data sheet

1. General description

Logic level N-Channel MOSFET in a small MLPAK33-WF (SOT8002-3D) package using Trench 9 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Trench 9 technology
- Small footprint (3 x 3 mm) for compact design
- Qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automated optical inspection

3. Applications

- Motor drive
- Battery protection
- DC-DC conversion

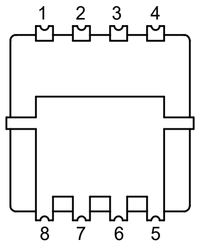
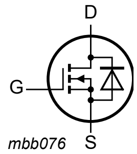
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	-	90	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	84	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		2.78	3.96	4.6	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 13; Fig. 14		-	3.7	7.4	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **MLPAK33 (SOT8002-3)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Q4R6-40H	MLPAK33	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Q4R6-40H	6AR

8. Limiting values

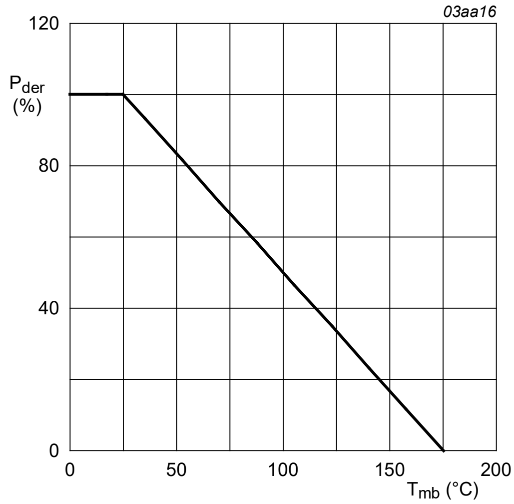
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	84	W
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	90	A
		V_{GS} = 5 V; T_{mb} = 100 °C; Fig. 2		-	68	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	387	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	84	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	387	A

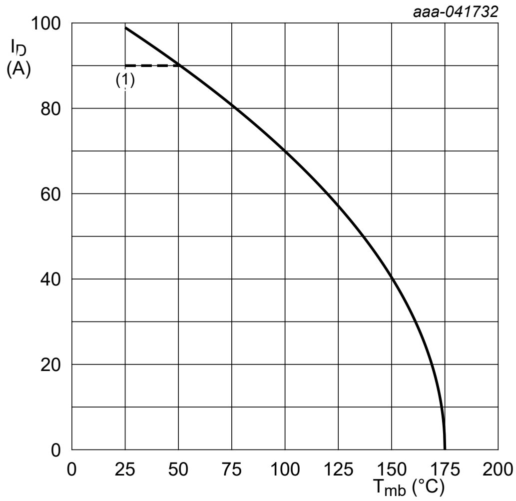
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 39.14 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 136 µs; Fig. 4	[1] [2]	-	139	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 40 V; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[3]	-	84	A

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.
[3] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

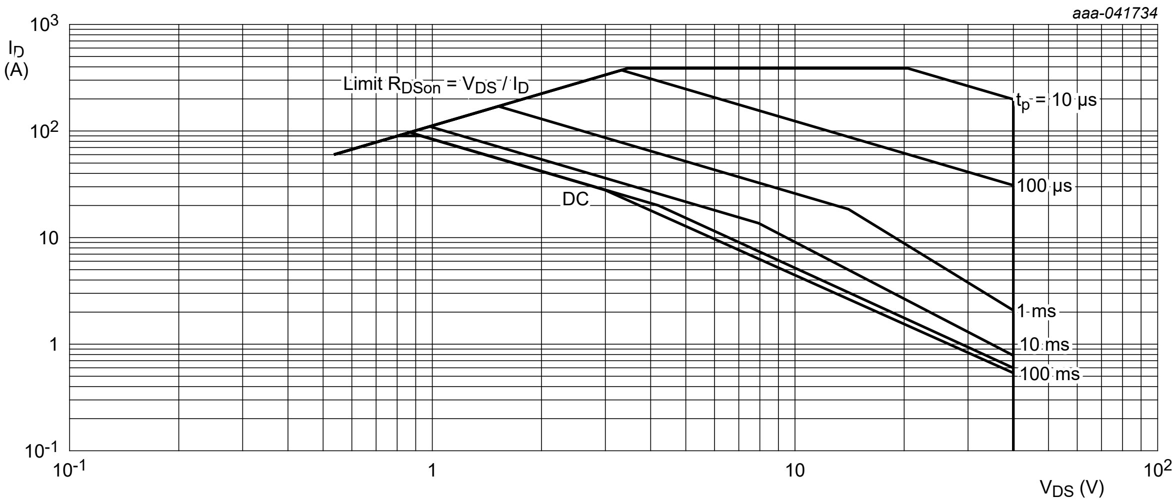
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 5 V

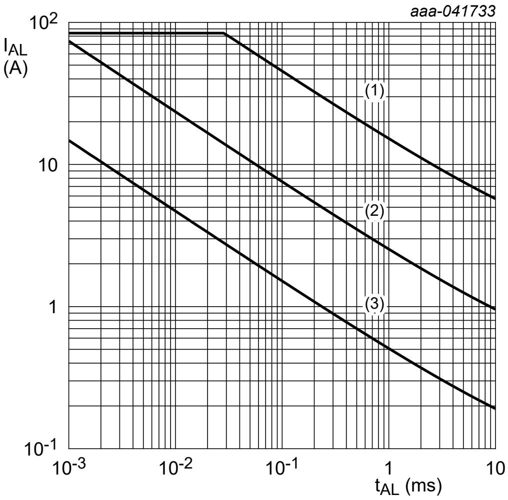
(1) 90 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.49	1.79	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	40	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.

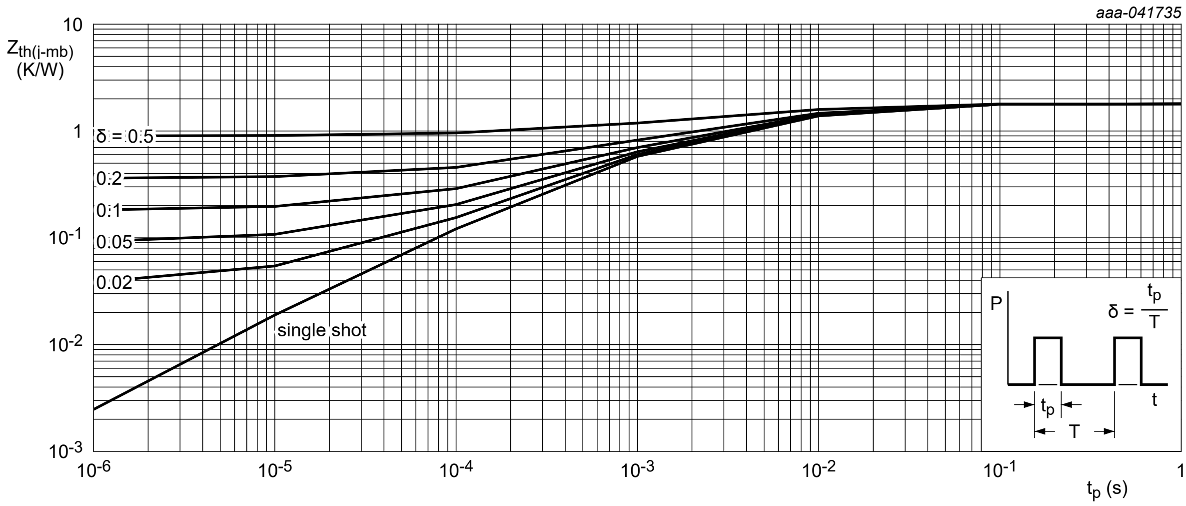


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

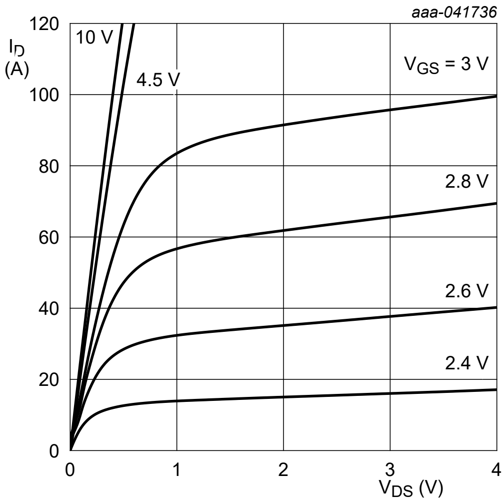
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C		40	44	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -40 °C		-	40.5	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.35	1.63	2.05	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10		0.7	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.6	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	μA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	μA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		2.78	3.96	4.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 12		4.1	5.57	6.8	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 12		4.46	5.95	7.41	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12		5.29	7.14	8.79	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 11		3.26	4.65	5.98	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 105 °C; Fig. 12		4.82	6.57	8.85	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 125 °C; Fig. 12		5.24	7	9.63	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 175 °C; Fig. 12		6.22	8.39	11.4	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		1.04	2.6	6.5	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		-	38	52	nC
		I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; T_j = 25 °C; Fig. 13; Fig. 14		-	17	24	nC
Q_{GS}	gate-source charge			-	7	10	nC
Q_{GD}	gate-drain charge			-	3.7	7.4	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	2604	3645	pF
C_{oss}	output capacitance			-	462	647	pF
C_{rss}	reverse transfer capacitance			-	103	227	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 0.8 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	16	-	ns
t_r	rise time			-	21	-	ns
$t_{d(off)}$	turn-off delay time			-	25	-	ns
t_f	fall time			-	14	-	ns

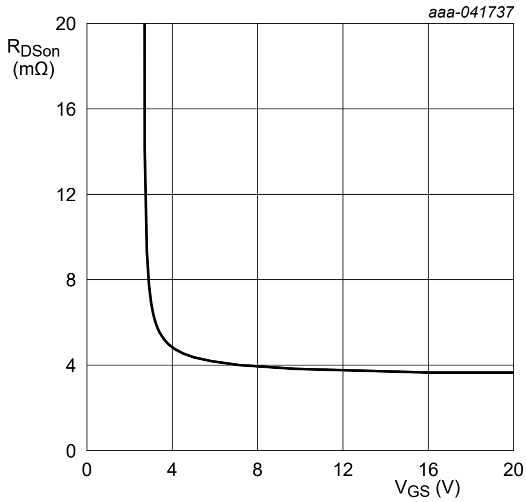
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.82	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 17		-	24	-	ns
Q_r	recovered charge		[1]	-	15	-	nC

[1] includes capacitive recovery



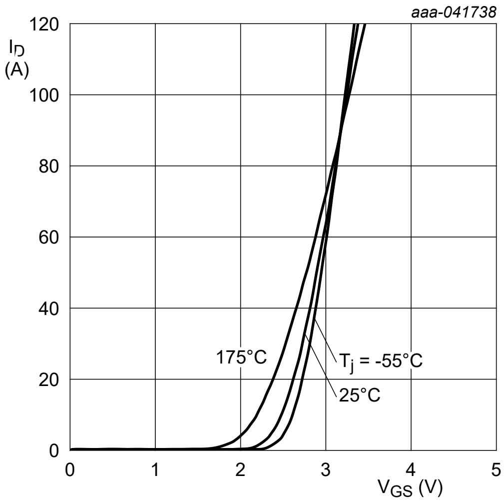
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



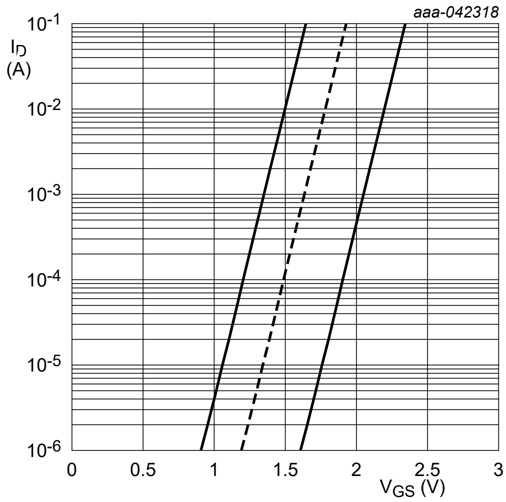
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



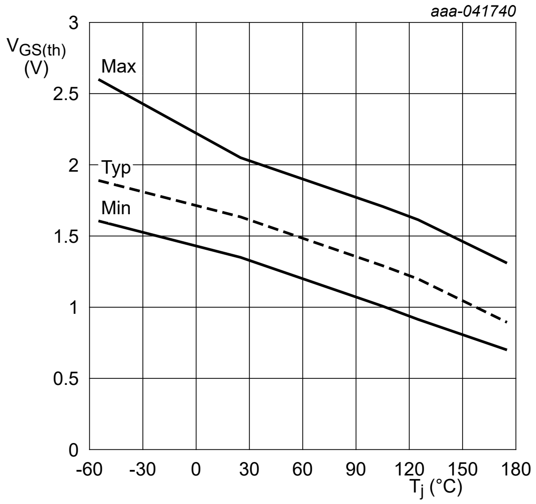
V_{DS} = 8 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



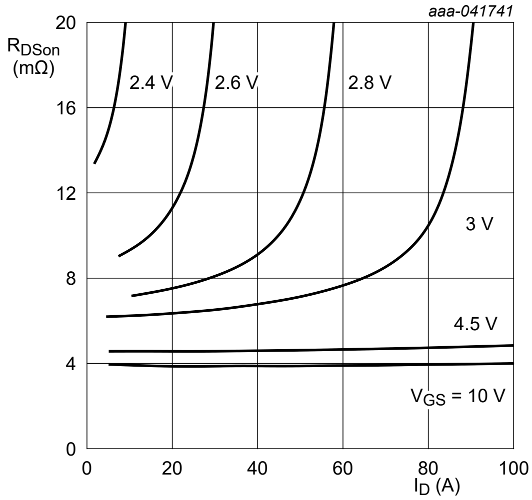
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage



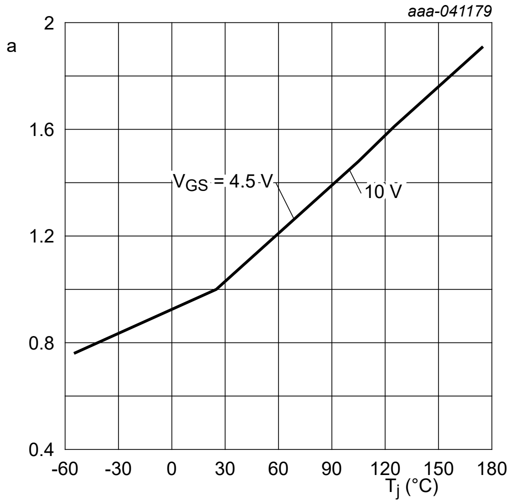
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature



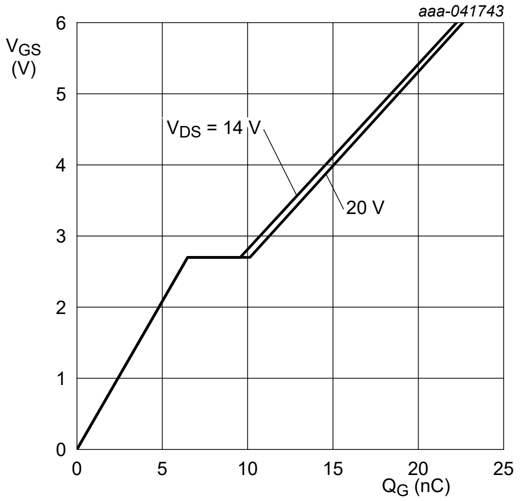
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values

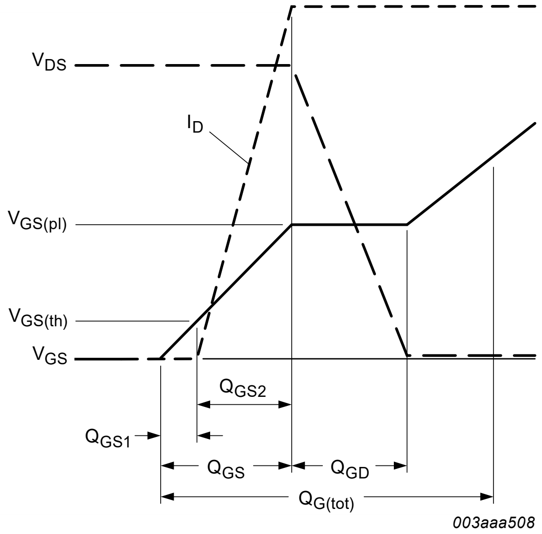
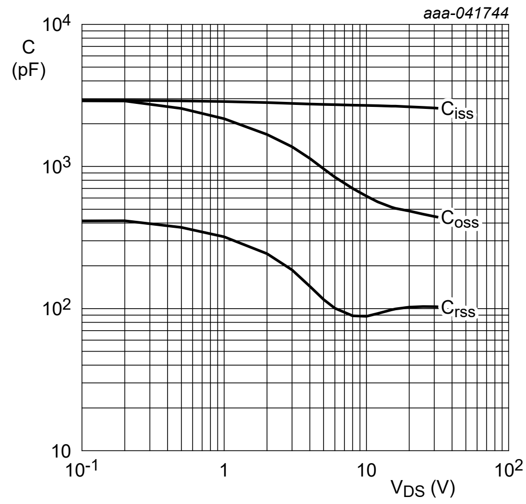
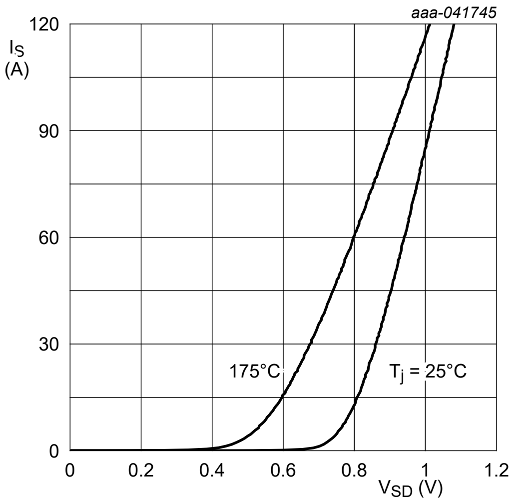


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

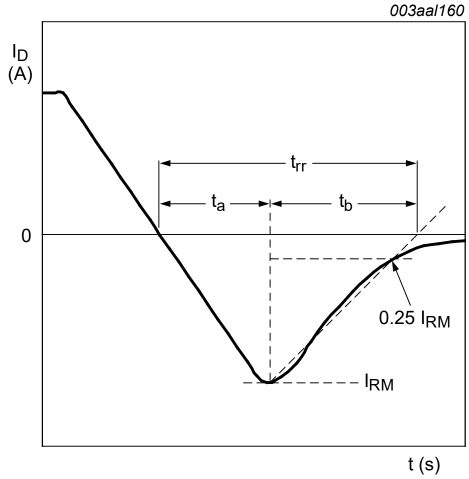
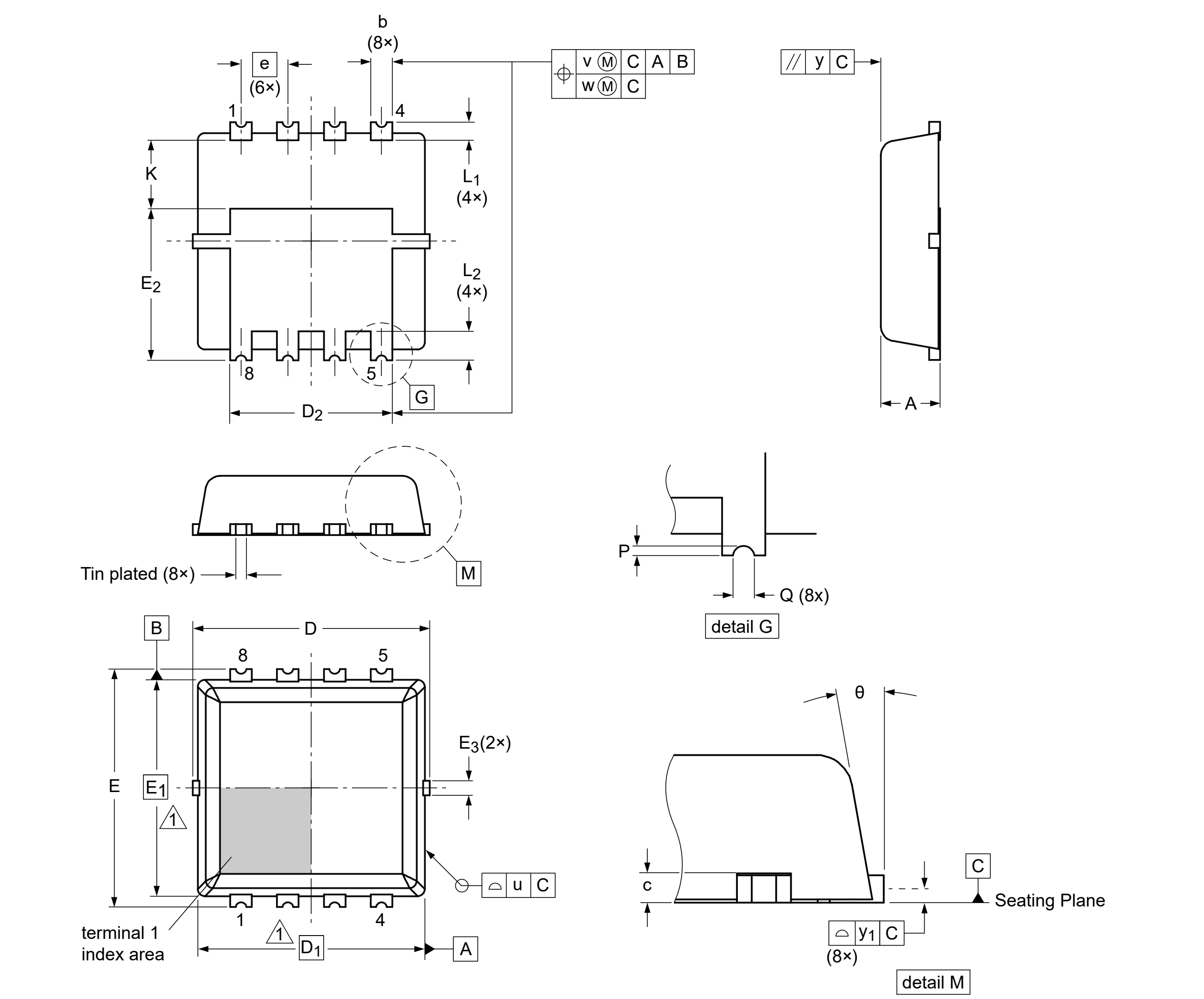


Fig. 17. Reverse recovery timing definition

11. Package outline

MLPAK33: plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body **SOT8002-3**



⚠1 Dimensions do not include mold flash, protrusions of gate burrs, mold flash, tie bar protrusion or tie bar flash. Mold flash shall not be greater than 0.05 mm

0 — 5 mm
scale

w
0.05

Dimensions (mm are the original dimensions)

Unit		A	b	c	D	D_1	D_2	e	E	E_1	E_2	E_3	K	L_1	L_2	P	Q	θ	y	y_1	u	v
	max	0.90	0.40	0.18	3.40		2.35		3.40		2.20			0.40	0.55			12°				
mm	nom	0.80	0.32	0.15	3.30	3.15 BSC	2.25	0.65 BSC	3.30	3.0 BSC	2.10	0.2 REF	0.95 REF	0.25	0.40	0.1 REF	0.15 REF	10°	0.05	0.05	0.1	0.1
	min	0.70	0.25	0.12	3.20		2.15		3.20		2.00			0.10	0.25			8°				

sot8002-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8002-3						23-07-21

Fig. 18. Package outline MLPAK33 (SOT8002-3)

12. Soldering

Footprint information for reflow soldering of MLPAK33 package **SOT8002-3**

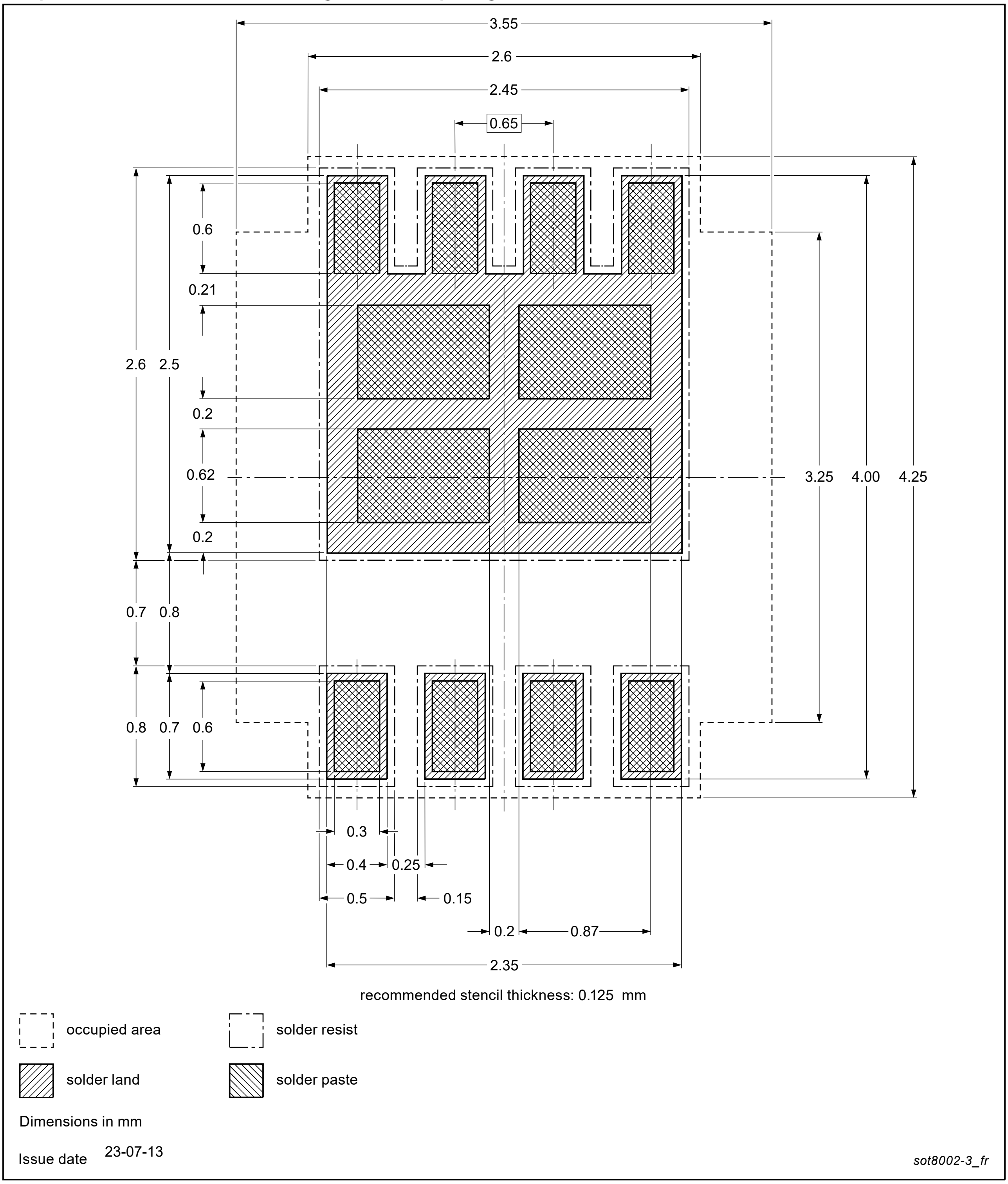


Fig. 19. Reflow soldering footprint for MLPAK33 (SOT8002-3)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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Date of release: 7 May 2025