BUK9MJJ-55PTT

Dual TrenchPLUS logic level FET

Rev. 01 — 14 May 2009 Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode field-effect power transistor in SO20. Device is manufactured using NXP High-Performance (HPA) TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

1.2 Features and benefits

- Integrated current sensors
- Integrated temperature sensors

1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

1.4 Quick reference data

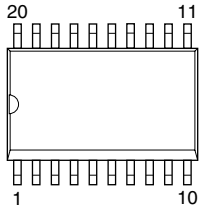
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics, FET1 and FET2						
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A; T_j = 25 °C; see Figure 16; see Figure 17	-	13	15	mΩ
I_D/I_{sense}	ratio of drain current to sense current	T_j = 25 °C; V_{GS} = 5 V; see Figure 18	5850	6500	7150	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	T_j = 25 °C; V_{GS} = 0 V; I_D = 250 µA	55	-	-	V

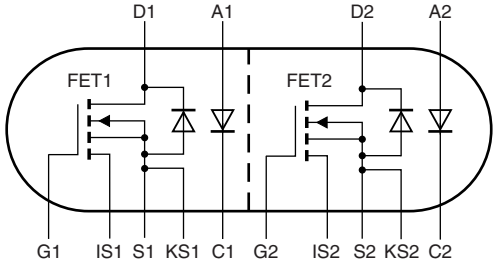
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G1	gate 1		
2	IS1	current sense 1		
3	D1	drain 1		
4	A1	anode 1		
5	C1	cathode 1		
6	G2	gate 2		
7	IS2	current sense 2		
8	D2	drain 2		
9	A2	anode 2		
10	C2	cathode 2		
11	D2	drain 2		
12	KS2	Kelvin source 2		
13	S2	source 2		
14	S2	source 2		
15	D2	drain 2		
16	D1	drain 1		
17	KS1	Kelvin source 1		
18	S1	source 1		
19	S1	source 1		
20	D1	drain 1		



SOT163-1
(SO20)



003aaa745

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9MJJ-55PTT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Limiting Values, FET1 and FET2						
V_{DS}	drain-source voltage	25 °C < T_j < 150 °C		-	55	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ; 25 °C < T_j < 150 °C		-	55	V
V_{GS}	gate-source voltage			-15	15	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 5 V; see Figure 3; see Figure 2;	[1][2]	-	12.9	A
		T_{sp} = 100 °C; V_{GS} = 5 V; see Figure 2;	[1][2]	-	8.1	A
I_{DM}	peak drain current	T_{sp} = 25 °C; t_p ≤ 10 µs; pulsed; see Figure 3		-	230	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 1		-	4.5	W
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage			-	100	V
Source-drain diode, FET1 and FET2						
I_S	source current	T_{sp} = 25 °C;	[2][1]	-	6.5	A
I_{SM}	peak source current	t_p ≤ 10 µs; pulsed; T_{sp} = 25 °C		-	230	A
Avalanche ruggedness, FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 12.9 A; V_{sup} ≤ 55 V; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; see Figure 4;	[3][4] [5]	-	527	mJ
Electrostatic discharge, FET1 and FET2						
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ; pins 3, 16 and 20 to pins 1, 2, 17, 18 and 19 shorted		-	4	kV
		HBM; C = 100 pF; R = 1.5 kΩ; pins 8, 11 and 15 to pins 6, 7, 12,13 and 14 shorted		-	4	kV
		HBM; C = 100 pF; R = 1.5 kΩ; all pins		-	0.15	kV

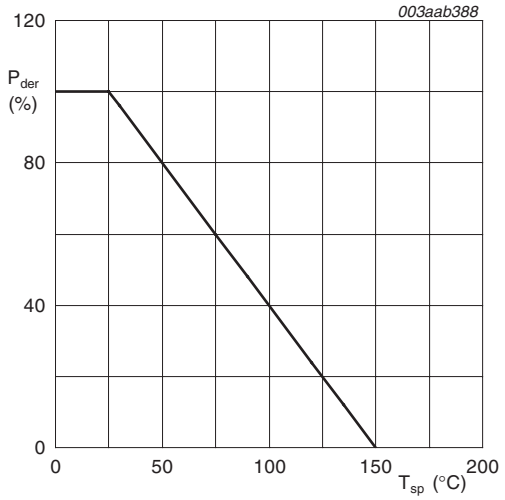
[1] Single device conducting.

[2] Current is limited by chip power dissipation rating.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

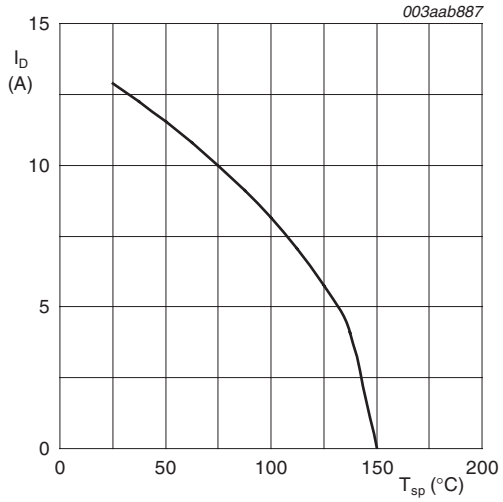
[4] Repetitive rating defined in avalanche rating figure.

[5] Refer to application note AN10273 for further information.



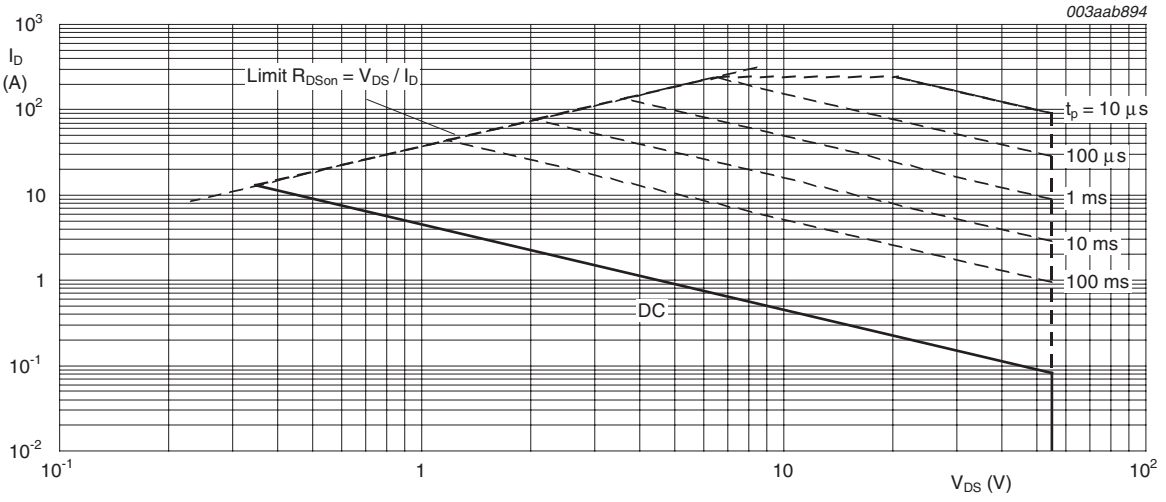
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature, FET1 and FET2



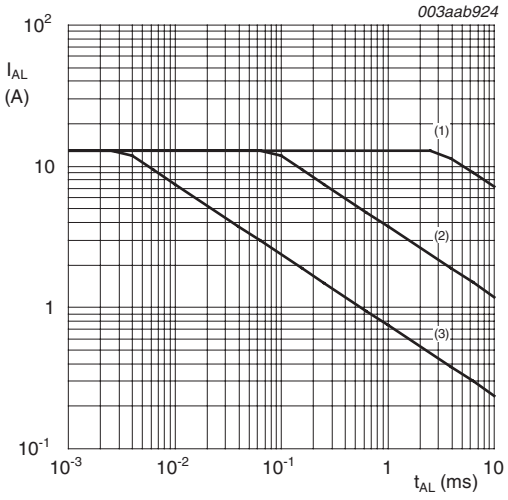
$$V_{GS} \geq 5V$$

Fig 2. Continuous drain current as a function of solder point temperature, FET1 and FET2



$$T_{sp} = 25\,°C; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2



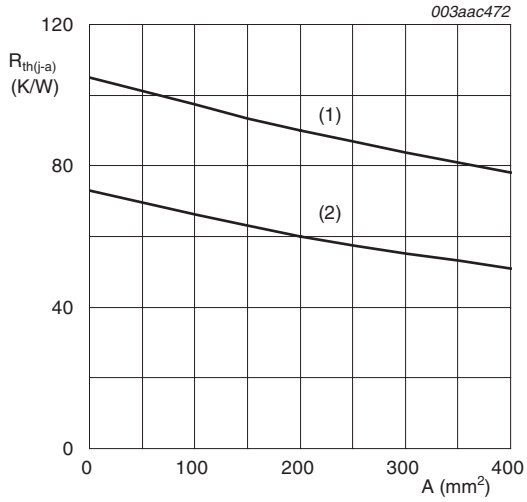
(1) Single-pulse; $T_j = 25\,°C$.
(2) Single-pulse; $T_j = 150\,°C$.
(3) Repetitive.

Fig 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	FET1	-	-	28	K/W
		FET2	-	-	28	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; Both channels conducting; zero heat sink area; see Figure 5; see Figure 6	-	73	-	K/W
		mounted on a printed-circuit board; Both channels conducting; 200 mm^2 copper heat sink area; see Figure 5; see Figure 7	-	60	-	K/W
		mounted on a printed-circuit board; Both channels conducting; 400 mm^2 copper heat sink area; see Figure 5; see Figure 8	-	51	-	K/W
		mounted on a printed-circuit board; One channel conducting; zero heat sink area; see Figure 5; see Figure 6	-	105	-	K/W
		mounted on a printed-circuit board; One channel conducting; 200 mm^2 copper heat sink area; see Figure 5; see Figure 7	-	90	-	K/W
		mounted on a printed-circuit board; One channel conducting; 400 mm^2 copper heat sink area; see Figure 5; see Figure 8	-	78	-	K/W



(1) One channel conducting dissipating 500mW.
(2) Both channels conducting each dissipating 500mW.
Zero air flow

Fig 5. Thermal resistance from junction to ambient as a function of printed-circuit board (PCB) heat sink area

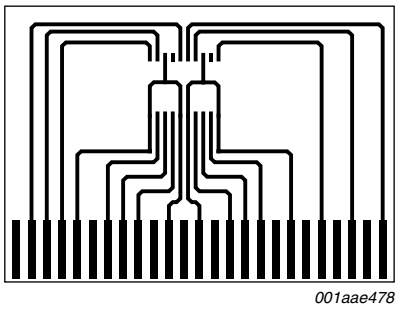


Fig 6. PCB used for thermal tests; zero heat sink area

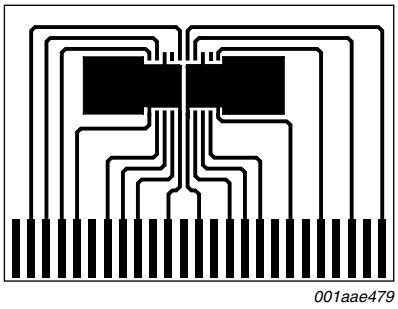


Fig 7. PCB used for thermal tests; heat sink area 200 mm^2

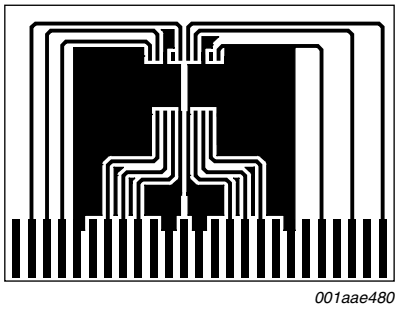


Fig 8. PCB used for thermal tests; heat sink area 400 mm^2

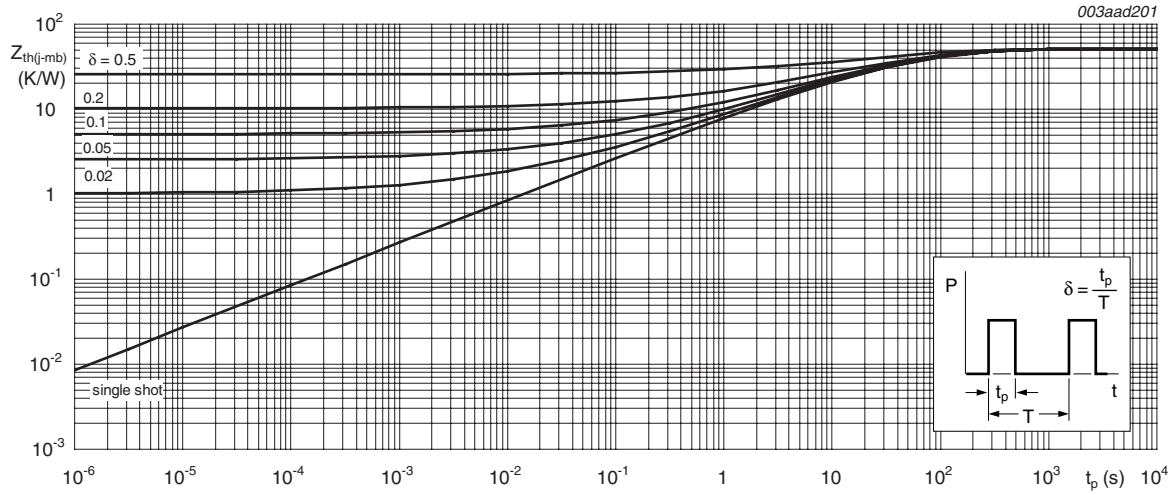


Fig 9. Transient thermal impedance from juction to ambient as a function of pulse duration, FET1 and FET2 (PCB used for thermal tests;heat sink area 400mm²)

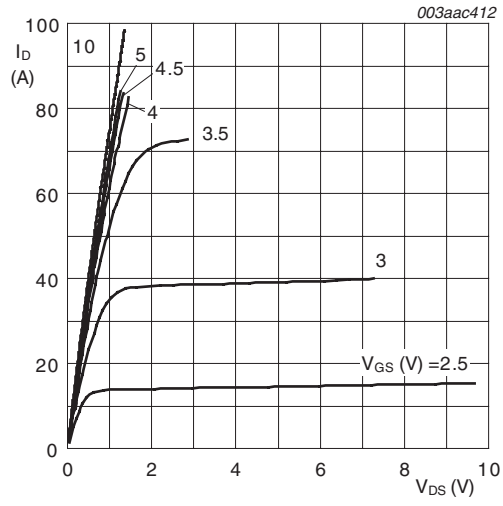
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics, FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	55	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 14; see Figure 15	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 14; see Figure 15	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 14; see Figure 15	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	3	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 150 °C	-	-	125	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	300	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A; T_j = 25 °C; see Figure 16; see Figure 17	-	13	15	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 150 °C; see Figure 16; see Figure 17	-	-	27.6	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; see Figure 16; see Figure 17	-	14.2	16.7	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; see Figure 16; see Figure 17	-	12.1	13.4	mΩ
I_D/I_{sense}	ratio of drain current to sense current	T_j = 25 °C; V_{GS} = 5 V; see Figure 18	5850	6500	7150	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	I_F = 250 µA; 25 °C < T_j < 150 °C; see Figure 19	-5.4	-5.7	-6	mV/K

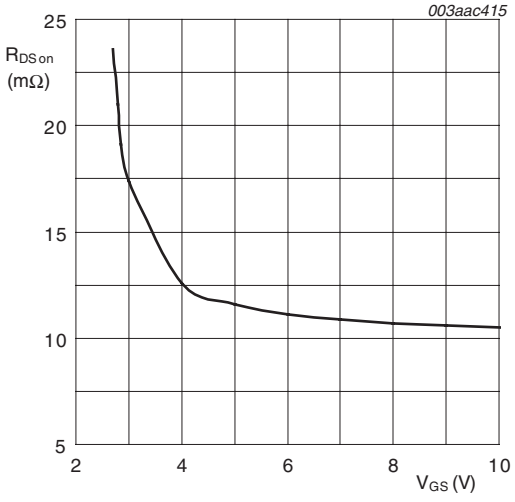
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{F(TSD)}$	temperature sense diode forward voltage	I_F = 250 µA; T_j = 25 °C; see Figure 19	2.855	2.9	2.945	V
Dynamic characteristics, FET1 and FET2						
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 44 V; V_{GS} = 5 V; see Figure 20	-	33	-	nC
Q_{GS}	gate-source charge		-	6.7	-	nC
Q_{GD}	gate-drain charge		-	13.3	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 21	-	2450	3267	pF
C_{oss}	output capacitance		-	360	432	pF
C_{rss}	reverse transfer capacitance		-	137	180	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 3 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω	-	35	-	ns
t_r	rise time		-	70	-	ns
$t_{d(off)}$	turn-off delay time		-	135	-	ns
t_f	fall time		-	61	-	ns
L_D	internal drain inductance	From pin to centre of die	-	0.85	-	nH
L_S	internal source inductance	From source lead to source bonding pad	-	1.9	-	nH
Source-drain diode, FET1 and FET2						
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 22	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V	-	44	-	ns
Q_r	recovered charge		-	88	-	nC



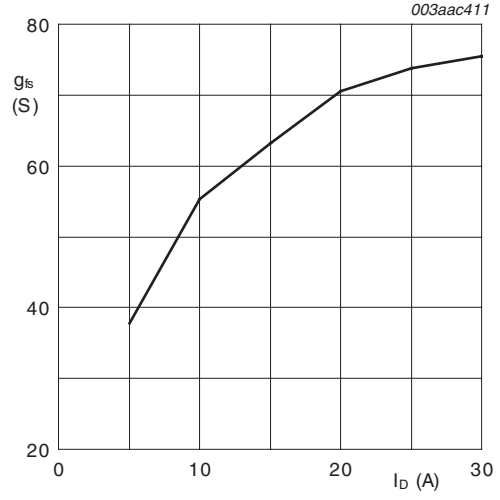
$T_j = 25\,°C; t_p = 300\,\mu s$

Fig 10. Output characteristics: drain current as a function of drain-source voltage; typical values, FET1 and FET2



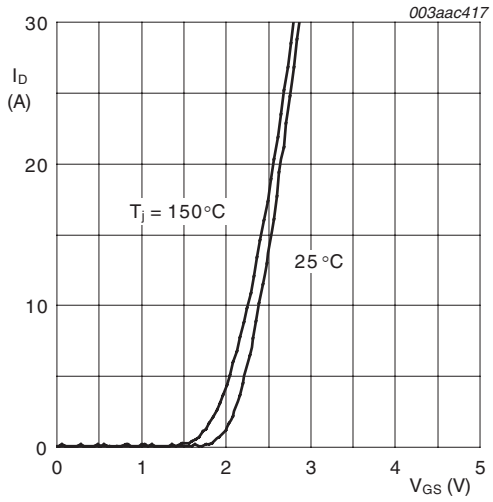
$T_j = 25\,°C; I_D = 10\,A$

Fig 11. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2



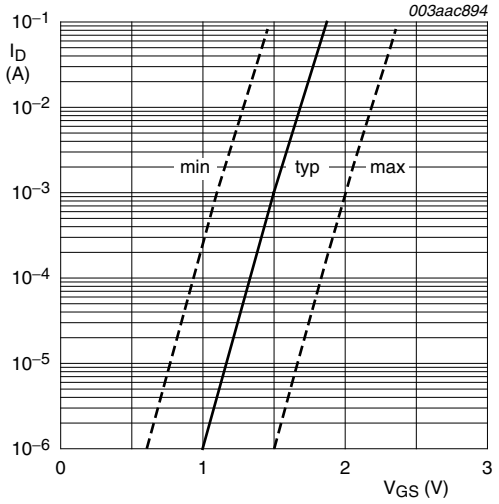
$T_j = 25\,°C; V_{DS} = 25\,V$

Fig 12. Forward transconductance as a function of drain current; typical values, FET1 and FET2



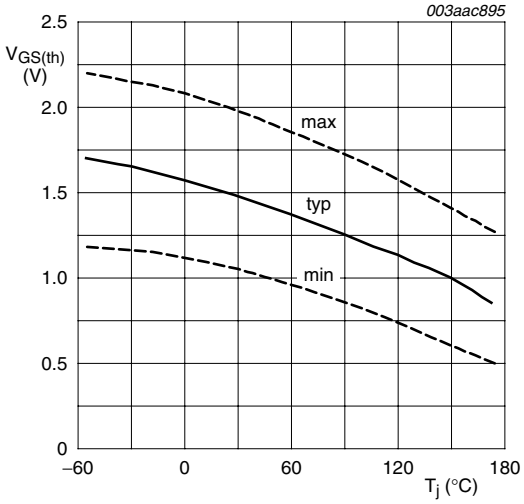
$V_{DS} = 25\,V$

Fig 13. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2



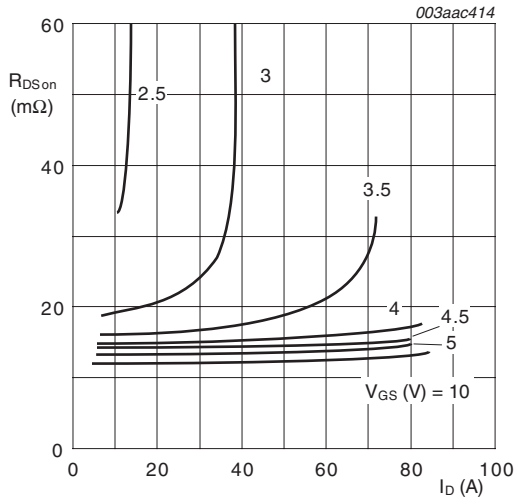
$T_j = 25\,°C; V_{DS} = V_{GS}$

Fig 14. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2



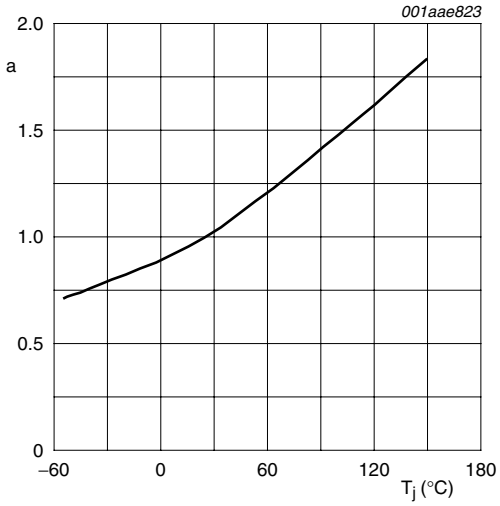
$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig 15. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



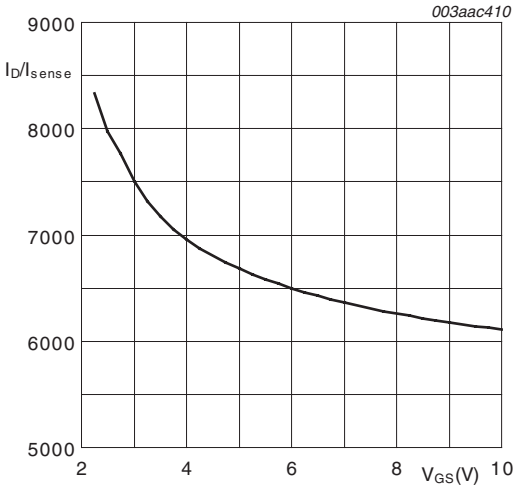
$T_j = 25\,°C; t_p = 300\,\mu s$

Fig 16. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



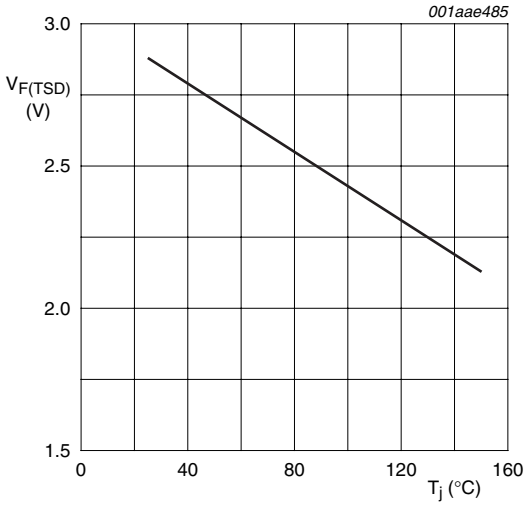
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 17. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



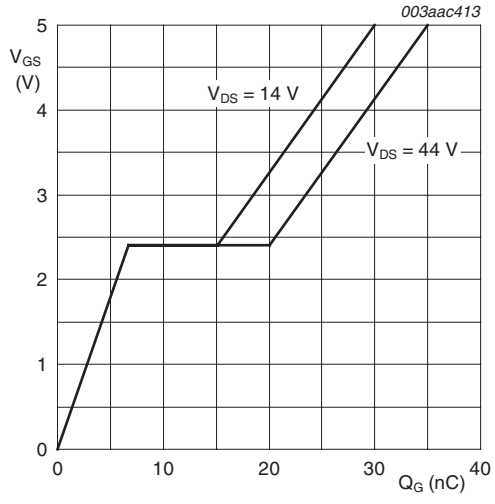
$T_j = 25\,°C; I_D = 5A$

Fig 18. Ratio of drain current to sense current as a function of gate-source voltage; typical values, FET1 and FET2



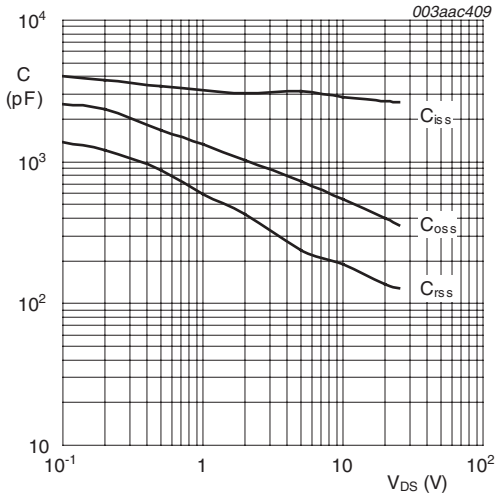
$I_F = 250\,\mu A$

Fig 19. Temperature sense diode forward voltage as a function of junction temperature; typical values, FET1 and FET2



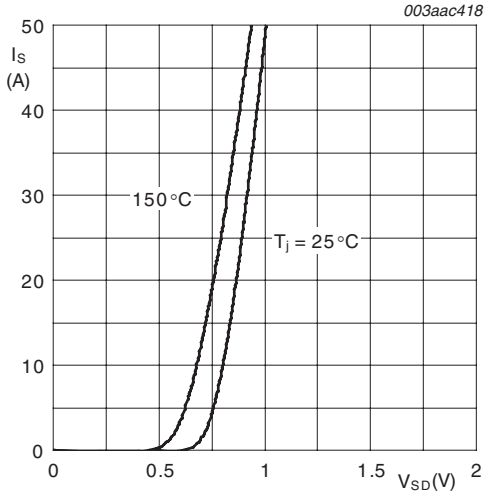
$T_j = 25\,°C; I_D = 10A$

Fig 20. Gate-source voltage as a function of turn-on gate charge; typical values, FET1 and FET2



$V_{GS} = 0\,V; f = 1MHz$

Fig 21. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

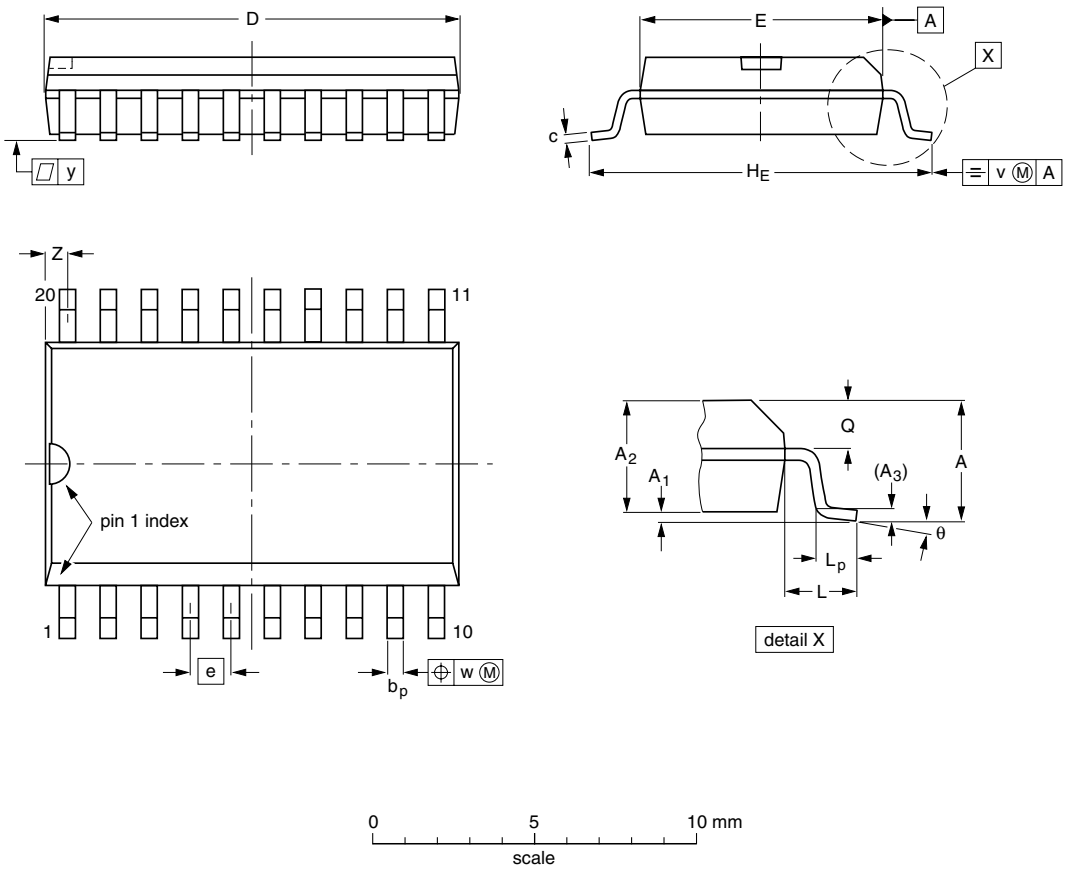


$V_{GS} = 0\,V$

Fig 22. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

7. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 23. Package outline SOT163-1

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9MJJ-55PTT_1	20090514	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

9.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

TrenchMOS — is a trademark of NXP B.V.

10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 May 2009
Document identifier: BUK9MJJ-55PTT_1