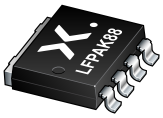

BUK7S1R0-40H

N-channel 40 V, 1.0 mΩ standard level MOSFET in LFPAK88

10 January 2025 **Product data sheet**

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a copper-clip LFPAK88 package. This product has been fully designed and qualified to meet beyond AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Fully automotive qualified to beyond AEC-Q101:
  - -55 °C to +175 °C rating suitable for thermally demanding environments
- LFPAK88 package:
  - Designed for smaller footprint and improved power density over older wire bond packages such as D²PAK for today's space constrained high power automotive applications
  - Thin package and copper clip enables LFPAK88 to be highly efficient thermally
- LFPAK copper clip technology enabling improvements over wire bond packages by:
  - Increased maximum current capability and excellent current spreading
  - Improved R_{DSon}
  - Low source inductance
  - Low thermal resistance R_{th}
- LFPAK Gull Wing leads:
  - Flexible leads enabling high Board Level Reliability absorbing mechanical and thermal cycling stress, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- Unique 40 V Trench 9 superjunction technology:
  - Reduced cell pitch and superjunction platform enables lower R_{DSon} in the same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs

3. Applications

- 12 V automotive systems
- 48 V DC/DC systems (on 12 V secondary side)
- Higher power motors, lamps and solenoid control
- Reverse polarity protection
- LED lighting
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	325	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	375	W

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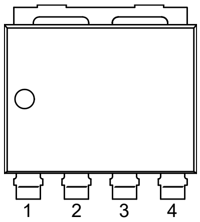
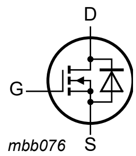
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		0.62	0.88	1	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	17	34	nC
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V	[2]	-	49	-	nC
S	softness factor	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	0.8	-	

[1] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7S1R0-40H	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7S1R0-40H	`7S1R040H`

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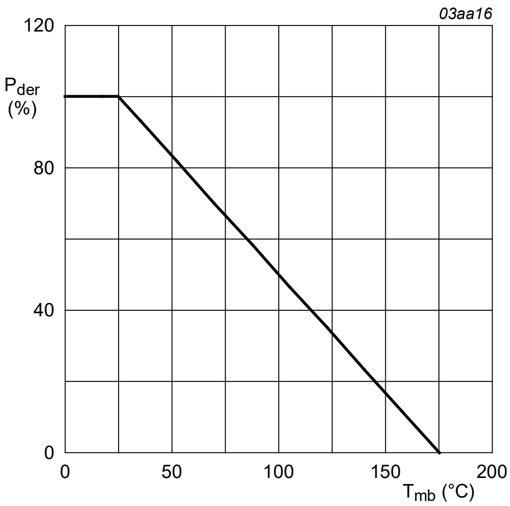
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

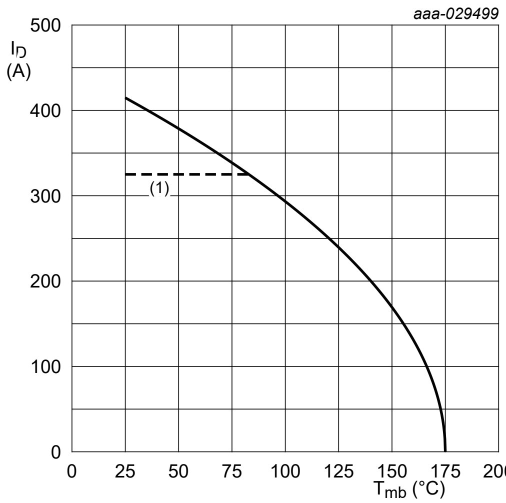
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage		[1]	-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	375	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[2]	-	325	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3; Fig. 4	[2]	-	1659	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[2]	-	350	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1659	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 120 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 5	[3] [4]	-	437	mJ

[1] Refer to application note AN90001 for further information.
[2] This current had been successfully demonstrated during product characterisation. In practical applications the current will be limited by PCB, thermal design and operating temperature.
[3] Single pulse avalanche rating limited by maximum junction temperature of 175°C.
[4] Refer to application note AN10273 for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V
(1) 325A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

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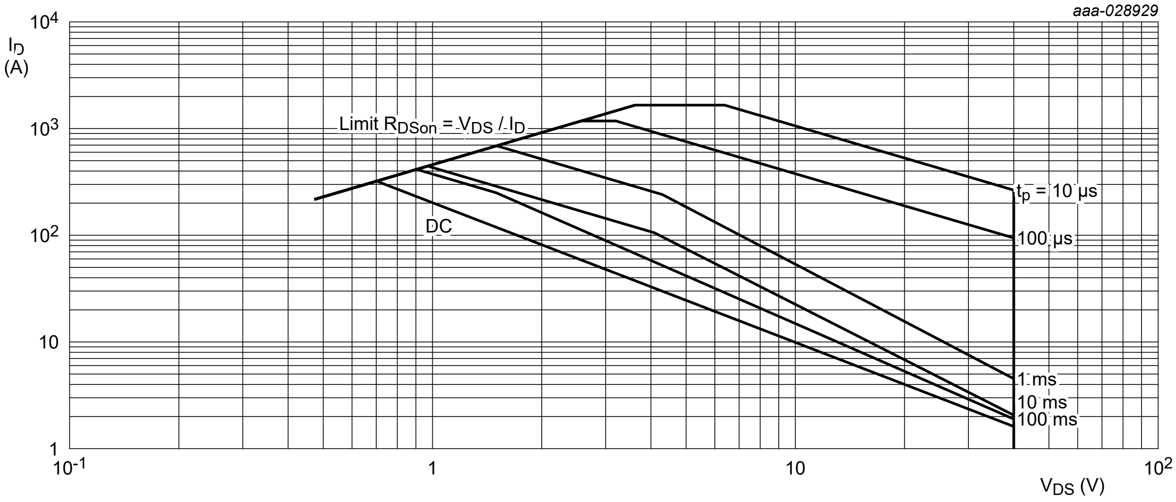
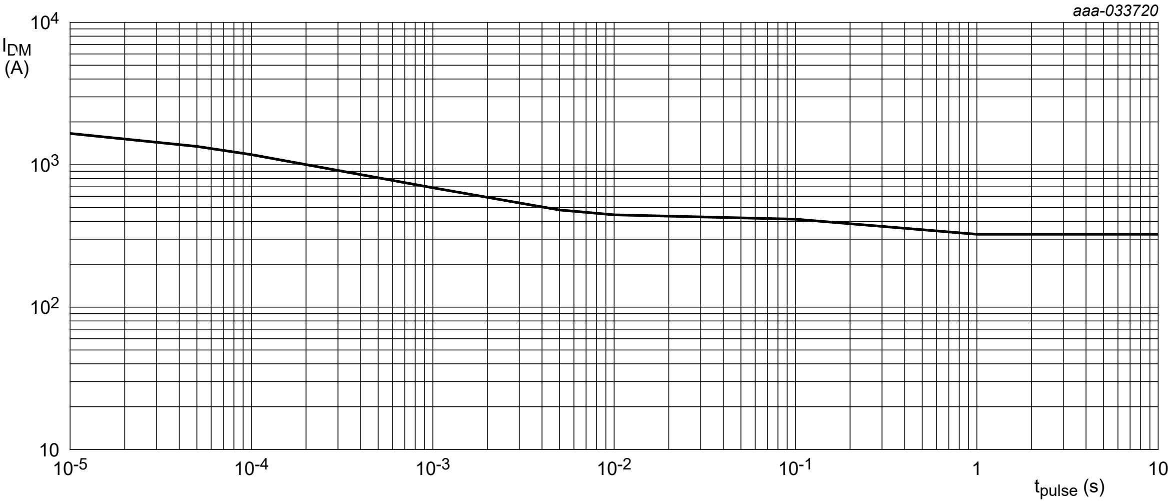


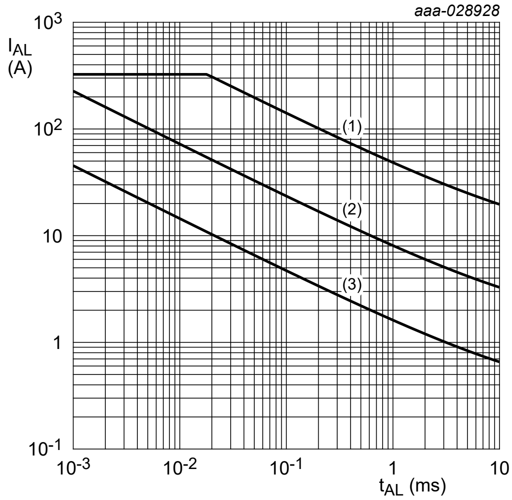
T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



V_{GS} = 10V ; T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 4. Peak Current Capability



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	0.35	0.4	K/W

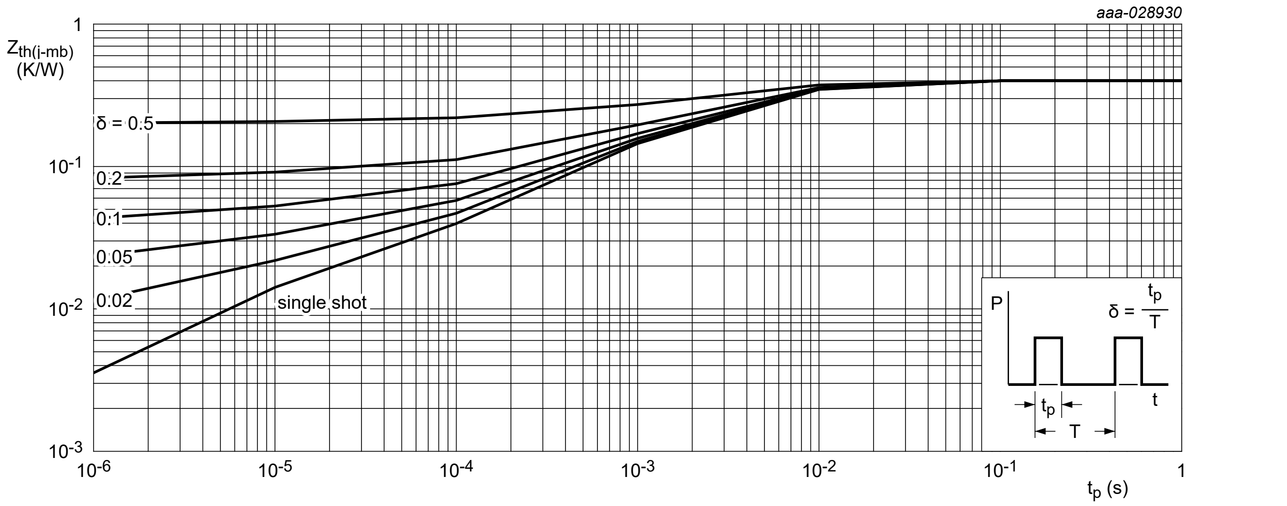

Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -40 °C		-	40.5	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 11		1	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 11		-	-	4.3	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.2	1.5	μA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	4.7	25	μA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C		-	287	1000	μA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

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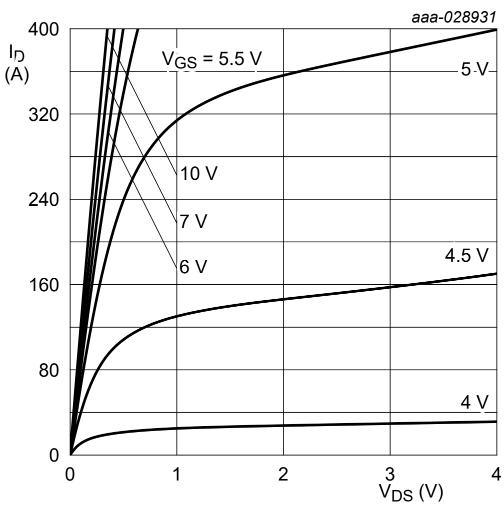
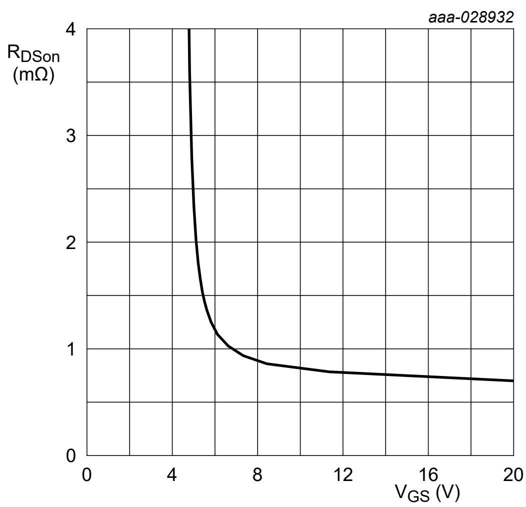
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		0.62	0.88	1	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 13		0.87	1.3	1.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 13		0.97	1.4	1.75	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 13		1.2	1.8	2.2	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.4	0.9	2.3	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	98	137	nC
Q_{GS}	gate-source charge			-	27	40	nC
Q_{GD}	gate-drain charge			-	17	34	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	7373	10322	pF
C_{oss}	output capacitance			-	1578	2209	pF
C_{rss}	reverse transfer capacitance			-	295	649	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	23	-	ns
t_r	rise time			-	19	-	ns
$t_{d(off)}$	turn-off delay time			-	59	-	ns
t_f	fall time			-	26	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.76	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V		-	43	-	ns
Q_r	recovered charge		[1]	-	49	-	nC
S	softness factor	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	0.8	-	
		I_S = 25 A; dI_S/dt = -500 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C		-	0.7	-	

[1] includes capacitive recovery



T_j = 25 °C

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values



T_j = 25 °C; I_D = 25 A

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

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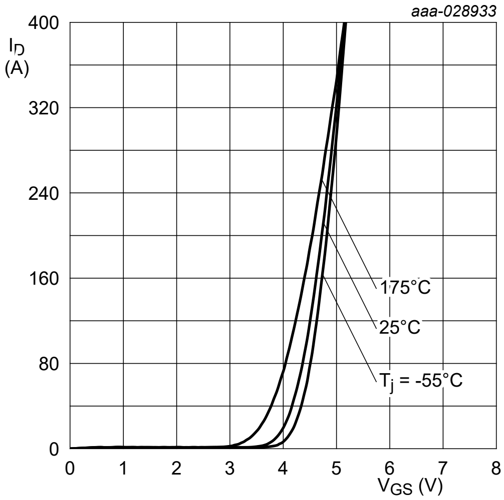
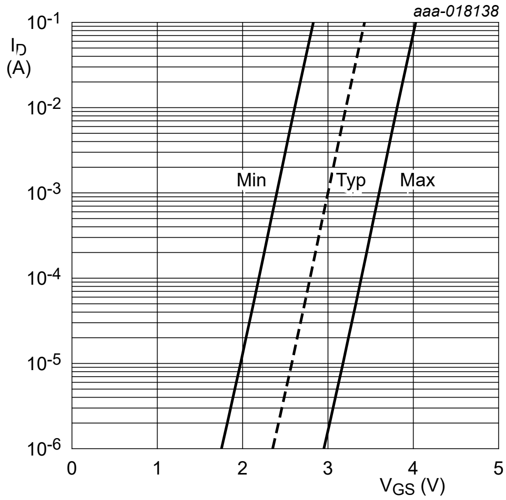


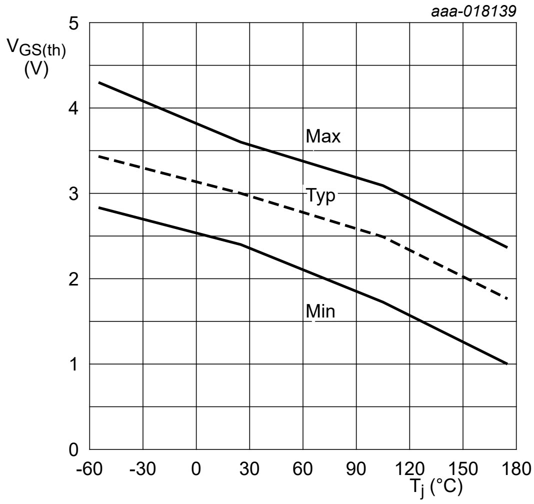
V_{DS} = 8 V

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



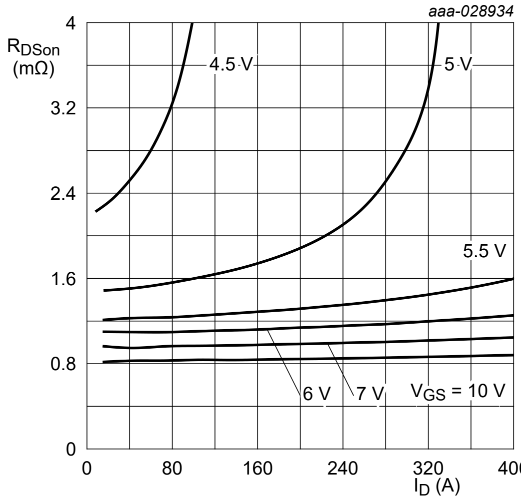
T_j = 25 °C; V_{DS} = 5 V

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 11. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

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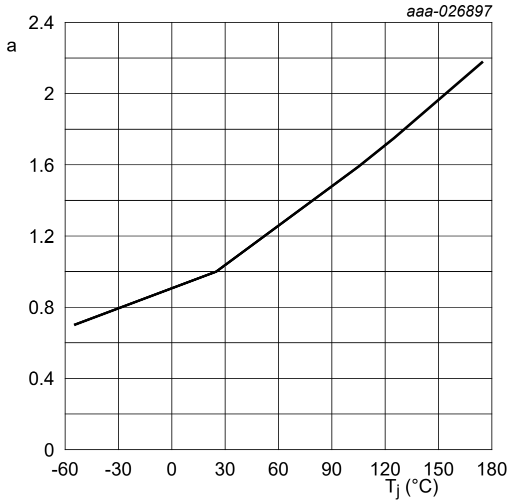
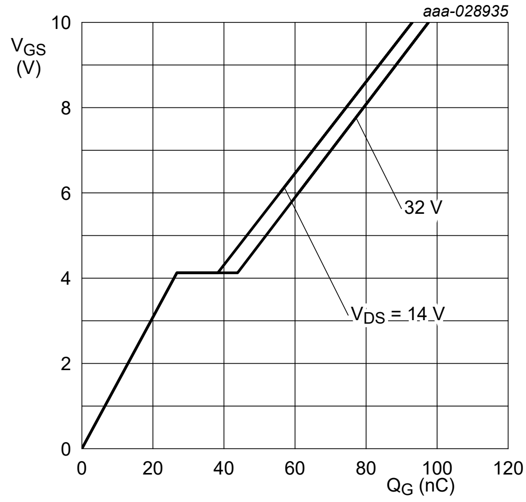


$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

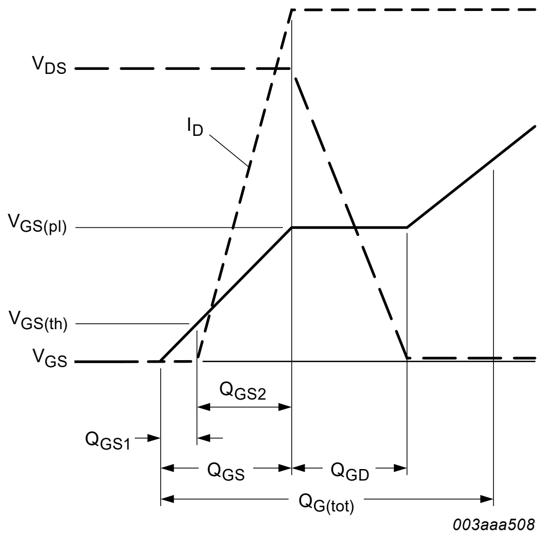
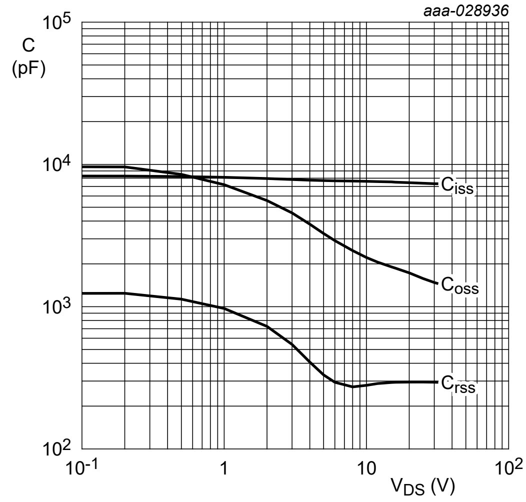


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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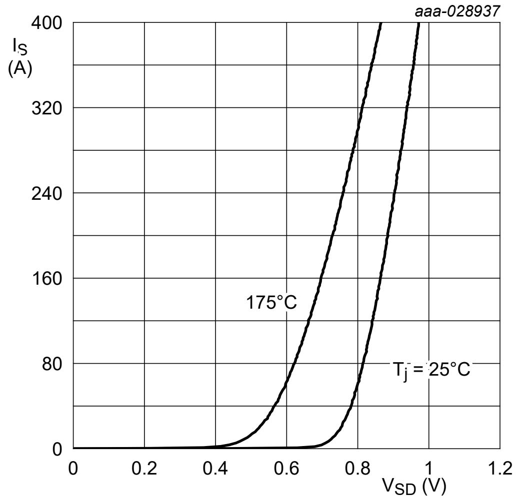

V_{GS} = 0 V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

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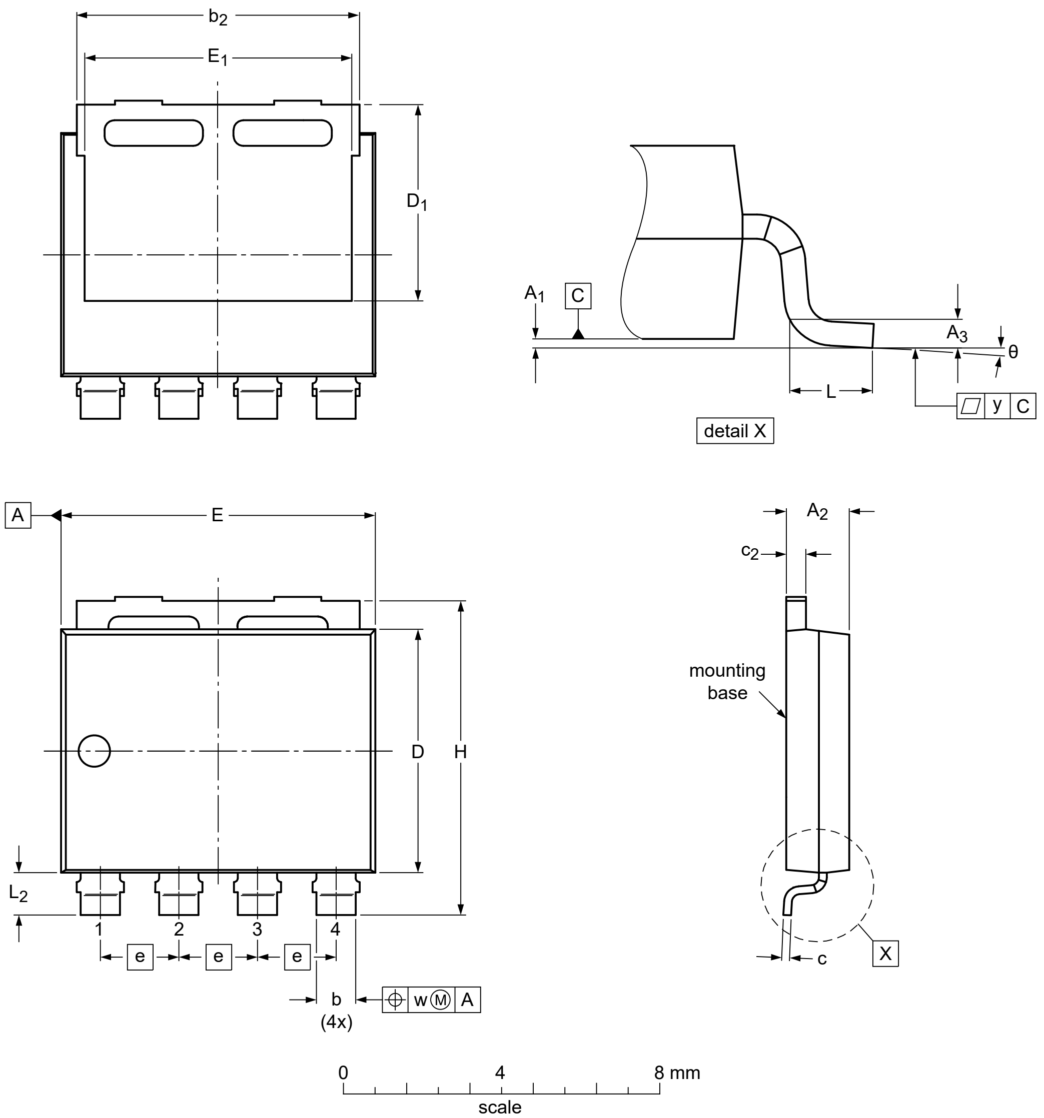
11. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads **SOT1235**



Dimensions (mm are the original dimensions)

Unit		A_1	A_2	A_3	b	b_2	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H(1)	L	L_2	w	y	θ
mm	max	0.15	1.7		1.1	7.3	0.24	0.55	6.3	5.1	8.1	6.9		8.1	0.8	1.3			8°
	nom			0.25									2.0				0.25	0.10	
	min	0.00	1.5		0.9	7.1	0.18	0.45	6.1	4.9	7.9	6.7		7.8	0.6	0.9			0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1235_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1235						~~17-08-02~~ 17-08-07

Fig. 18. Package outline LFPAK88 (SOT1235)

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12. Soldering

Footprint information for reflow soldering of LFPAK88 package **SOT1235**

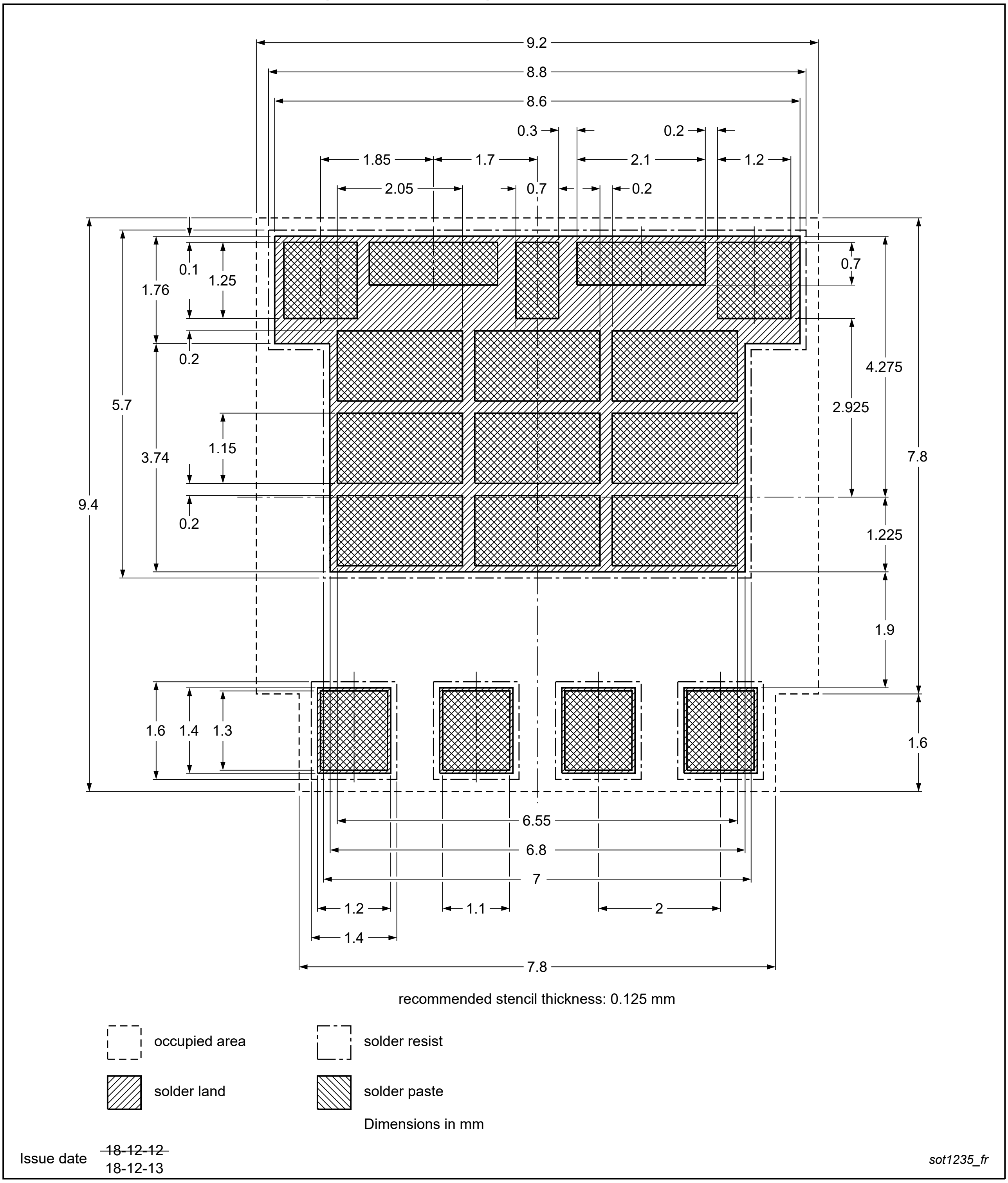

Fig. 19. Reflow soldering footprint for LFPAK88 (SOT1235)

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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