

BUK7Q9R5-40H

Standard level N-Channel MOSFET in MLPAK33-WF (SOT8002-3D)

28 August 2025

Product data sheet

1. General description

Standard level N-Channel MOSFET in a compact MLPAK33-WF (SOT8002-3D) package using Trench 9 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- · Trench 9 technology Designed for ruggedness
- Small footprint (3 x 3 mm) for compact design
- Qualified to AEC-Q101 at 175 °C
- · Side-wettable flanks for robust solder joints and automated optical inspection

3. Applications

- Motor drive
- Battery protection
- DC-DC Conversion

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	-	-	51	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	-	47	W
Tj	junction temperature		-55	-	175	°C
Static charac	teristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11	5	7.2	9.5	mΩ
Dynamic cha	racteristics			,		
Q_{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 20 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 13; Fig. 14	-	2	4	nC



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	1 2 3 4 	
2	S	source		D
3	S	source		
4	G	gate		_G (LE本)
mb	D	Mounting base; connected to drain	MLPAK33-WF (SOT8002-3)	mbb076 S

6. Ordering information

Table 3. Ordering information

Type number	Package						
	Name	Description	Version				
BUK7Q9R5-40H		plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals;pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3				

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Q9R5-40H	1NF

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V
V_{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>	-	47	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	-	51	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>	-	36	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$; Fig. 3	-	202	Α
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drai	n diode		,		
Is	source current	T _{mb} = 25 °C	-	39	Α
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	202	Α

Symbol	Parameter	Conditions		Min	Max	Unit		
Avalanche rugg	Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 22.5 A; $V_{sup} \le 40$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 82 μs; Fig. 4	[1] [2]	-	47.8	mJ		
I _{AS}	non-repetitive avalanche current	$V_{sup} \le 40 \text{ V}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25 \text{ °C};$ $R_{GS} = 50 \Omega; Fig. 4$	[3]	-	42	Α		

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.
- [3] Protected by 100% test

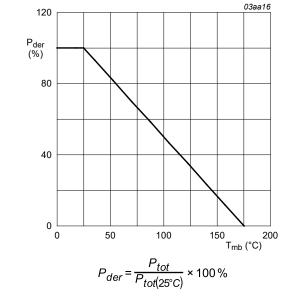


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

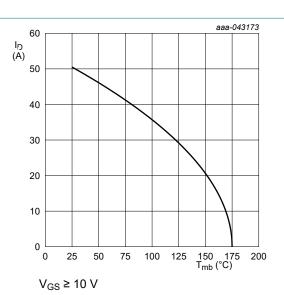
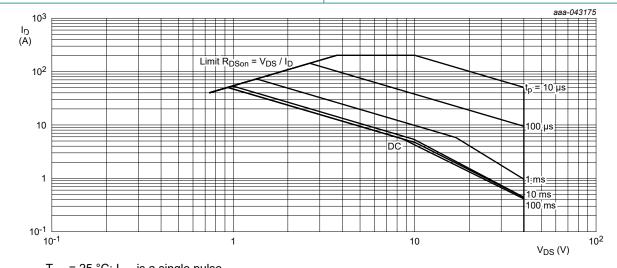
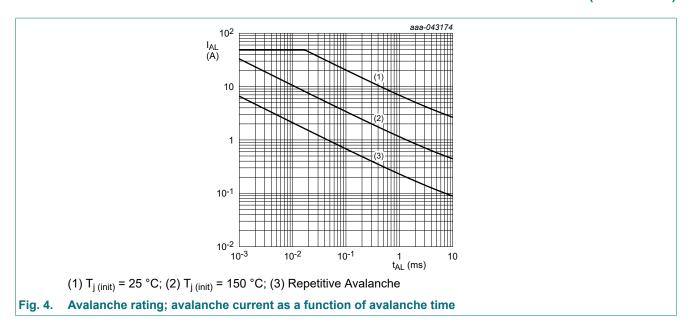


Fig. 2. Continuous drain current as a function of mounting base temperature



 T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

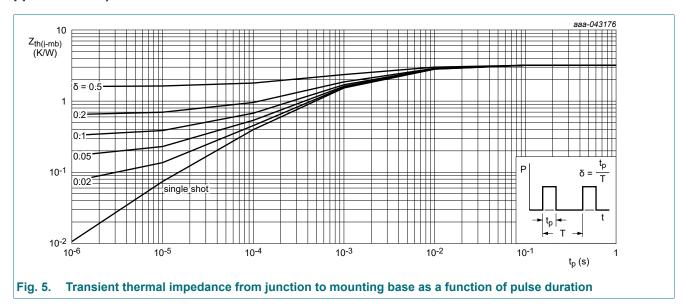


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5		-	2.66	3.19	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	40	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _i = 25 °C	40	44	-	V
, ,	breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _i = -40 °C	-	40.5	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	36	40	-	V
00()	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	2.4	3	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 10$	-	-	4.3	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.01	1	μΑ
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	5	7.2	9.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 105 \text{ °C};$ Fig. 12	6.7	10	14	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 125 °C; Fig. 12	7.2	10.9	15.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 °C;$ Fig. 12	8.5	13	18.2	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	1	2.4	6	Ω
Dynamic cl	naracteristics			'	'	
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 20 V; V _{GS} = 10 V;	-	14	20	nC
Q _{GS}	gate-source charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	4	6	nC
Q _{GD}	gate-drain charge		-	2	4	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz;	-	908	1271	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>	-	283	396	pF
C _{rss}	reverse transfer capacitance	_	-	51	112	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 2 Ω; V _{GS} = 10 V;	-	4.1	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 ^{\circ}C$	-	3.3	-	ns
$t_{d(off)}$	turn-off delay time	1	-	12	-	ns
t _f	fall time	1	-	3.8	-	ns
Source-dra	in diode	•		'	<u> </u>	1
V _{SD}	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$	-	0.8	1.2	V
		•	+ + + + + + + + + + + + + + + + + + + +			_
t _{rr}	reverse recovery time	$I_S = 10 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 20 \text{ V}$; $T_i = 25 ^{\circ}\text{C}$; $\overline{\text{Fig. } 17}$	-	17	-	ns

^[1] includes capacitive recovery

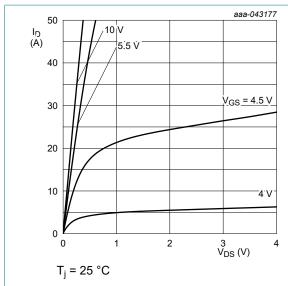


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

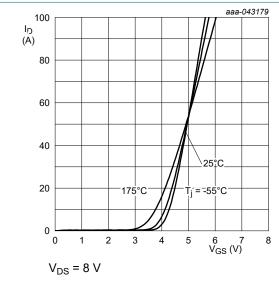


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

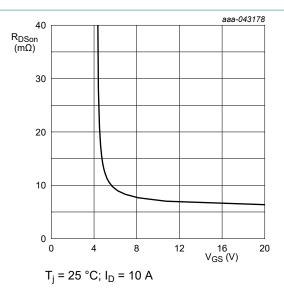


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

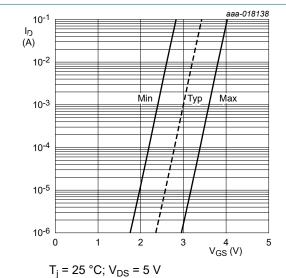


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

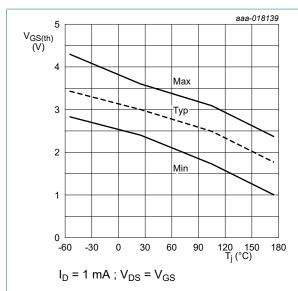


Fig. 10. Gate-source threshold voltage as a function of junction temperature

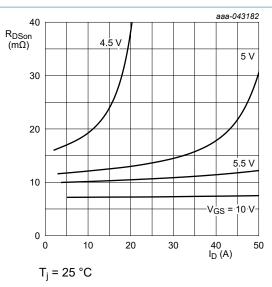


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

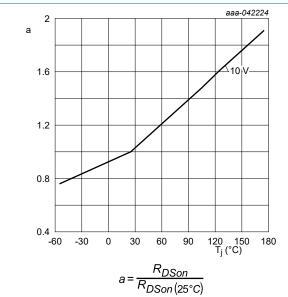


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

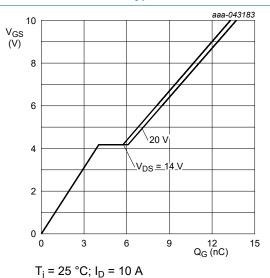


Fig. 13. Gate-source voltage as a function of gate charge; typical values

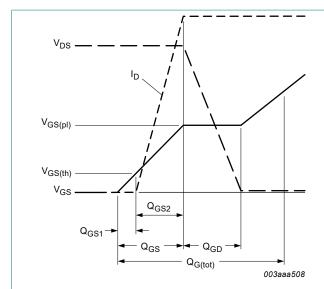


Fig. 14. Gate charge waveform definitions

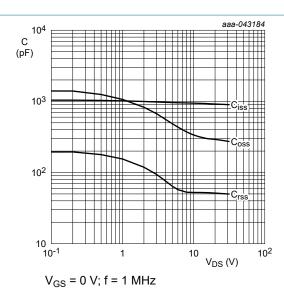


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical

values

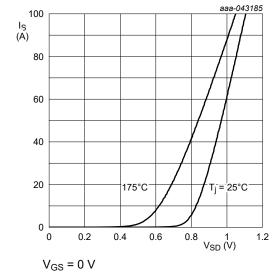


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

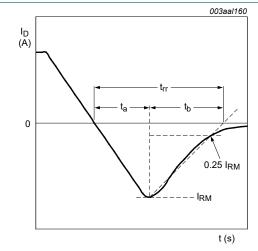


Fig. 17. Reverse recovery timing definition

11. Package outline

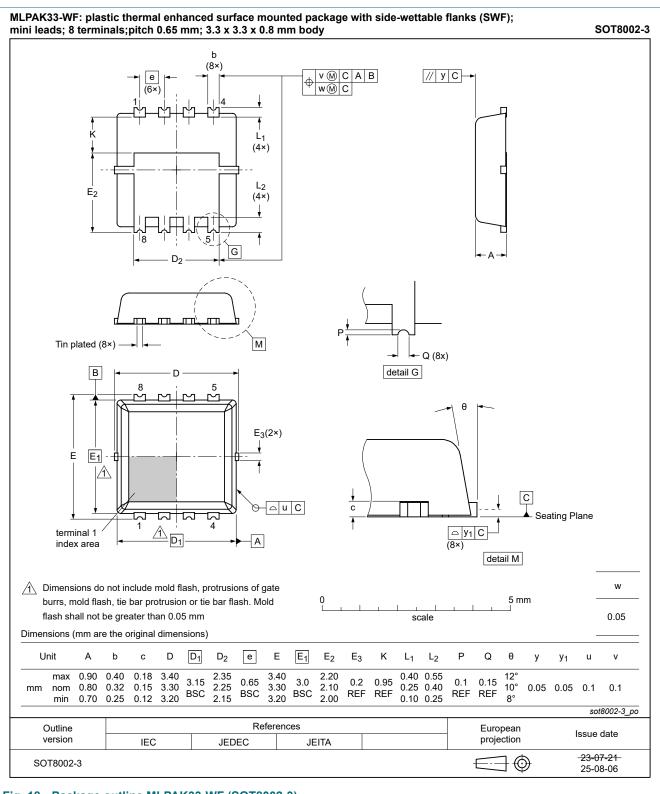
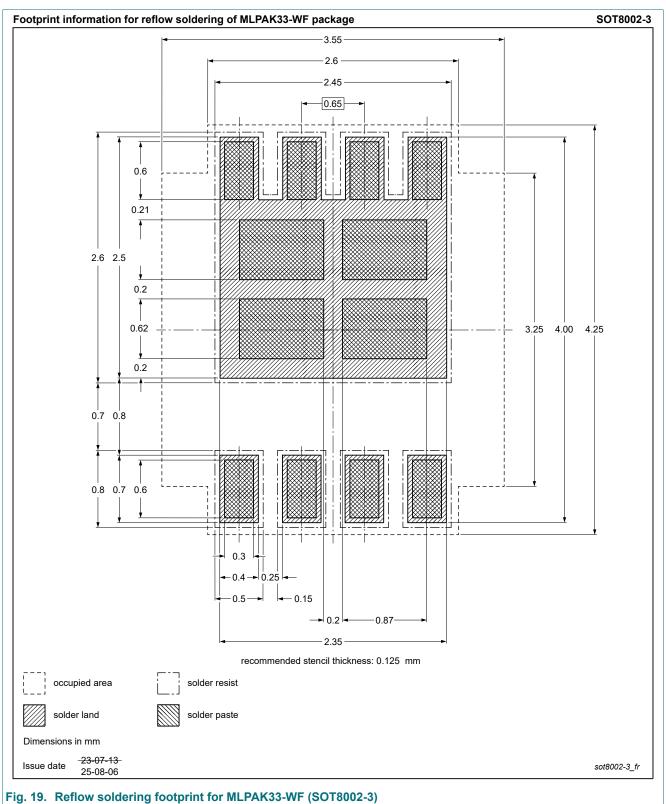


Fig. 18. Package outline MLPAK33-WF (SOT8002-3)

12. Soldering



13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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