



BUK7Q8R4-40H

Standard level N-Channel MOSFET in MLPAK33-WF
(SOT8002-3D)

28 August 2025

Product data sheet

1. General description

Standard level N-Channel MOSFET in a compact MLPAK33-WF (SOT8002-3D) package using Trench 9 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Trench 9 technology - Designed for ruggedness
- Small footprint (3 x 3 mm) for compact design
- Qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automated optical inspection

3. Applications

- Motor drive
- Battery protection
- DC-DC Conversion

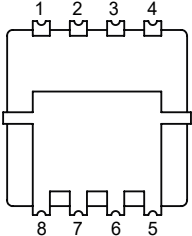
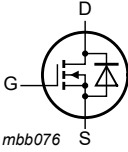
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	57	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	51	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	4.9	7	8.4	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 15\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	3	6	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33-WF (SOT8002-3)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Q8R4-40H	MLPAK33-WF	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Q8R4-40H	1NE

8. Limiting values

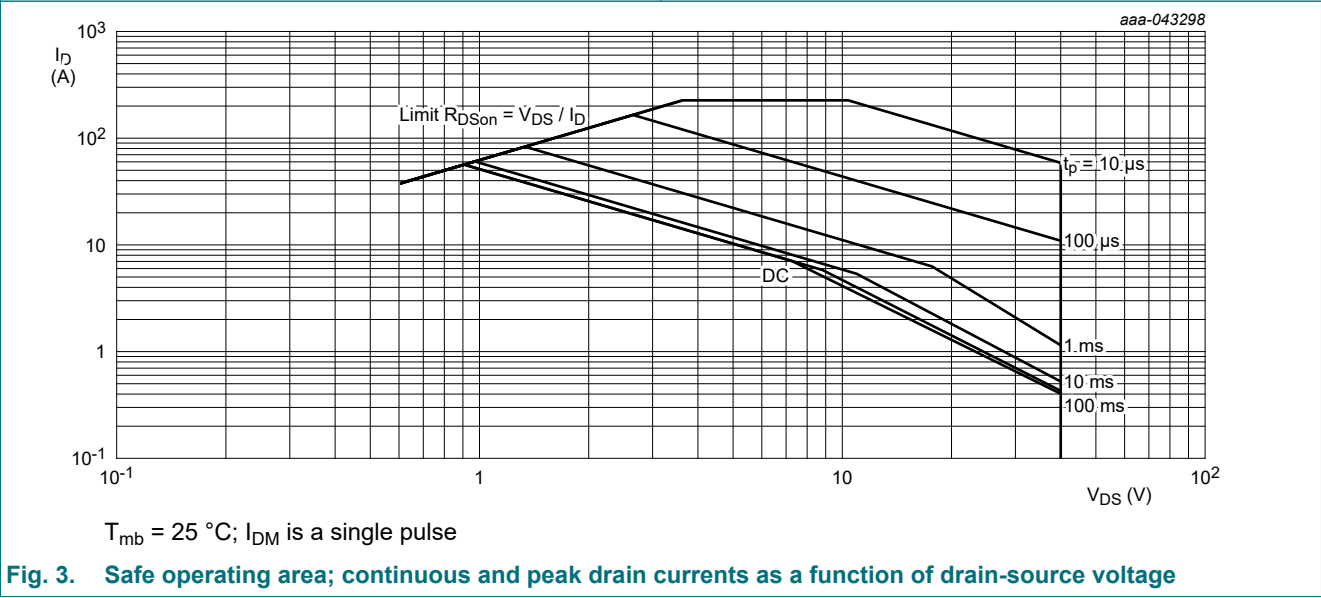
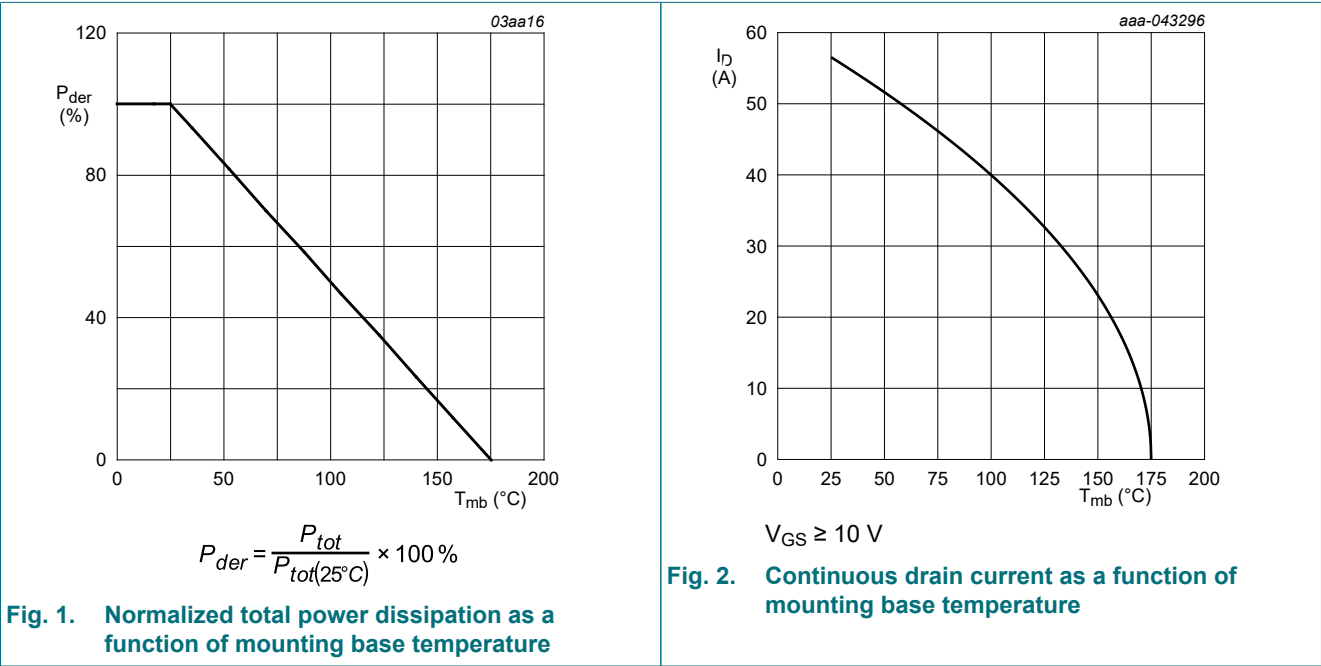
Table 5. Limiting values

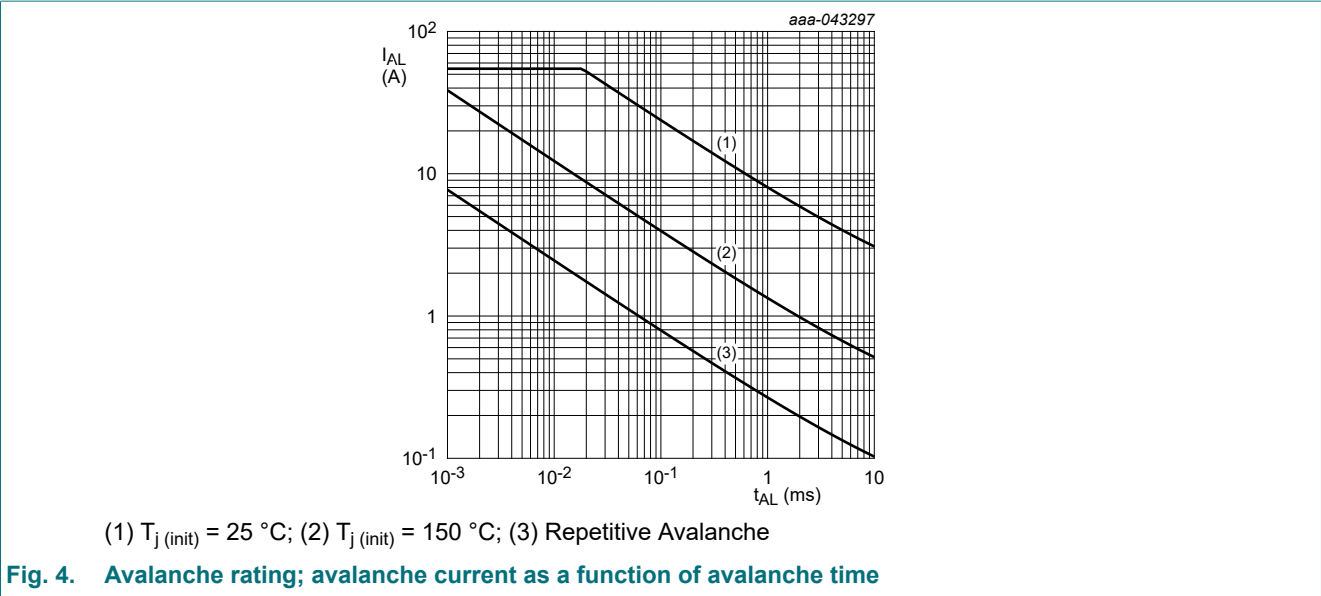
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	51	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	57	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	40	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	226	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	43	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	226	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{J(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 90\text{ }\mu\text{s}$; Fig. 4	[1] [2]	-	58.7	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{J(\text{init})} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[3]	-	48	A

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.
- [3] Protected by 100% test



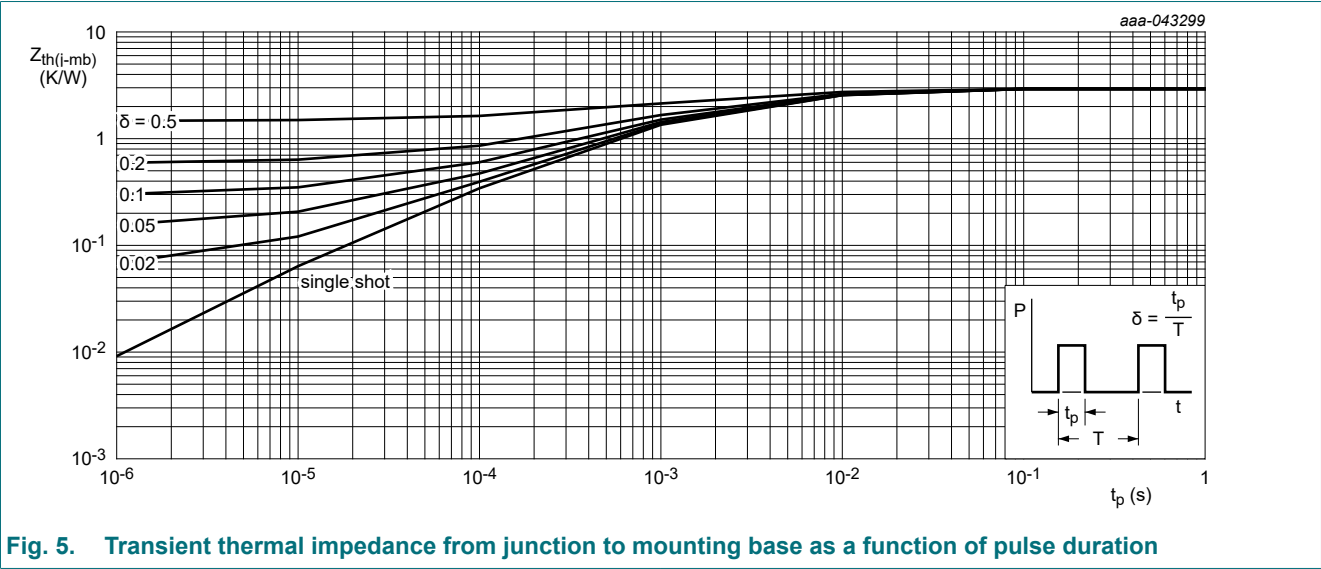


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	2.44	2.92	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	40	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		40	44	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -40 °C		-	40.5	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		36	40	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 9 ; Fig. 10		2.4	3	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C; Fig. 10		1	-	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C; Fig. 10		-	-	4.3	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C		-	0.01	1	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _J = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _J = 25 °C; Fig. 11		4.9	7	8.4	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _J = 105 °C; Fig. 12		6.5	9.3	12.4	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _J = 125 °C; Fig. 12		7.1	10	13.5	mΩ
		V _{GS} = 10 V; I _D = 15 A; T _J = 175 °C; Fig. 12		8.4	12	16	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C		1	2.5	6.3	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 15 A; V _{DS} = 20 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	16	22	nC
Q _{GS}	gate-source charge			-	5	7.5	nC
Q _{GD}	gate-drain charge			-	3	6	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15		-	1093	1530	pF
C _{oss}	output capacitance			-	293	410	pF
C _{rss}	reverse transfer capacitance			-	56	123	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 1.3 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	4.7	-	ns
t _r	rise time			-	4.3	-	ns
t _{d(off)}	turn-off delay time			-	13	-	ns
t _f	fall time			-	4.3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 15 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 15 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C; Fig. 17		-	18	-	ns
Q _r	recovered charge		[1]	-	10	-	nC

[1] includes capacitive recovery

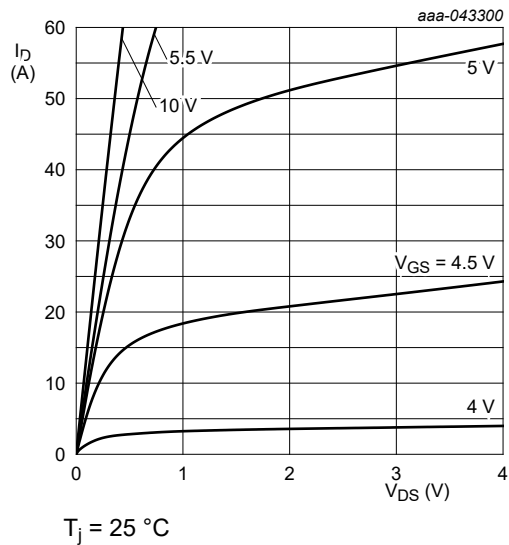


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

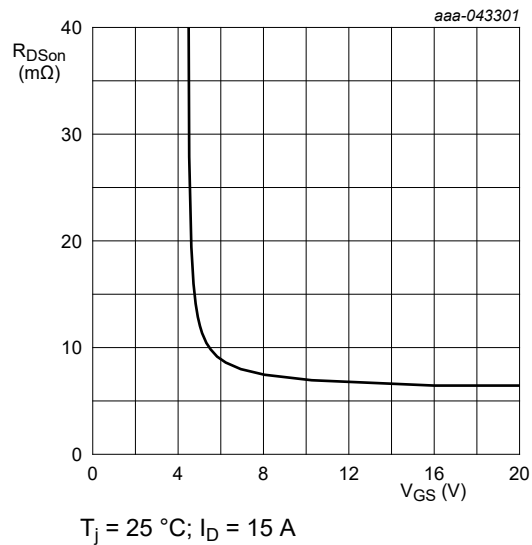


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

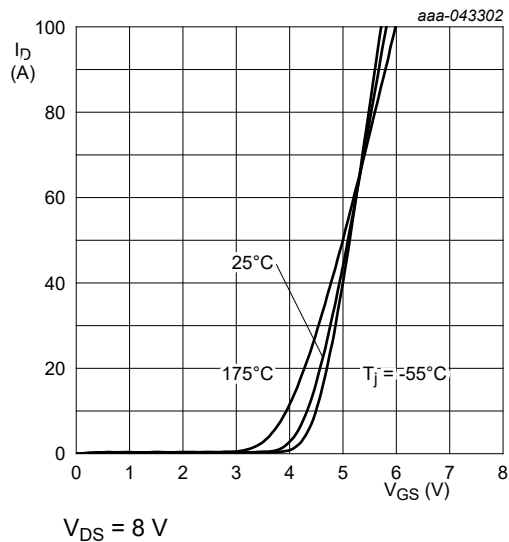


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

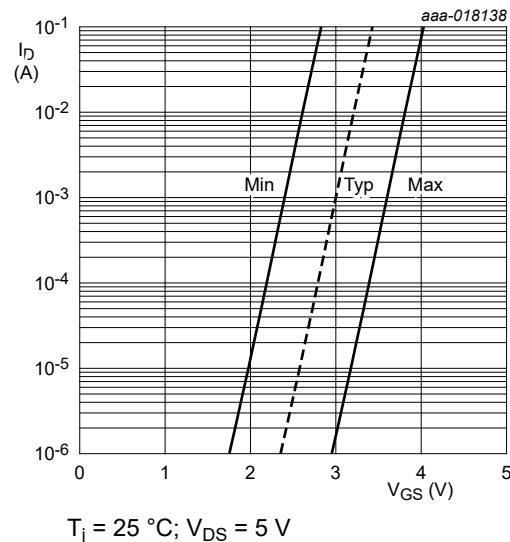


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

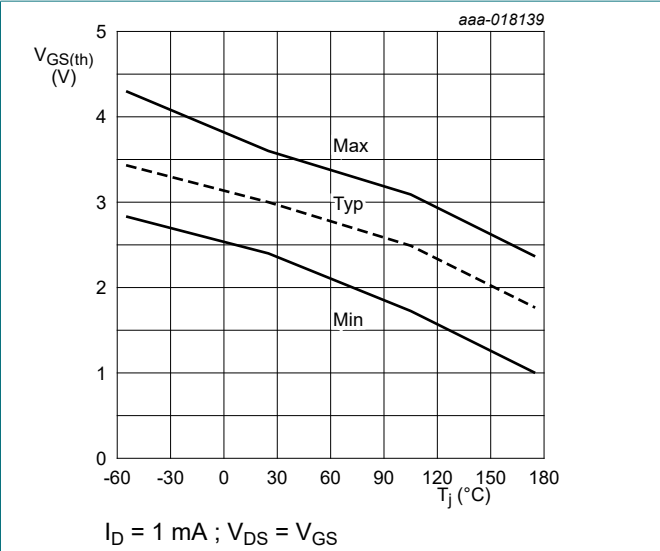


Fig. 10. Gate-source threshold voltage as a function of junction temperature

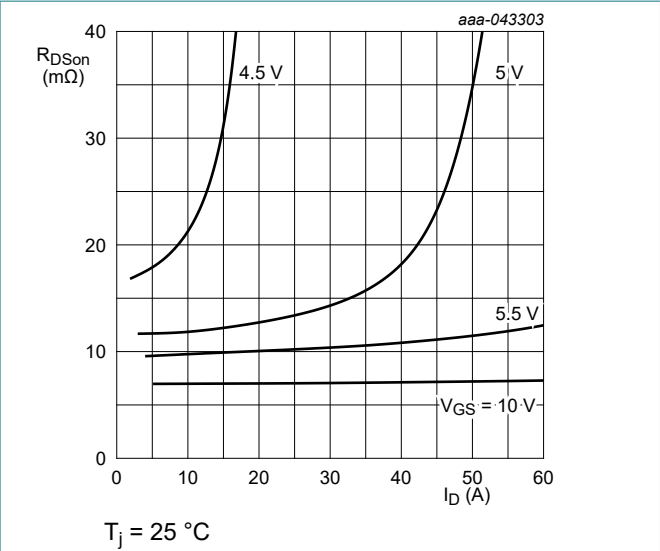


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

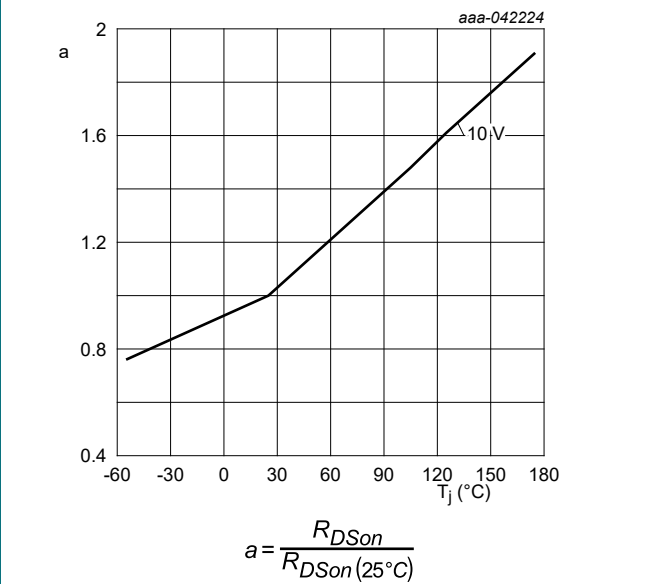


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

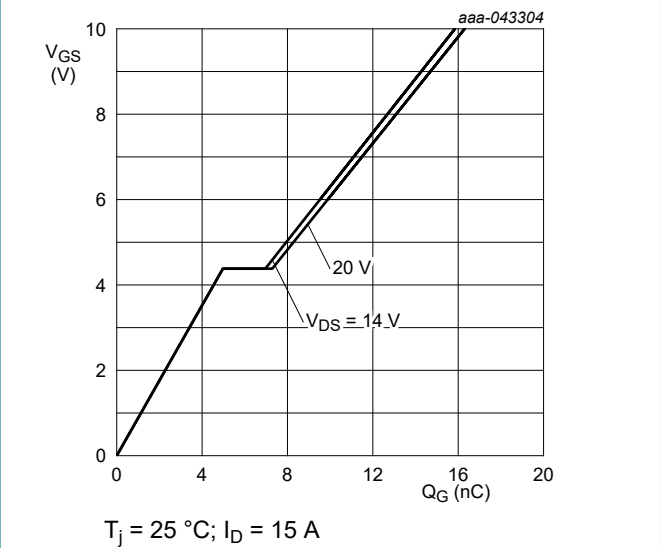


Fig. 13. Gate-source voltage as a function of gate charge; typical values



Fig. 14. Gate charge waveform definitions

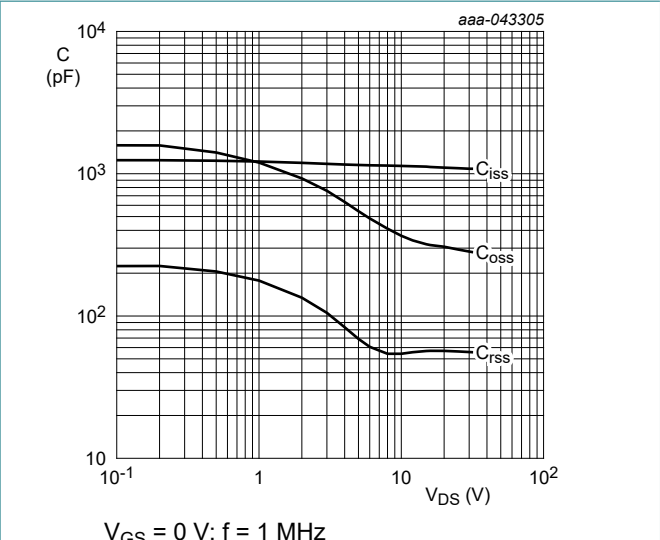


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

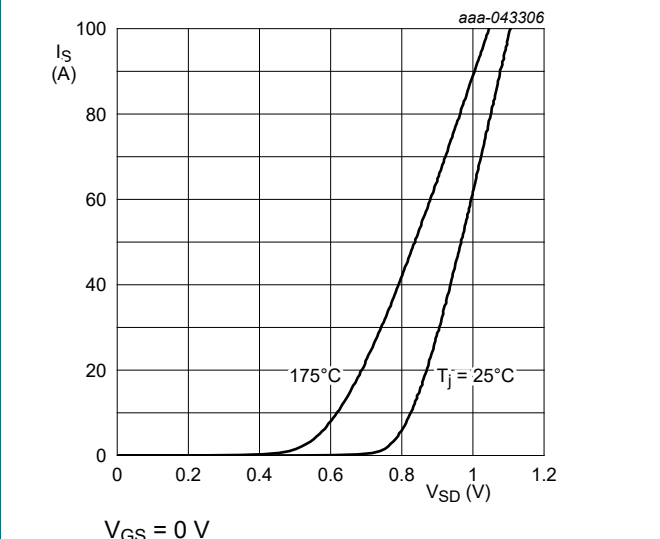


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

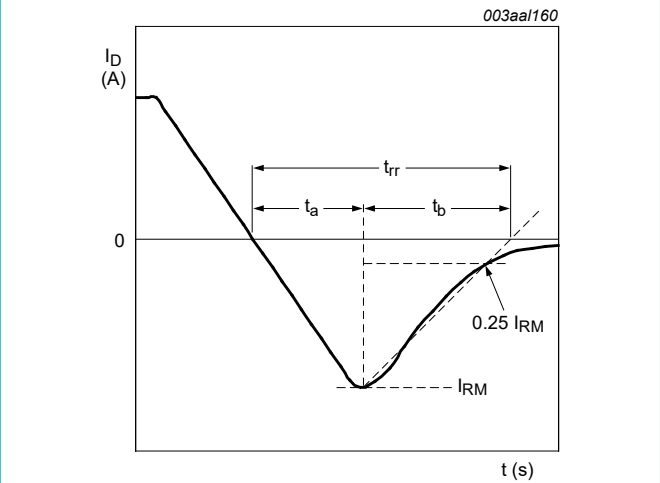


Fig. 17. Reverse recovery timing definition

11. Package outline

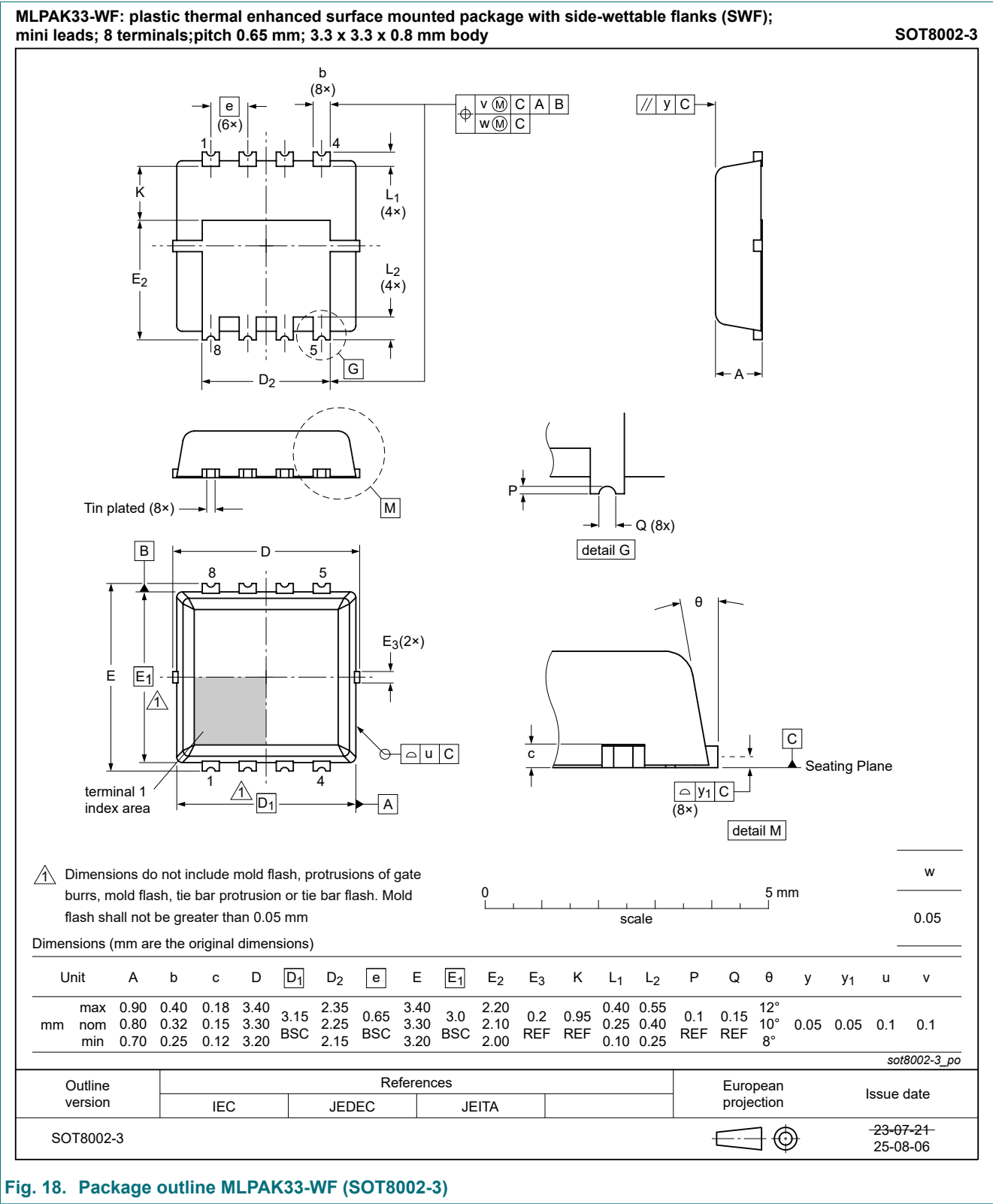
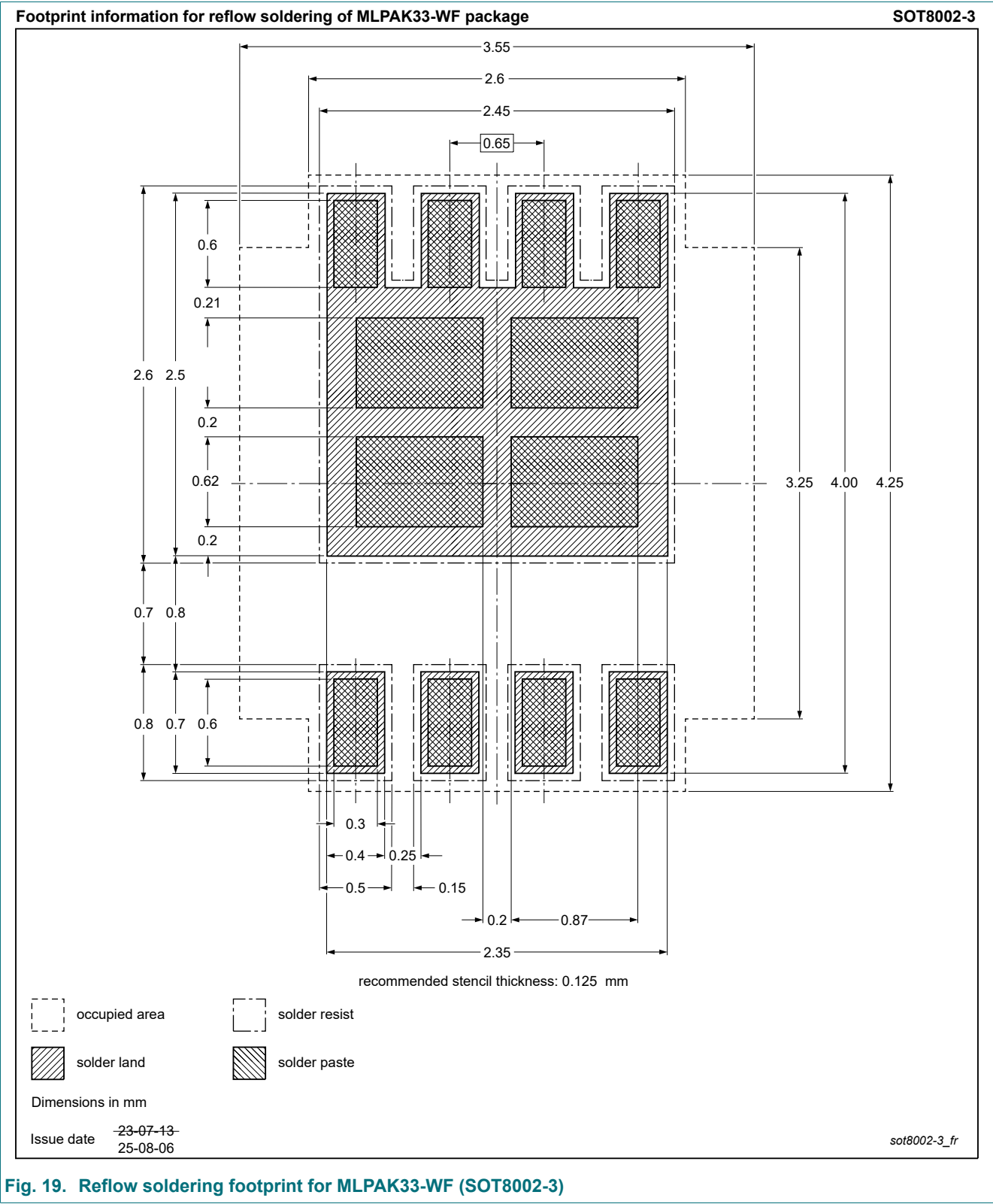


Fig. 18. Package outline MLPAK33-WF (SOT8002-3)

12. Soldering



13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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