

# BUK7Q4R9-40H

Standard level N-Channel MOSFET in MLPAK33-WF  
(SOT8002-3D)

7 May 2025

Product data sheet

## 1. General description

Standard level N-Channel MOSFET in a small MLPAK33-WF (SOT8002-3D) package using Trench 9 technology. This product has been designed and qualified to meet AEC-Q101 requirements delivering high performance and reliability.

## 2. Features and benefits

- Trench 9 technology
- Small footprint (3 x 3 mm) for compact design
- Qualified to AEC-Q101 at 175 °C
- Side-wettable flanks for robust solder joints and automated optical inspection

## 3. Applications

- Motor drive
- Battery protection
- DC-DC Conversion

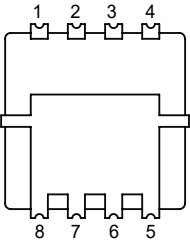
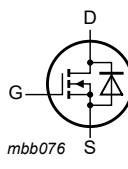
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	70	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	84	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	2.87	4.1	4.9	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 20\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	4	8	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-3)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Q4R9-40H	MLPAK33	plastic thermal enhanced surface mounted package with side-wettable flanks (SWF); mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-3

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Q4R9-40H	6AS

8. Limiting values

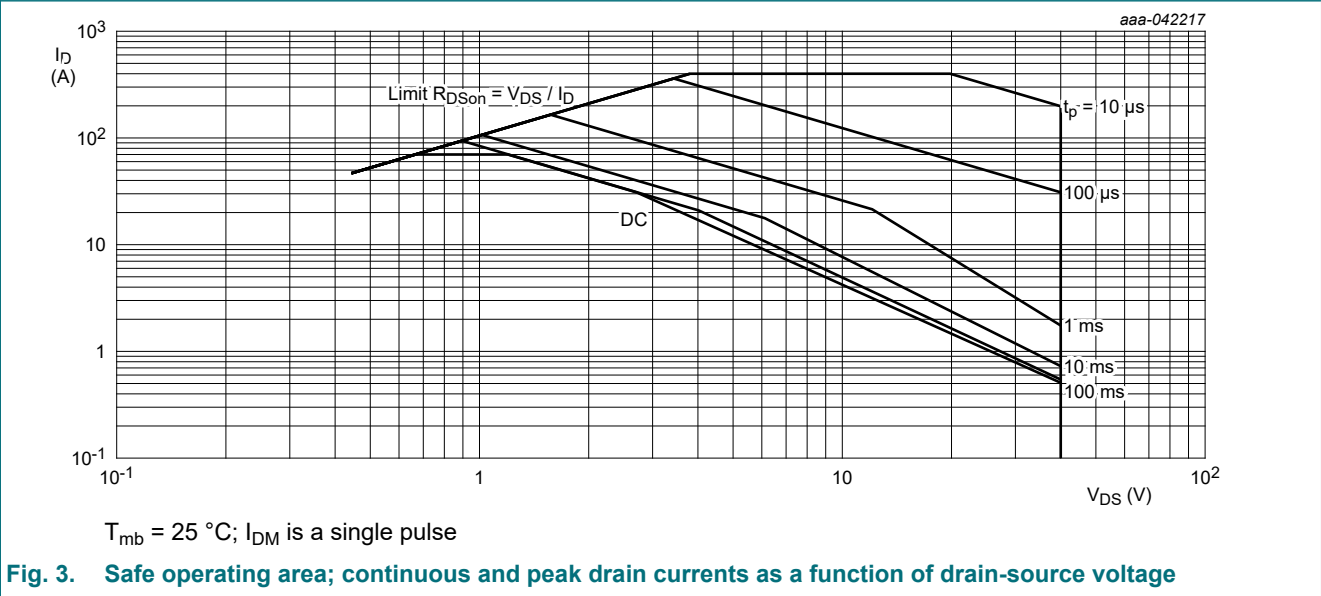
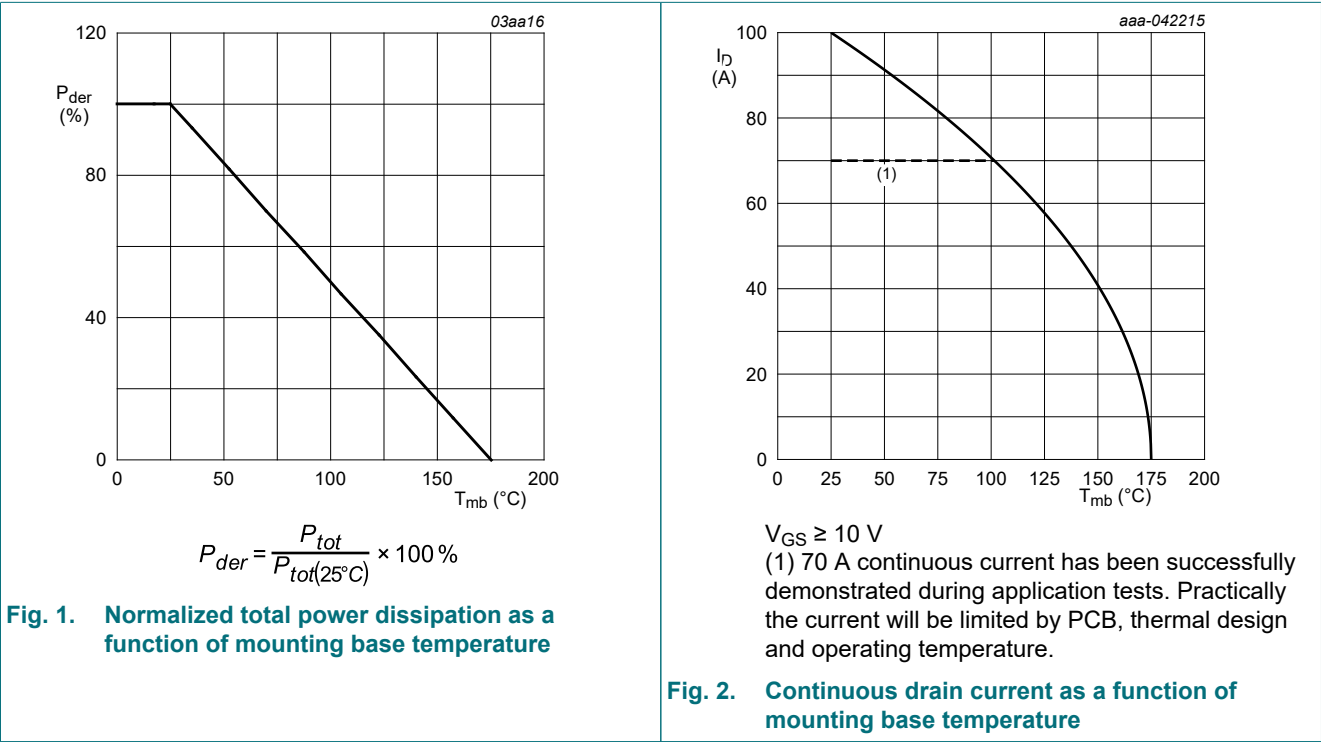
Table 5. Limiting values

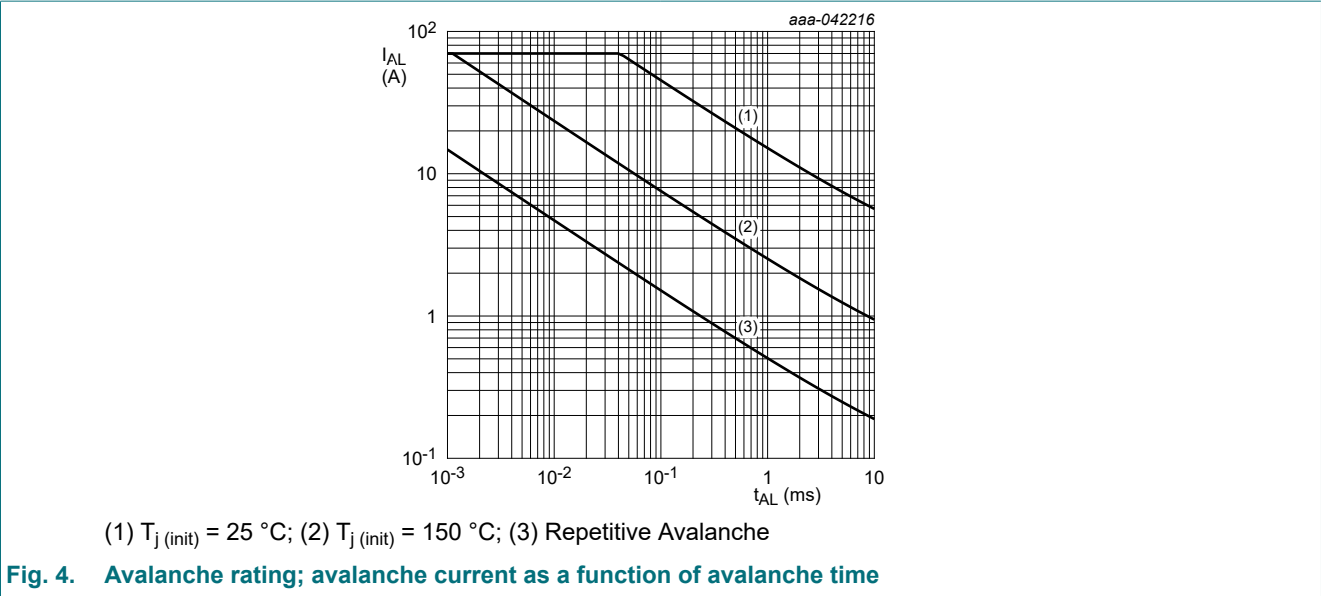
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	84	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	-	70	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2	-	70	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3	-	400	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
Source-drain diode					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	70	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	400	A

Symbol	Parameter	Conditions		Min	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 39.14\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; unclamped; $t_p = 135\ \mu\text{s}$ ; <a href="#">Fig. 4</a>	[1] [2]	-	138	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} = 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $R_{GS} = 50\ \Omega$ ; <a href="#">Fig. 4</a>	[3]	-	70	A

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.
- [3] Protected by 100% test.



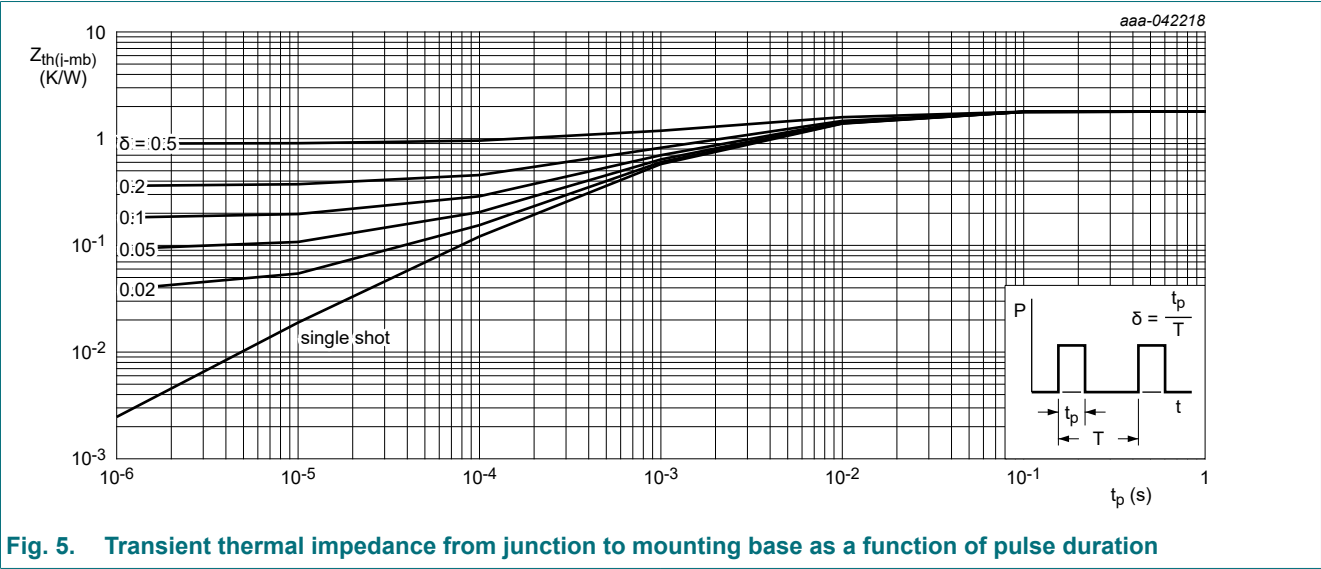


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	1.49	1.79	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	40	K/W

[1] Device on 4 layer PCB. Refer to TN00008 for further information.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C		40	44	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -40 °C		-	40.5	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C		36	40	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		2.4	3	3.6	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = 175 °C; <a href="#">Fig. 10</a>		1	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = -55 °C; <a href="#">Fig. 10</a>		-	-	4.3	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	0.01	1	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 175 °C		-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>		2.87	4.1	4.9	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 105 °C; <a href="#">Fig. 12</a>		4.25	5.51	7.25	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 125 °C; <a href="#">Fig. 12</a>		4.62	5.93	7.89	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 12</a>		5.48	7.08	9.36	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C		1	2.47	6.2	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	29	40	nC
Q <sub>GS</sub>	gate-source charge			-	8.8	13.2	nC
Q <sub>GD</sub>	gate-drain charge			-	4	8	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 15</a>		-	2096	3144	pF
C <sub>oss</sub>	output capacitance			-	474	663	pF
C <sub>rss</sub>	reverse transfer capacitance			-	106	233	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 20 V; R <sub>L</sub> = 0.8 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>J</sub> = 25 °C		-	7	-	ns
t <sub>r</sub>	rise time			-	8	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	23	-	ns
t <sub>f</sub>	fall time			-	9	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>		-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>		-	24	-	ns
Q <sub>r</sub>	recovered charge		[1]	-	16	-	nC

[1] includes capacitive recovery

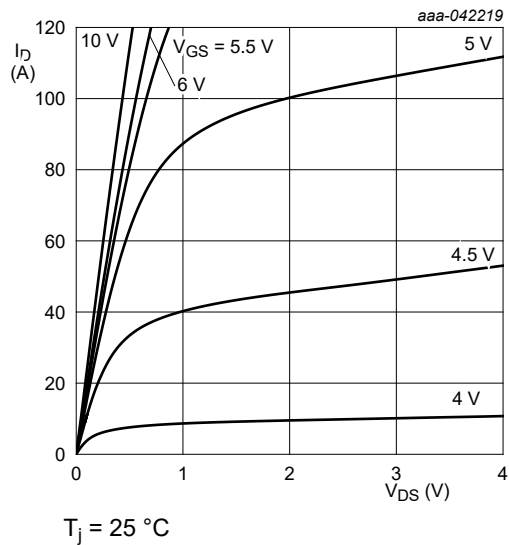


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

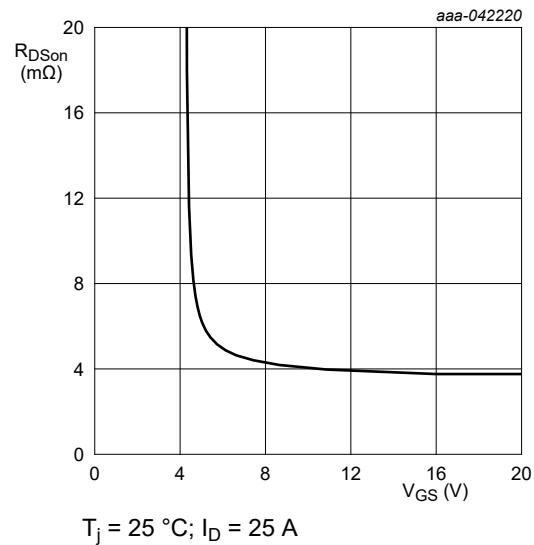


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

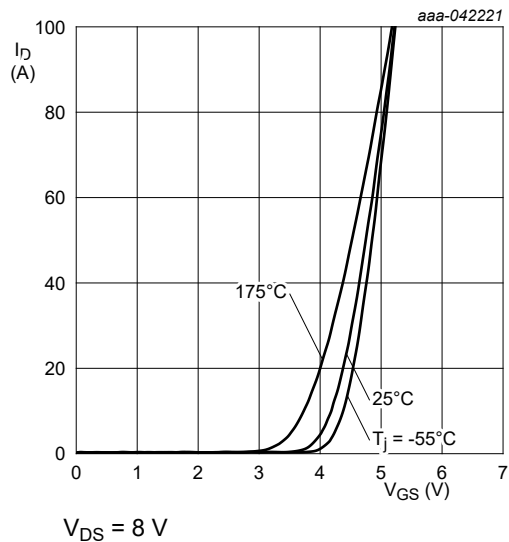


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

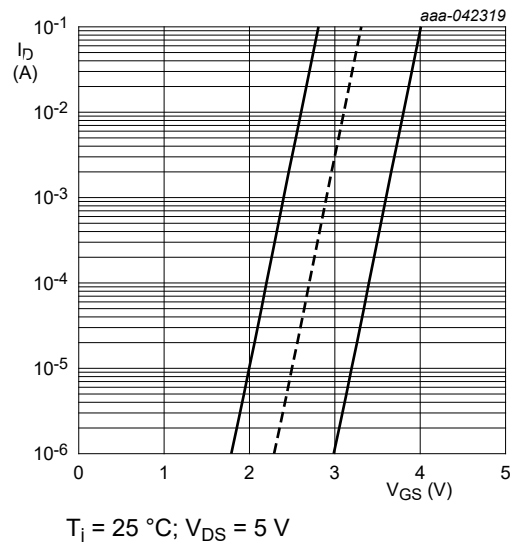


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

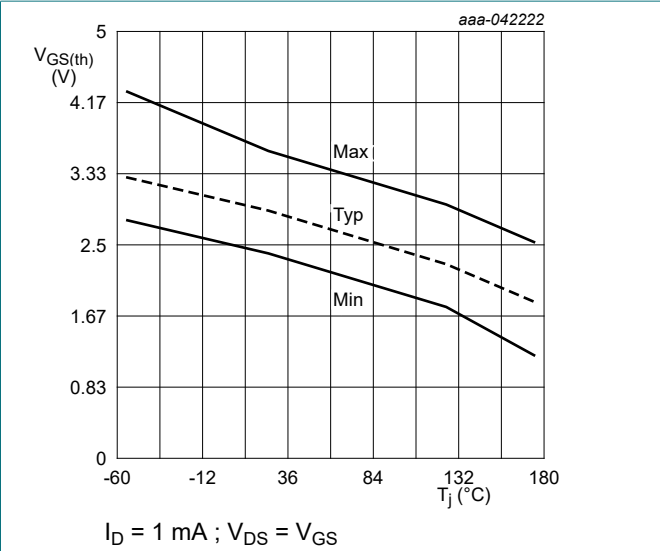


Fig. 10. Gate-source threshold voltage as a function of junction temperature

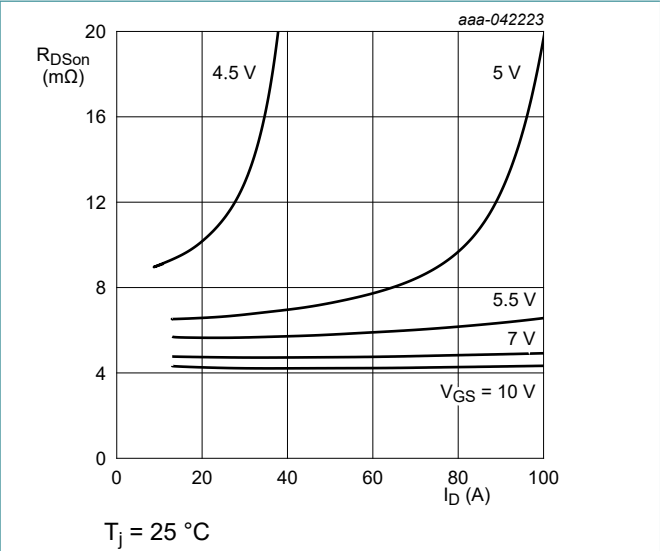


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

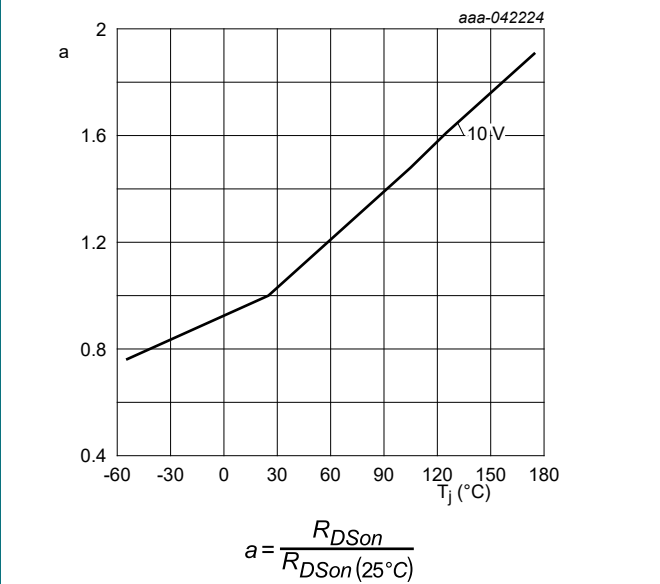


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

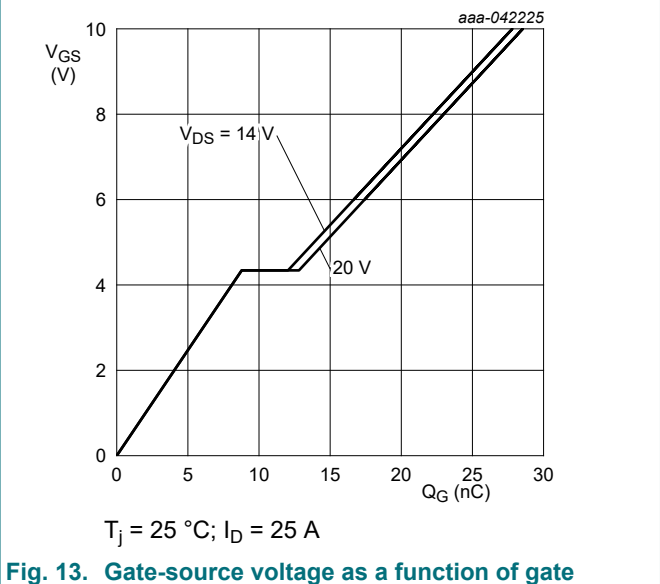


Fig. 13. Gate-source voltage as a function of gate charge; typical values

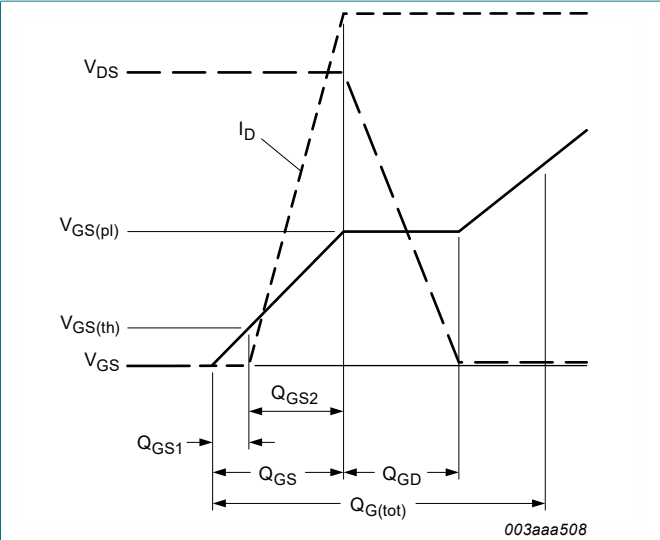


Fig. 14. Gate charge waveform definitions

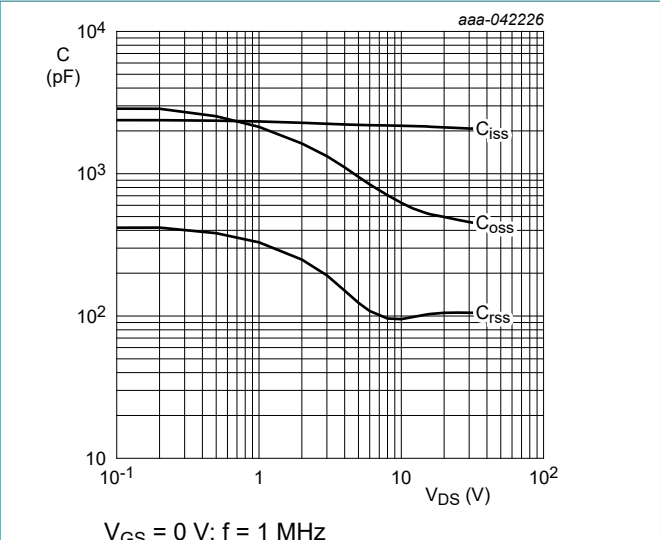


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

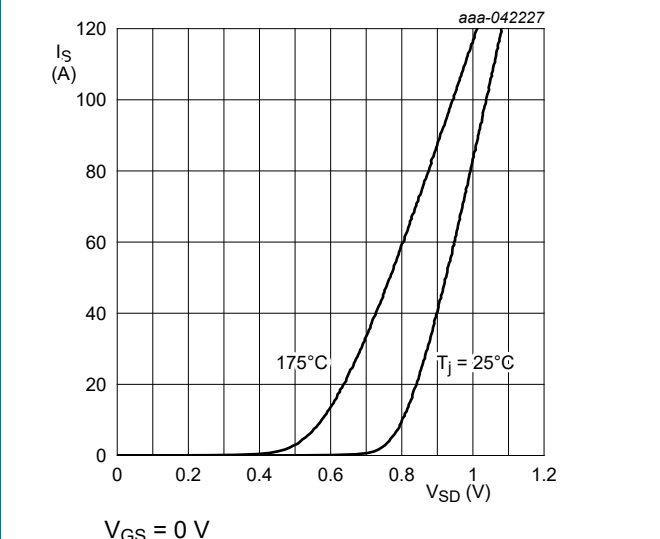


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

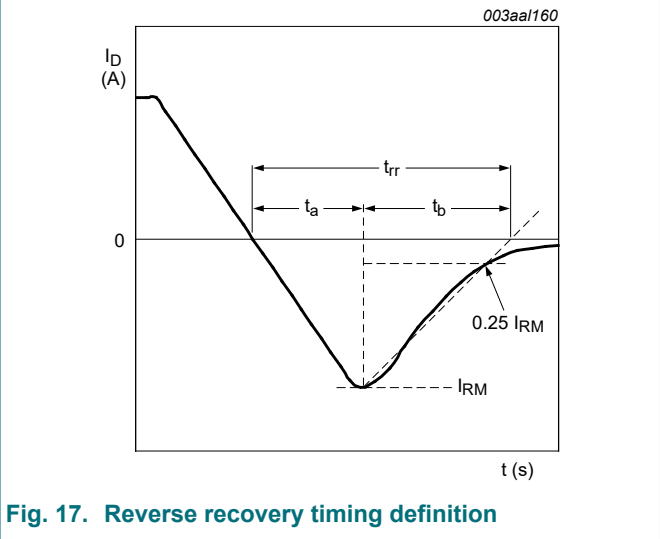


Fig. 17. Reverse recovery timing definition



11. Package outline

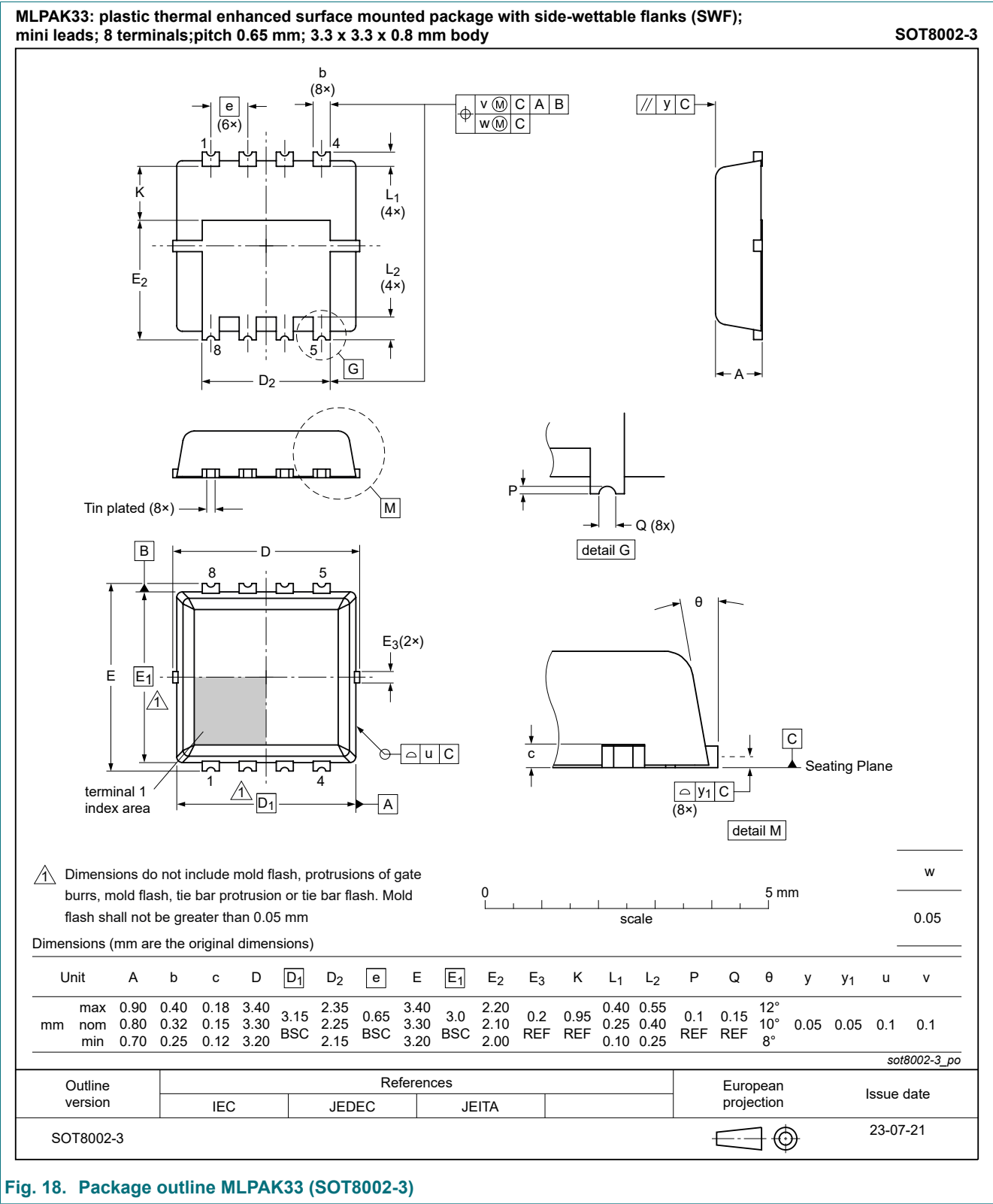


Fig. 18. Package outline MLPAK33 (SOT8002-3)

12. Soldering

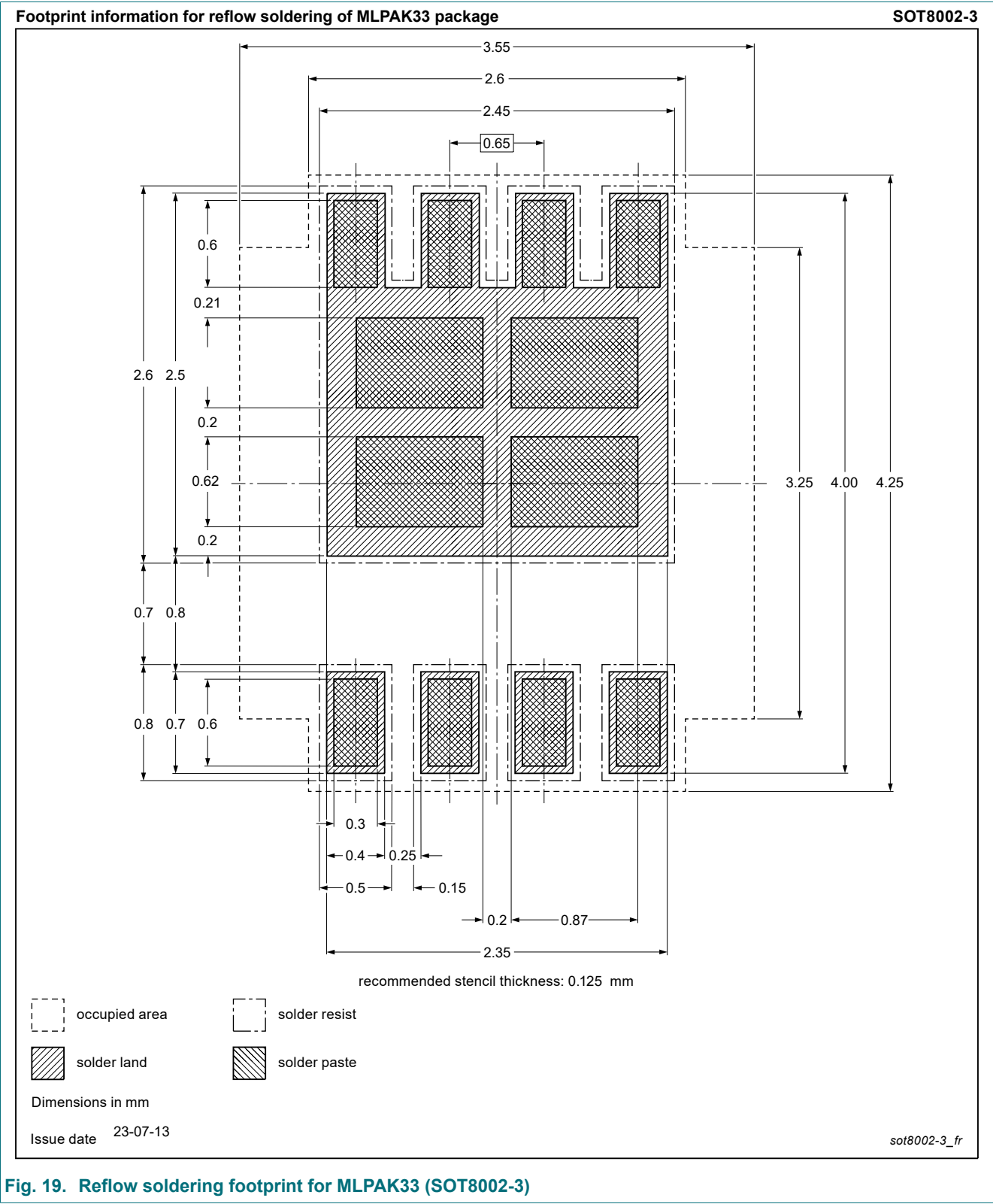


Fig. 19. Reflow soldering footprint for MLPAK33 (SOT8002-3)

### 13. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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