Low Duty LCD Segment Driver for Automotive application

BU91796MUF-M MAX 80 Segments (SEG20×COM4)

General Description

BU91796MUF-M is a 1/4 duty general-purpose LCD driver that can be used for automotive applications and can drive up to 80 LCD Segments.
It can support operating temperature of up to +105°C and qualified for AEC-Q100 Grade2, as required for automotive applications.
Wettable flank QFN package is suitable for small footprint applications and provides significant advantages in inspectability and solder joint reliability.

Features

- AEC-Q100 Qualified (Note)
- Integrated RAM for Display Data (DDRAM): 20 x 4 bit (Max 80 Segment)
- LCD Drive Output: 4 Common Output, Max 20 Segment Output
- Integrated Buffer AMP for LCD Driving
- Integrated Oscillator Circuit
- No External Components
- Low Power Consumption Design

(Note) Grade 2

Applications

- Instrument Clusters
- Climate Controls
- Car Audios / Radios
- Metering
- White Goods
- Healthcare Products
- Battery Operated Applications

etc.

Key Specifications

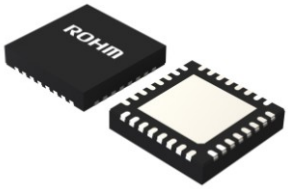
- Supply Voltage Range: +2.5V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 80Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 2wire Serial Interface

Special Characteristics

- ESD(HBM): ±2000V
- Latch-up current: ±100mA

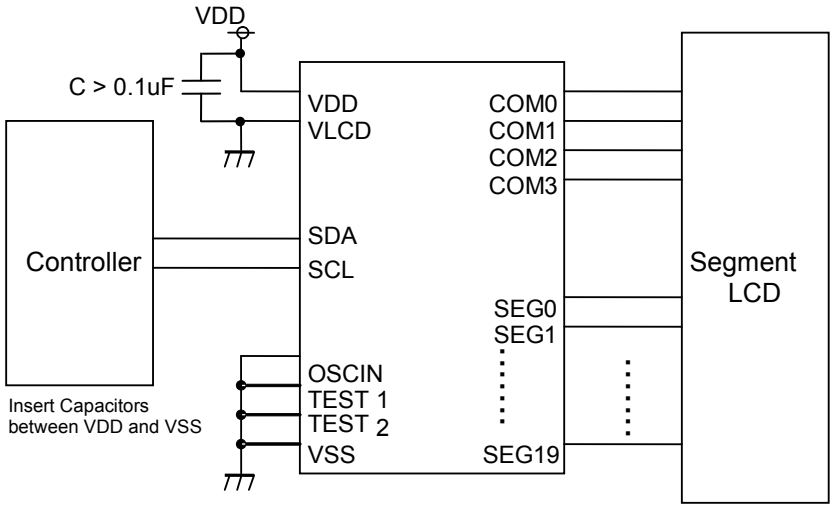
Package

W (Typ.) x D (Typ.) x H (Max.)



VQFN32FV5050
5.0mm x 5.0mm x 1.0mm

Typical Application Circuit



Internal Clock Mode

Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

Block Diagram / Pin Configuration / Pin Description

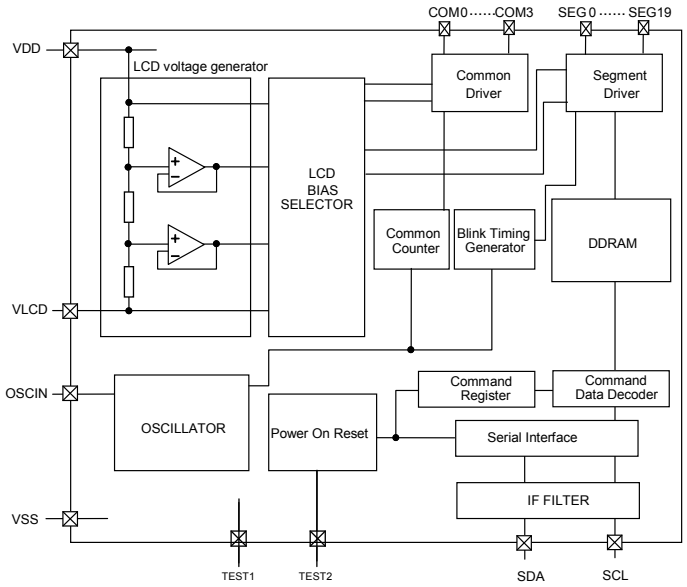


Figure 2. Block Diagram

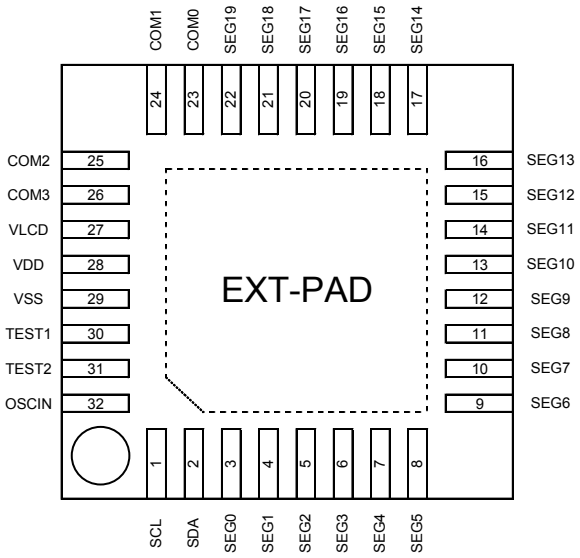


Figure 3. Pin Configuration (TOP VIEW)

Table 1. Pin Description

Pin Name	Pin No.	I/O	Function	Handling when unused
TEST1	30	I	Test input (ROHM use only) Must be connected to VSS	VSS
TEST2	31	I	POR enable setting VDD: POR disenable (Note1) VSS: POR enable	VSS
OSCIN	32	I	External clock input External clock and Internal clock can be selected by command Must be connected to VSS when using internal oscillator	VSS
SDA	2	I/O	Serial data in-out terminal	-
SCL	1	I	Serial clock terminal	-
VSS	29	-	GND	-
VDD	28	-	Power supply	-
VLCD	27	-	Power supply for LCD driving	-
SEG0-19	3-22	O	SEGMENT output for LCD driving	OPEN
COM0-3	23-26	O	COMMON output for LCD driving	OPEN
EXT-PAD	- (Note2)	-	Substrate	OPEN/VSS

(Note1) This function is guaranteed by design, not tested in production process. Software Reset is necessary to initialize IC in case of TEST2=VDD.
(Note2) To radiate heat, Contact a board with the EXT-PAD which is located at the bottom side of VQFN32FV5050 package.
Supply VSS level or Open state as the input condition for this PAD.

Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Maximum Voltage1	VDD	-0.5 to +7.0	V	Power Supply
Maximum Voltage2	VLCD	-0.5 to VDD	V	LCD Drive Voltage
Power Dissipation	Pd	0.70(Note1)	W	
Input Voltage Range	VIN	-0.5 to VDD+0.5	V	
Operational Temperature Range	Topr	-40 to +105	°C	
Storage Temperature Range	Tstg	-55 to +125	°C	

(Note1) Derate by 7.0mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +105°C, VSS=0V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Power Supply Voltage1	VDD	2.5	-	6.0	V	Power Supply
Power Supply Voltage2	VLCD	0	-	VDD-2.4	V	LCD Drive Voltage, VDD-VLCD ≥ 2.4V

Electrical Characteristics

DC Characteristics (VDD=2.5V to 6.0V, VLCD=0V, VSS=0V, Ta=-40°C to +105°C, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
"H" Level Input Voltage		VIH	0.7VDD	-	VDD	V	SDA,SCL,OSCIN
"L" Level Input Voltage		VIL	VSS	-	0.3VDD	V	SDA,SCL,OSCIN
"H" Level Input Current		IIH	-	-	1	μA	SDA,SCL,OSCIN(Note2), TEST2
"L" Level Input Current		IIL	-1	-	-	μA	SDA,SCL,OSCIN, TEST2
SDA "L" Level Output Voltage		VOL_SDA	0	-	0.4	V	Iload = 3mA
LCD Driver On Resistance	SEG	R_{ON}	-	3	-	kΩ	Iload=±10μA
	COM	R_{ON}	-	3	-	kΩ	
VLCD Supply Voltage		VLCD	0	-	VDD-2.4	V	VDD-VLCD≥2.4V
Standby Current		IDD1	-	-	5	μA	Display off, Oscillation off
Power Consumption		IDD2	-	12.5	30	μA	VDD=3.3V, VLCD=0V, Ta=25°C Power save mode1, FR=71Hz 1/3 bias, Frame inverse

(Note2) For external clock mode only.

Electrical Characteristics – continued

Oscillation Characteristics (VDD=2.5V to 6.0V, VLCD=0V, VSS=0V, Ta=-40°C to +105°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Frame Frequency1	fCLK1	56	80	112	Hz	FR = 80Hz setting, VDD=2.5V to 6.0V, Ta=-40°C to +105°C
Frame Frequency2	fCLK2	70	80	90	Hz	FR = 80Hz setting, VDD=3.3V, Ta=25°C
Frame Frequency3	fCLK3	77.5	87.5	97.5	Hz	FR = 80Hz setting, VDD=5.0V, Ta=25°C
Frame Frequency4	fCLK4	67.5	87.5	108	Hz	FR = 80Hz setting, VDD=5.0V, Ta=-40°C to +105°C
External Clock Rise Time	tr	-	-	0.3	μs	External clock mode (OSCIN) (Note)
External Clock Fall Time	tf	-	-	0.3	μs	
External Frequency	fEXCLK	15	-	300	KHz	
External Clock Duty	tdty	30	50	70	%	

(Note) <Frame frequency calculation at external clock mode>
DISCTL 80HZ setting: Frame frequency [Hz] = external clock [Hz] / 512
DISCTL 71HZ setting: Frame frequency [Hz] = external clock [Hz] / 576
DISCTL 64HZ setting: Frame frequency [Hz] = external clock [Hz] / 648
DISCTL 53HZ setting: Frame frequency [Hz] = external clock [Hz] / 768

【Reference Data】

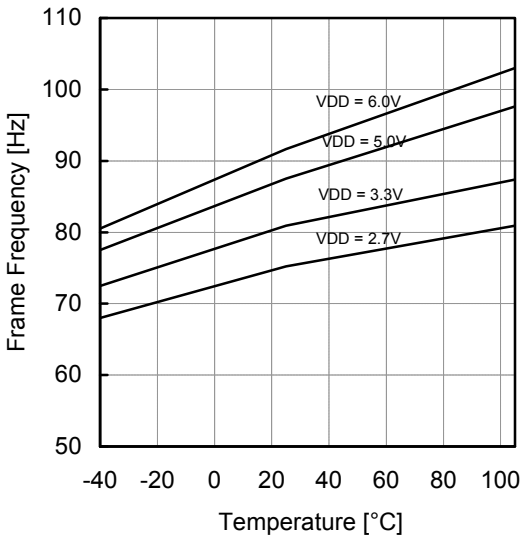


Figure 4. Typical Temperature Characteristics

Electrical Characteristics - continued

MPU interface Characteristics (VDD=2.5V to 6.0V, VLCD=0V, VSS=0V, Ta=-40°C to +105°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input Rise Time	tr	-	-	0.3	μs	
Input Fall Time	tf	-	-	0.3	μs	
SCL Cycle Time	tSCYC	2.5	-	-	μs	
“H” SCL Pulse Width	tSHW	0.6	-	-	μs	
“L” SCL Pulse Width	tSLW	1.3	-	-	μs	
SDA Setup Time	tSDS	100	-	-	ns	
SDA Hold Time	tSDH	100	-	-	ns	
Buss Free Time	tBUF	1.3	-	-	μs	
START Condition Hold Time	tHD;STA	0.6	-	-	μs	
START Condition Setup Time	tSU;STA	0.6	-	-	μs	
STOP Condition Setup Time	tSU;STO	0.6	-	-	μs	

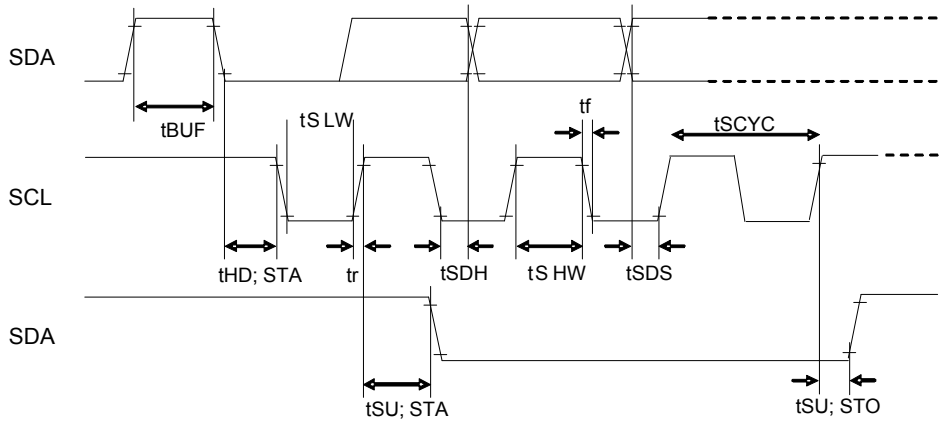


Figure 5. Interface Timing

I/O Equivalence Circuit

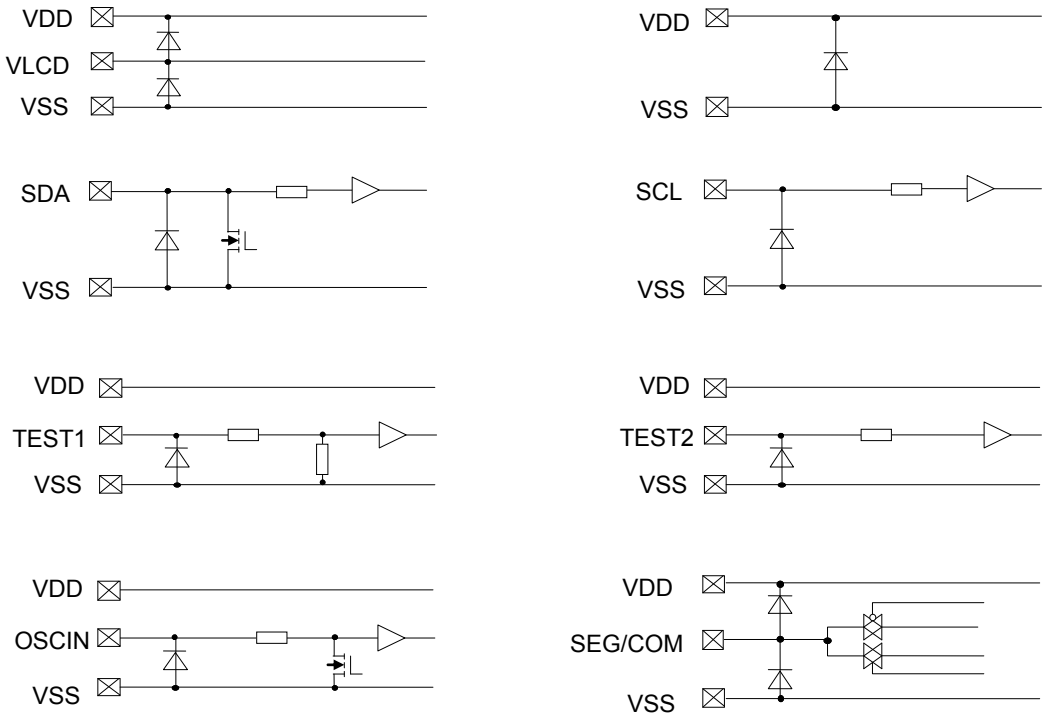
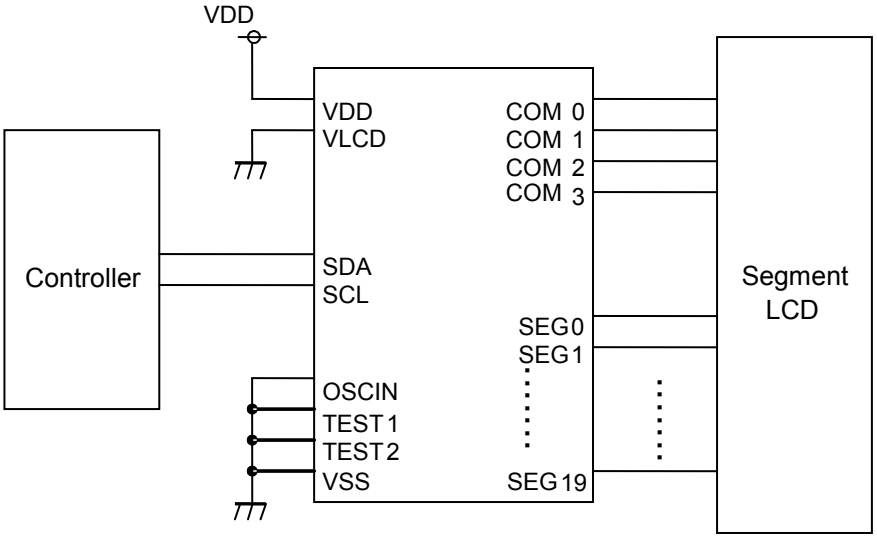
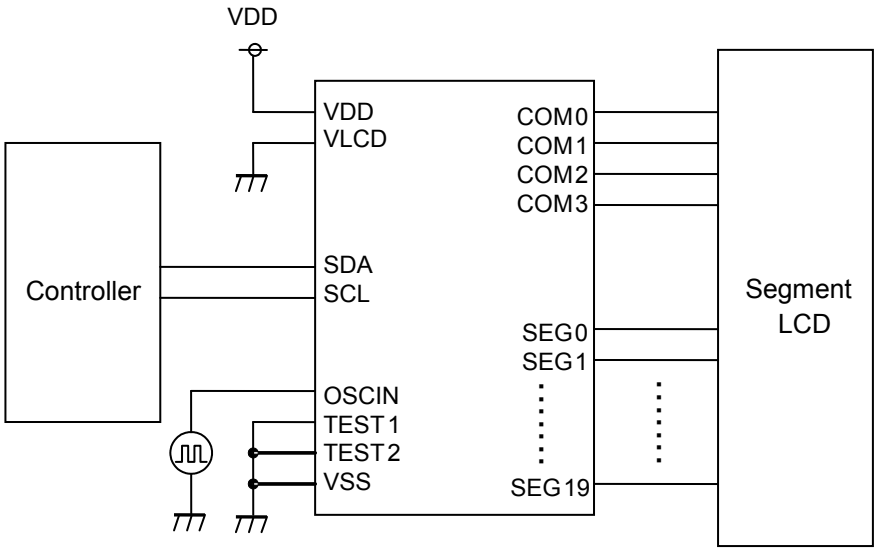


Figure 6 I/O Equivalence Circuit

Application Example



Internal Clock Mode



External Clock Mode

Figure 7. Example of Application Circuit

Functional Descriptions

Command /Data Transfer Method

BU91796MUF-M is controlled by 2wire signal (SDA, SCL).

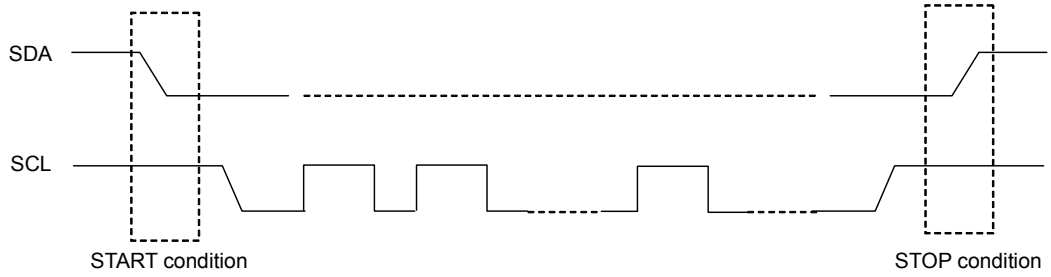


Figure 8. 2 wire Command/Data Transfer Format

It is necessary to generate START and STOP condition when sending command or display data through this 2 wire serial interface.

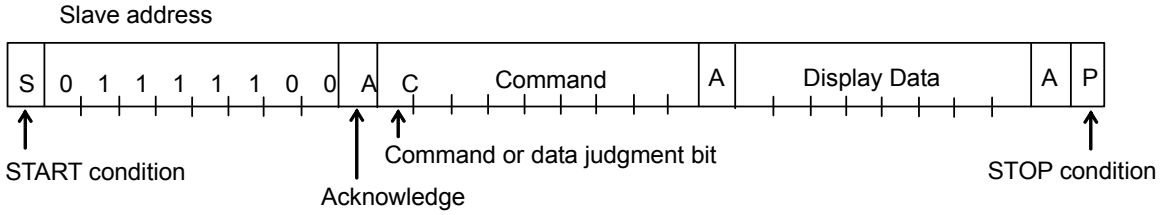


Figure 9. Interface Protcol

The following procedure shows how to transfer command and display data.

(1) Generate “START condition”.
(2) Issue Slave address.
(3) Transfer command and display data.
(4) Generate “STOP condition”

Acknowledge (ACK)

Data format is comprised of 8 bits, Acknowledge bit is returned after sending 8-bit data.
After the transfer of 8-bit data (Slave Address, Command, Display Data), release the SDA line at the falling edge of the 8th clock. The SDA line is then pulled “Low” until the falling edge of the 9th clock SCL.
(Output cannot be pulled “High” because of open drain NMOS).
If acknowledge function is not required, keep SDA line at “Low” level from 8th falling edge to 9th falling edge of SCL.

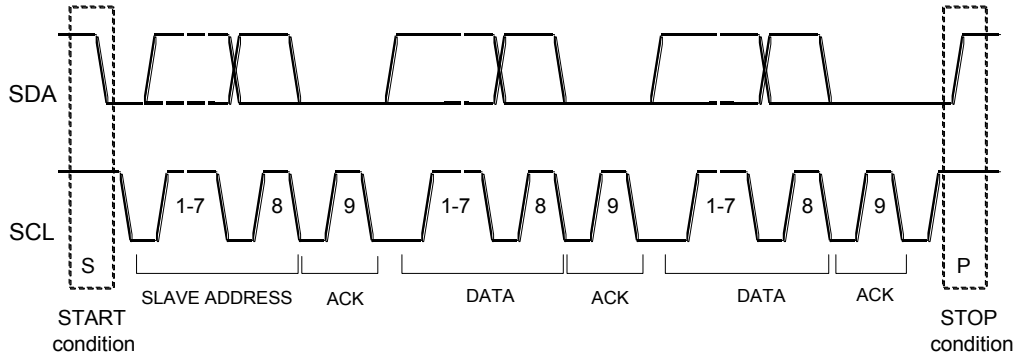
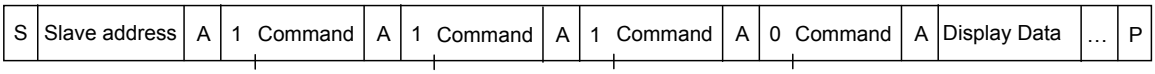


Figure 10. Acknowledge Timing

Command Transfer Method

Issue Slave Address (“01111100”) after generating “START condition”.
The 1st byte after Slave Address always becomes command input.
MSB (“command or data judge bit”) of command decide to next data is command or display data.
When set “command or data judge bit”=‘1’, next byte will be command.
When set “command or data judge bit”=‘0’, next byte data is display data.

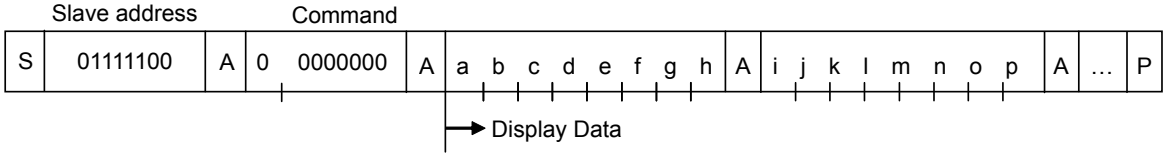


It cannot accept input command once it enters into display data transfer state.
In order to input command again it is necessary to generate “START condition”.
If “START condition” or “STOP condition” is sent in the middle of command transmission, command will be cancelled.
If Slave address is continuously sent following “START condition”, it remains in command input state.
“Slave address” must be sent right after the “START condition”.
When Slave Address cannot be recognized in the first data transmission, no Acknowledge bit is generated and next transmission will be invalid. When data is invalid status, if “START condition” is transmitted again, it will return to valid status.

Consider the MPU interface characteristic such as Input rise time and Setup/Hold time when transferring command and data (Refer to MPU Interface).

Write Display and Transfer Method

BU91796MUF-M has Display Data RAM (DDRAM) of 20×4=80bit.
The relationship between data input and display data, DDRAM data and address are as follows;



8-bit data is stored in DDRAM. ADSET command specifies the address to be written, and address is automatically incremented in every 4-bit data.
Data can be continuously written in DDRAM by transmitting data continuously.
When RAM data is written successively, after writing RAM data to 13h (SEG19), the address is returned to 00h (SEG0) by the auto-increment function

DDRAM address

BIT	00	01	02	03	04	05	06	07	・・・	11h	12h	13h	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG17	SEG18	SEG19	

Display data is written to DDRAM every 4-bit data.
No need to wait for ACK bit to complete data transfer.

Oscillator

The clock signals for logic and analog circuit can be generated from internal oscillator or external clock.
If internal oscillator circuit is used, OSCIN must be connected to VSS level.
When using external clock mode, input external clock from OSCIN terminal after ICSET command setting.

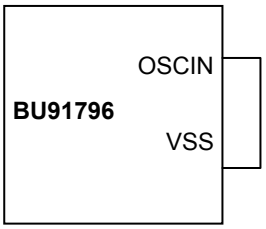


Figure 11. Internal Clock Mode

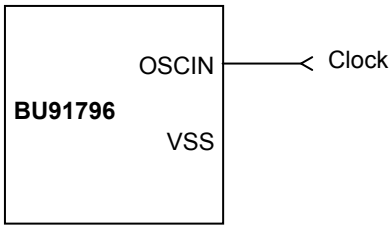


Figure 12. External Clock Mode

LCD Driver Bias Circuit

BU91796MUF-M generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
1/3 or 1/2 Bias can be set by MODESET command.
Line or frame inversion can be set by DISCTL command.
Refer to the “LCD driving waveform” for each LCD bias setting.

Blink Timing Generator

BU91796MUF-M has Blink function.
Blink mode is asserted by BLKCTL command.
The Blink frequency varies depending on fCLK characteristics at internal clock mode.
Refer to Oscillation Characteristics for fCLK.

Reset Initialize Condition

Initial condition after executing Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Command Description for initial value of registers.

Command / Function List

Description List of Command / Function

No.	Command	Function
1	Set IC Operation (ICSET)	Software reset, internal/external clock setting
2	Display Control (DISCTL)	Frame frequency, power save mode setting
3	Address Set (ADSET)	DDRAM address setting (00h to 13h)
4	Mode Set (MODESET)	Display on/off, 1/2bias or 1/3bias setting
5	Blink Control (BLKCTL)	Blink off/0.5s/1s/2s blink setting
6	All Pixel Control (APCTL)	All pixels on/off during DISPON

Detailed Command Description

D7 (MSB) is a command or data judgment bit.
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.
1: Next byte is command.

Set IC Operation (ICSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	0	1	*	P1	P0

(* : Don't care)

Set software reset execution.

Setup	P1
No operation	0
Software Reset Execute	1

When "Software Reset" is executed, BU91796MUF-M is reset to initial condition.
(Refer to Reset initialize condition)
Don't set Software Reset (P1) with P0 at the same time.

Set oscillator mode

Setup	P0	Reset initialize condition
Internal clock	0	○
External clock	1	

Internal clock mode: OSCIN must be connected to VSS level.
External clock mode: Input external clock from OSCIN terminal..

<Frame frequency Calculation at external clock mode>
DISCTL 80Hz setting: Frame frequency [Hz] = external clock [Hz] / 512
DISCTL 71Hz setting: Frame frequency [Hz] = external clock [Hz] / 576
DISCTL 64Hz setting: Frame frequency [Hz] = external clock [Hz] / 648
DISCTL 53Hz setting: Frame frequency [Hz] = external clock [Hz] / 768

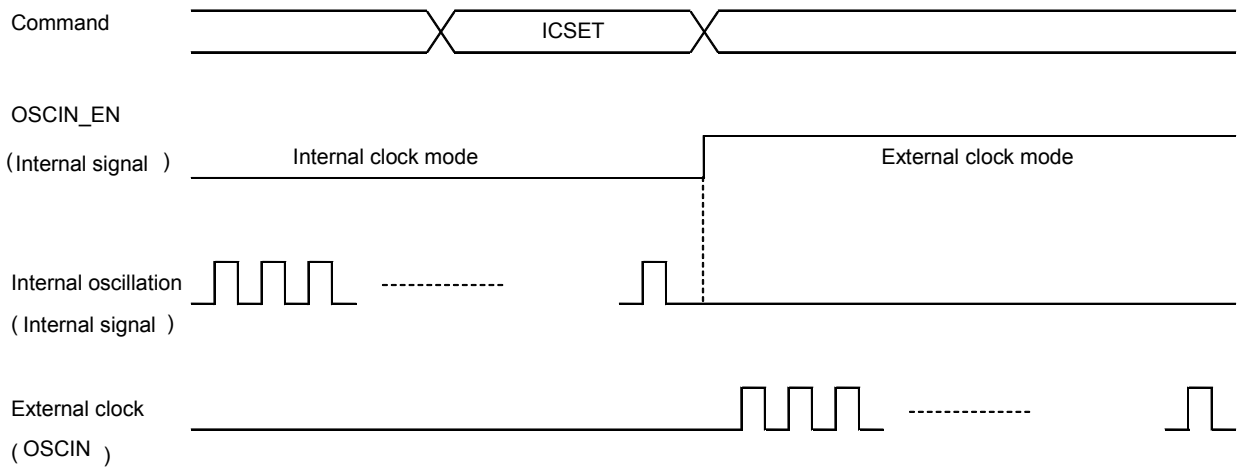


Figure 13. OSC MODE Switch Timing

Display Control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Power save mode FR.

Setup	P4	P3	Reset initialize condition
Normal mode (80Hz)	0	0	○
Power save mode 1 (71Hz)	0	1	
Power save mode 2 (64Hz)	1	0	
Power save mode 3 (50Hz)	1	1	

Power consumption is reduced in the following order:
Normal mode > Power save mode1 > Power save mode 2 > Power save mode 3.

Set LCD drive waveform.

Setup	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Power consumption is reduced in the following order:
Line inversion > Frame inversion
Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.
Regarding driving waveform, refer to LCD driving waveform.

Set Power save mode SR.

Setup	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

Power consumption is increased in the following order:
Power save mode 1 < Power save mode 2 < Normal mode < High power mode
Use VDD- VLCD ≥ 3.0V in High power mode condition.

(Reference current consumption data)

Setup	Current consumption
Power save mode 1	×0.5
Power save mode 2	×0.67
Normal mode	×1.0
High power mode	×1.8

The data above is for reference only. Actual consumption depends on Panel load.

Address Set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

The range of address can be set from 00000 to 10011(bin).
Don't set out of range address, otherwise address will be set 00000.

Mode Set (MODESET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	0	*	P3	P2	*	*

(* : Don't care)

Set display ON and OFF.

Setup	P3	Reset initialize condition
Display OFF (DISPOFF)	0	○
Display ON (DISPON)	1	

Display OFF : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1frame of data write. Display OFF mode will be disabled after Display ON command.
Display ON : SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

Set bias level

Setup	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

Refer to LCD driving waveform.

Blink Control (BLKCTL)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	1	0	*	P1	P0

(* : Don't care)

Set blink mode.

Blink mode (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

The Blink frequency varies depending on fCLK characteristics at internal clock mode.
Refer to Oscillation Characteristics for fCLK.

All Pixel Control (APCTL)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	1	1	1	1	1	P1	P0

All display set ON, OFF

Setup	P1	Reset initialize condition
Normal	0	○
All pixel ON (APON)	1	

Setup	P0	Reset initialize condition
Normal	0	○
All pixel OFF (APOFF)	1	

All pixels ON: All pixels are ON regardless of DDRAM data.
All pixels OFF: All pixels are OFF regardless of DDRAM data.

This command is valid in Display on status. The data of DDRAM is not changed by this command.
If set both P1 and P0 ="1", APOFF will be selected.

LCD Driving Waveform

(1/3bias)

Line Inversion

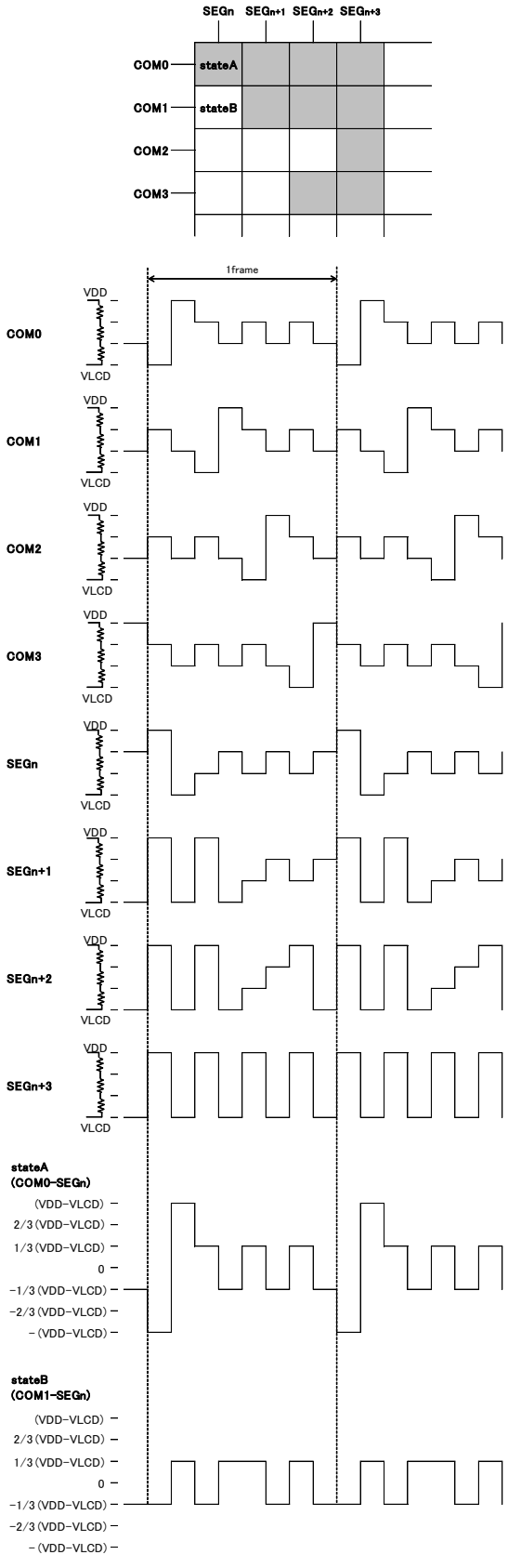


Figure 14. LCD Waveform at Line Inversion (1/3bias)

Frame Inversion

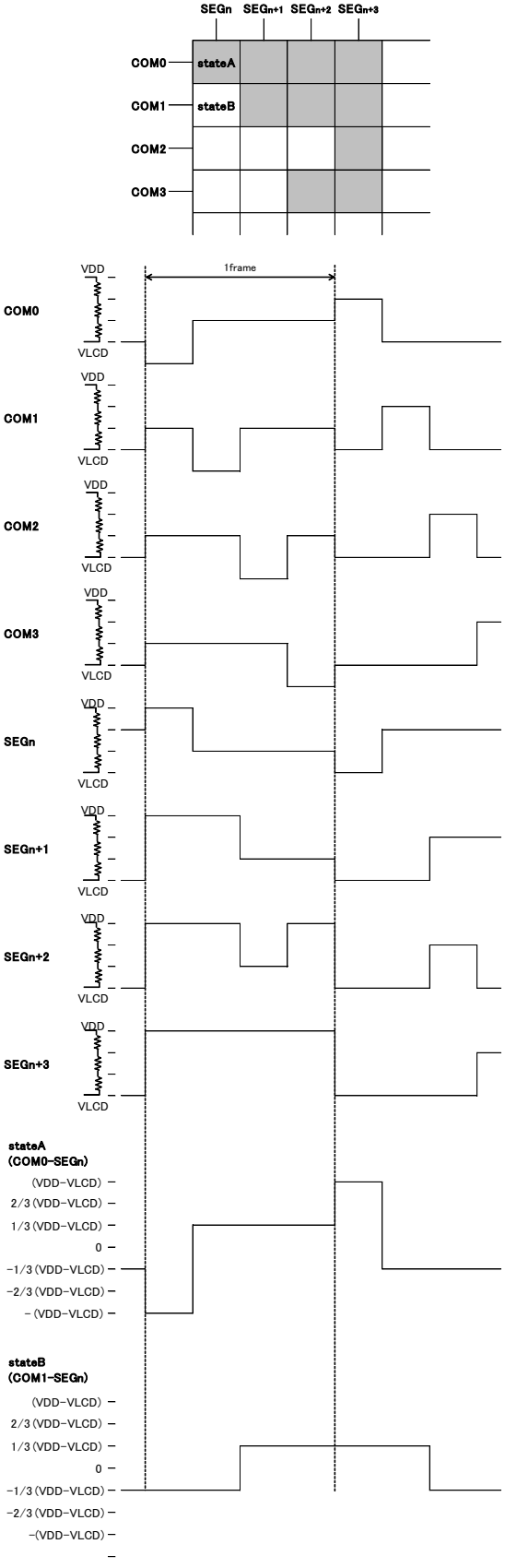


Figure 15. LCD Waveform at Frame Inversion (1/3bias)

(1/2bias)

Line Inversion

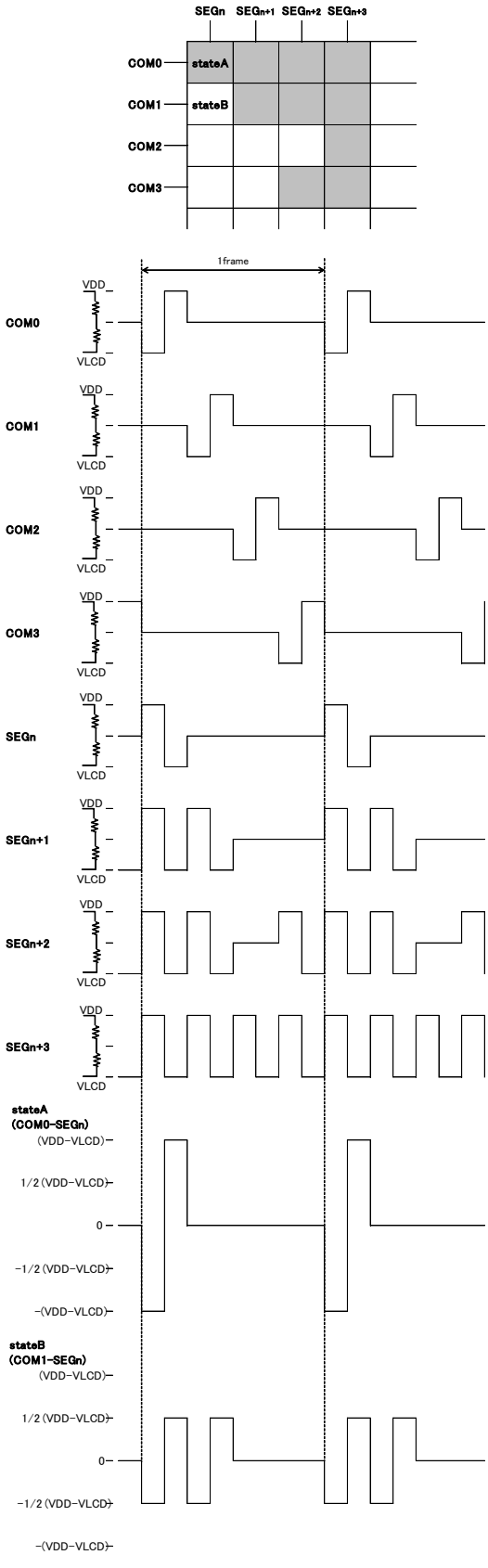


Figure 16. LCD Waveform in Line Inversion (1/2bias)

Frame Inversion

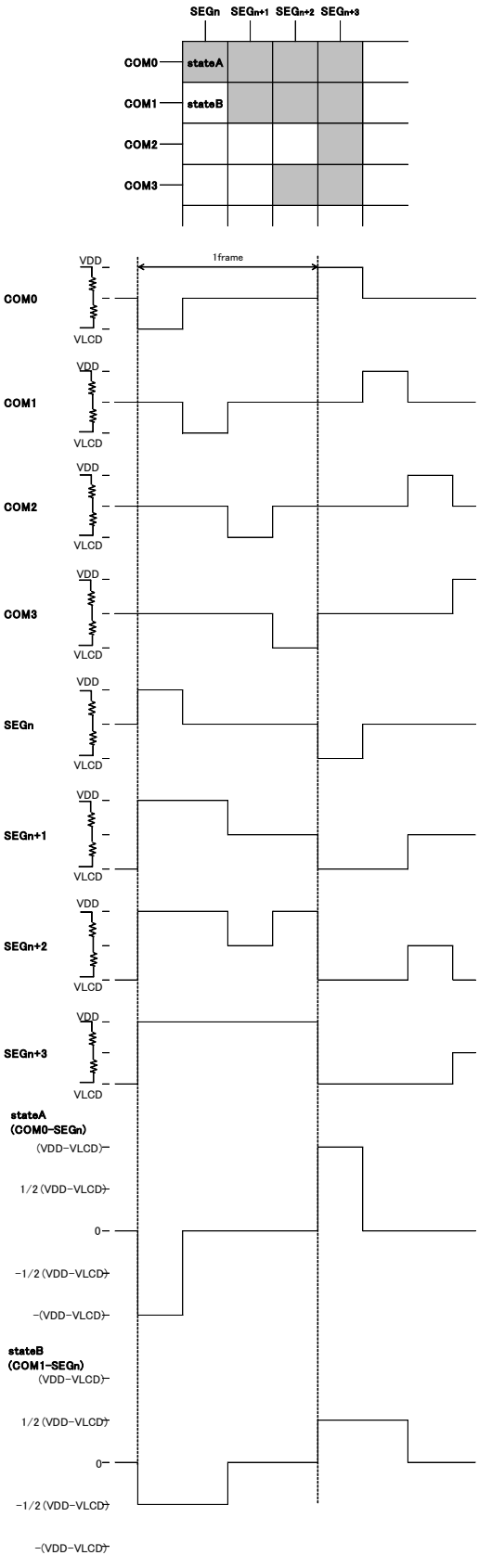


Figure 17. LCD Waveform in Frame Inversion (1/2bias)

Example of Display Data

If LCD layout pattern is like Figure 18 and Figure 19, and display pattern is like Figure 20, Display data will be shown as below.

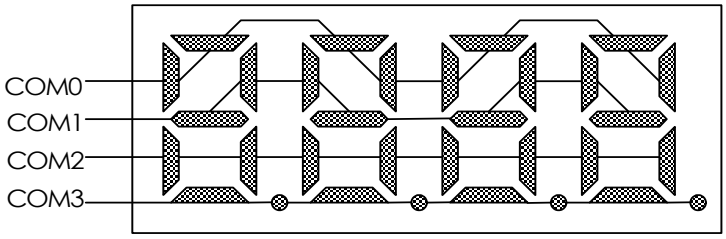


Figure 18. Example COM Line Pattern

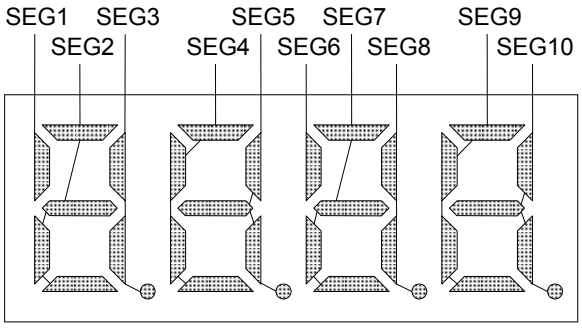


Figure 19. Example SEG Line Pattern

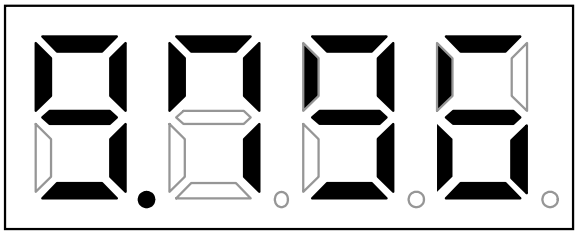


Figure 20. Example Display Pattern

<DDRAM data mapping in Figure 20 display pattern>

		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	D0	0	1	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
COM2	D2	0	0	0	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
COM3	D3	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Address		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

Initialize Sequence

Follow the Power-on sequence below to initialize condition.

Power on
↓
STOP condition
↓
START condition
↓
Issue slave address
↓
Execute Software Reset by sending ICSET command.

After Power-on and before sending initialize sequence, each register value, DDRAM address and DDRAM data are random.

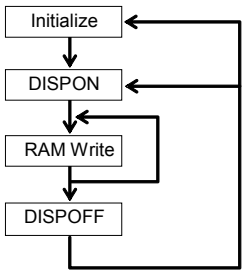
Start Sequence

Start Sequence Example1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0→5V (Tr: Min 1ms to Max 500ms)
	↓									
2	wait 100μs									Initialize IC
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
	↓									
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	0	1	*	1	0	Software Reset
	↓									
7	BLKCTL	1	1	1	1	0	*	0	0	Blink OFF
	↓									
8	DISCTL	1	0	1	0	0	1	0	0	80Hz, Frame inv., Power save mode1
	↓									
9	ICSET	1	1	1	0	1	*	0	1	External clock input
	↓									
10	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
11	Display Data	*	*	*	*	*	*	*	*	address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	address 02h to 03h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	address 12h to 13h
	↓									
12	Stop									Stop condition
	↓									
13	Start									Start condition
	↓									
14	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
15	MODESET	1	1	0	*	1	0	*	*	Display ON, 1/3bias
	↓									
16	Stop									Stop condition

(*: don't care)

Start Sequence Example2



Initialize Sequence

DISPON Sequence

RAM Write Sequence

DISPOFF Sequence

BU91796MUF-M is initialized with Start Sequence, starts to display with “DISPON Sequence”, updates display data with “RAM Write Sequence” and stops the display with “DISPOFF Sequence”.
Execute “DISPON Sequence” in order to restart display.

Initialize Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Power on									
wait 100us									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	
ICSET	1	1	1	0	1	0	1	0	Execute Software Reset
MODESET	1	1	0	0	0	0	0	0	Display OFF
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display data	*	*	*	*	*	*	*	*	Display data
…									
STOP									

DISPON Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	
ICSET	1	1	1	0	1	0	0	0	Execute internal OSC mode
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
MODESET	1	1	0	0	1	0	0	0	Display ON
STOP									

RAM Write Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	
ICSET	1	1	1	0	1	0	0	0	Execute internal OSC mode
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
MODESET	1	1	0	0	1	0	0	0	Display ON
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display Data	*	*	*	*	*	*	*	*	Display data
…									
STOP									

DISPOFF Sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	
ICSET	1	1	1	0	1	0	0	0	Execute internal OSC mode
MODESET	1	1	0	0	0	0	0	0	Display OFF
STOP									

Abnormal operation may occur in BU91796MUF-M due to the effect of noise or other external factor.
To avoid this phenomenon, it is highly recommended to input command according to sequence described above during initialization, display ON/OFF and refresh of RAM data.

Cautions in Power ON/OFF

BU91796MUF-M has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Keep the following recommended Power-On conditions in order to power up properly.

Set power up conditions to meet the recommended tR, tF, tOFF, and Vbot specification below in order to ensure P.O.R operation.
Set pin TEST2=”L” to enable POR circuit.

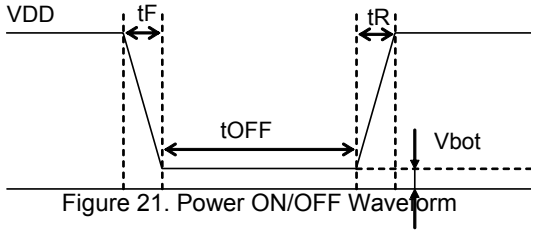


Figure 21. Power ON/OFF Waveform

Recommended condition of tR, tF, tOFF, Vbot (Ta=25°C)

tR(Note)	tF(Note)	tOFF(Note)	Vbot(Note)
1ms to 500ms	1ms to 500ms	Min 20ms	Less than 0.1V

(Note) This function is guaranteed by design, not tested in production process.

If it is difficult to keep above conditions, execute the following sequence as quickly as possible after Power-On.

Setting TEST2="H" disables the POR circuit, in such case, execute the following sequence.
Note however that it cannot accept command while supply is unstable or below the minimum supply range.
Note also that software reset is not a complete alternative to POR function.

1. Generate STOP Condition

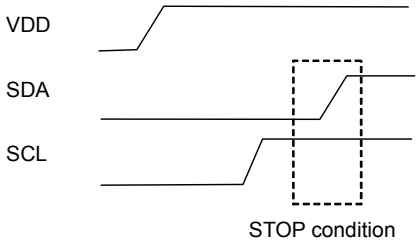


Figure 22. Stop Condition

2. Generate START Condition.

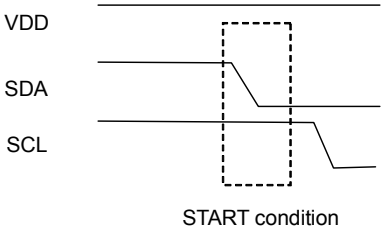


Figure 23. Start Condition

3. Issue Slave Address

4. Execute Software Reset (ICSET) Command

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Data transmission

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

Ordering Information

B U 9 1 7 9 6 M U F - M E 2

Part Number

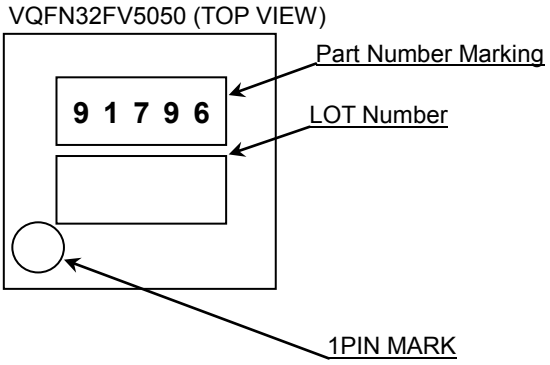
Package
MUF : VQFN32FV5050

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Lineup

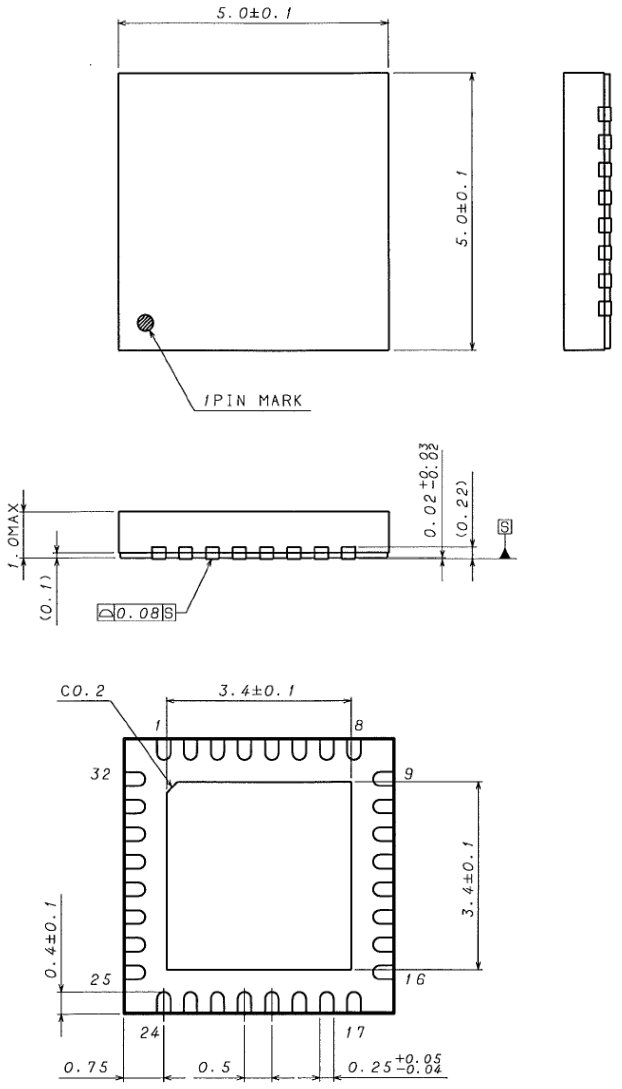
Package		Orderable Part Number
VQFN32FV5050	Reel of 2500	BU91796MUF-ME2

Marking Diagram



Physical Dimension Tape and Reel Information

Package Name	VQFN32FV5050



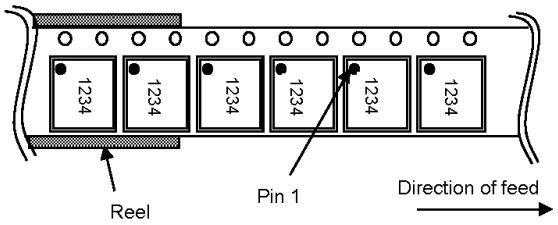
(UNIT:mm)

PKG:VQFN32FV5050
Drawing No.EX395-5001

NOTE:Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
8. Feb. 2016	001	First release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [f] Sealing or coating our Products with resin or other coating materials
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   [h] Use of the Products in places subject to dew condensation

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8. Confirm that operation temperature is within the specified range described in the product specification.

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

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BU91796MUF-M - Web Page

Part Number	BU91796MUF-M
Package	VQFN32FV5050
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes