

LCD Segment Drivers

Multi- function LCD Segment Drivers

BU91501KV-M

MAX 204 Segment(51SEGx4COM)

General Description

The BU91501KV-M is 1/4 or 1/3-Duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU91501KV-M can drive up to 204 LCD Segments directly and control up to 4 general-purpose output ports and up to 30 key input detection.

Features

- AEC-Q100 Qualified (Note)
- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- Either 1/4 or 1/3 duty can be selected
 - 1/4 duty drive : Up to 204 segments
 - 1/3 duty drive : Up to 156 segments
- Integrated RAM for display data (DDRAM)
- Segment/GPO (Max 4port) output mode selectable
- Support standby mode
- Integrated Power-on Reset circuit
- Integrated Oscillator circuit
- No external component
- Low power consumption design

(Note) Grade 2

Applications

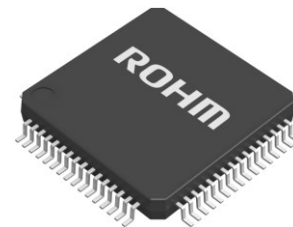
- Car Audio, Home Electrical Appliance, Meter Equipment etc.

Key Specifications

- Supply Voltage Range: 2.7V to 6.0V
- LCD drive power supply Range: 4.5V to 6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 204 Segments
- Display Duty: 1/3, 1/4 selectable
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

Package

W (Typ.) x D (Typ.) x H (Max.)



VQFP64
12.00mm x 12.00mm x 1.60mm

Typical Application Circuit

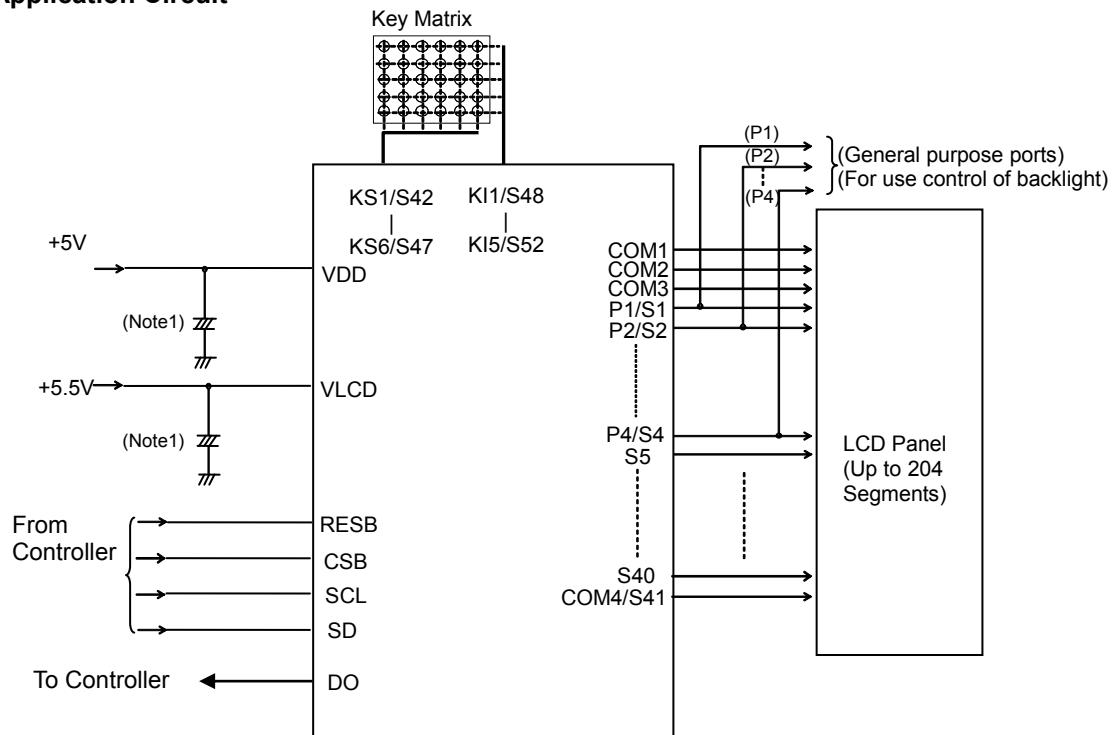


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Block Diagram / Pin Configuration / Pin Description

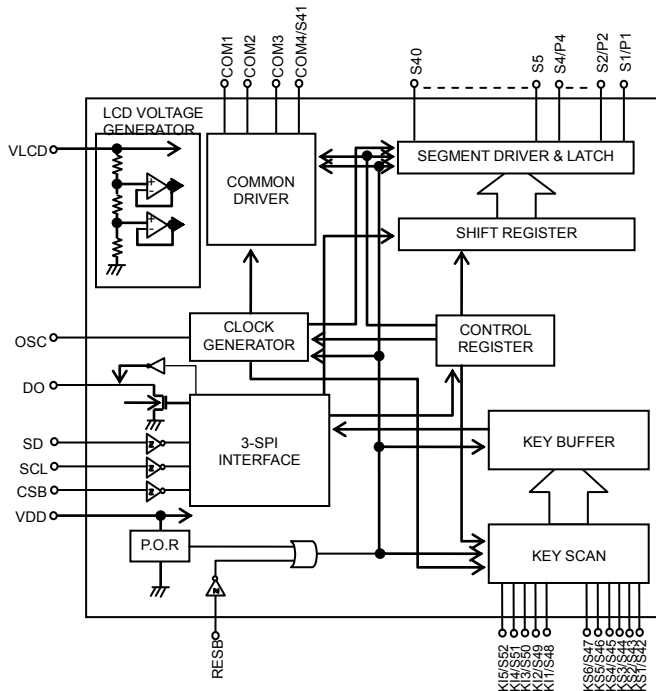


Figure 2. Block Diagram

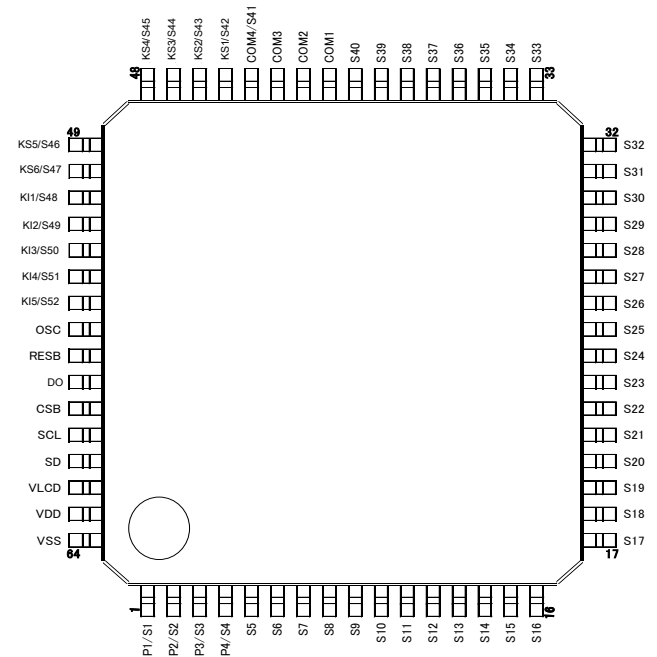


Figure 3. Pin Configuration (TOP VIEW)

| Terminal | Terminal No. | I/O | Handling When Unused | Functions |
|-----------------|--------------|-----|----------------------|--|
| CSB | 59 | I | VDD | Chip select : "L" active |
| SCL | 60 | I | VSS | Serial data transfer clock |
| SD | 61 | I | VSS | Input serial data |
| VDD | 63 | - | - | Power Supply for the logic |
| OSC | 56 | I/O | OPEN/VSS | External Clock Input: Fix to low or open when the internal clock mode setting. |
| DO | 58 | O | OPEN | Output data |
| RESB | 57 | I | VDD | Reset Input: RESB="L" : Display is disabled. RESB="H" : Display is controllable. However, serial data can not be transferred when RESB is "L". |
| VSS | 64 | - | - | Power supply pin. Must be connected to ground. |
| VLCD | 62 | - | - | Power Supply for the LCD driver |
| COM1~COM3 | 41 to 43 | O | OPEN | COMMON output for LCD driver |
| COM4/S41 | 44 | O | OPEN | COMMON / SEGMENT output for LCD driver. Assigned as SEGMENT output in 1/3Duty mode. |
| S1/P1~S4/P4 | 1 to 4 | O | OPEN | SEGMENT output for LCD driving / General Purpose Output S1/P1~S4/P4 pins can also be used as General Purpose Outputs when set up by the control data. |
| S5~S40 | 5 to 40 | O | OPEN | SEGMENT output for LCD driver |
| KS1/S42~KS6/S47 | 45 to 50 | O | OPEN | Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S42 to KS6/S47 pins can be used as segment outputs when specified by the control data. |
| KI1/S48~KI5/S52 | 51 to 55 | I/O | OPEN | Key scan inputs These pins have built-in pull-down resistors. The KI1/S48 to KI5/S52 pins can be used as segment outputs when specified by the control data. |

Table 1. Pin Description

Absolute Maximum Ratings (Ta=25°C, VSS=0.0V)

| Parameters | Symbol | Ratings | Unit | Remarks |
|-----------------------------|--------|-------------------------|------|-------------------|
| Power Supply voltage 1 | VDD | -0.5 to +7.0 | V | Power supply |
| Power Supply voltage 2 | VLCD | -0.5 to +7.0 | V | LCD drive voltage |
| Power Dissipation | Pd | 1.00 ^(Note2) | W | |
| Input voltage range | VIN | -0.5 to VDD+0.5 | V | |
| Operating temperature range | Topr | -40 to +105 | °C | |
| Storage temperature range | Tstg | -55 to +125 | °C | |

(Note2) When operated higher than Ta=25°C, subtract 10mW per degree. (Using ROHM standard board)

(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

| Parameters | Symbol | Ratings | | | Unit | Remarks |
|------------------------|--------|---------|-----|-----|------|--------------------|
| | | MIN | TYP | MAX | | |
| Power Supply voltage 1 | VDD | 2.7 | - | 6.0 | V | Power supply |
| Power Supply voltage 2 | VLCD | 4.5 | - | 6.0 | V | LCD driver voltage |

(Note3) The power supply condition shall be met VLCD ≥ VDD.

Electrical Characteristics

(Unless otherwise specified, Ta=-40°C to +105°C, VDD=2.7 to 6.0V, VLCD=4.5 to 6.0V, VSS=0.0V)

| Parameters | Symbol | Limits | | | Unit | Conditions |
|----------------------------|---------|-----------------|-----|-----------------|------|--|
| | | MIN | TYP | MAX | | |
| "H" Input Voltage | VIH | 0.7VDD | - | VDD | V | SD, SCL, CSB, RESB, OSC |
| "L" Input Voltage | VIL | VSS | - | 0.3VDD | V | SD, SCL, CSB, RESB, OSC |
| "H" Input Current | IIH | - | - | 5.0 | μA | SD, SCL, CSB, RESB, OSC, VI=5.5V |
| "L" Input Current | IIL | -5.0 | - | - | μA | SD, SCL, CSB, RESB, OSC, VI=0.0V |
| Input Floating Voltage | VIF | - | - | 0.05VDD | V | KI1 to KI5 |
| Pull-down Resistance | RPD | 50 | 100 | 250 | kΩ | KI1 to KI5, VLCD=5.0V |
| Output Off Leakage Current | IOFFH | - | - | 6.0 | μA | DO, Vo=5.5V |
| "H" Level Output Voltage | VOH1 | VLCD-1.0 | - | - | V | P1 to P4, Io=-1mA |
| | VOH2 | VLCD-1.0 | - | - | | S1 to S52, Io=-20μA |
| | VOH3 | VLCD-1.0 | - | - | | COM1 to COM4, Io=-100μA |
| | VOH4 | VLCD-1.0 | - | - | | KS1 to KS6, Io=-500μA |
| "L" Level Output Voltage | VOL1 | - | - | 1.0 | V | P1 to P4, Io=1mA |
| | VOL2 | - | - | 1.0 | | S1 to S52, Io=20μA |
| | VOL3 | - | - | 1.0 | | COM1 to COM4, Io=100μA |
| | VOL4 | - | - | 1.0 | | KS1 to KS6, Io=25μA |
| | VOL5 | - | - | 0.5 | | DO, Io=1mA |
| LCD Bias Voltage | VMID1 | 1/2VLCD -1.0 | - | 1/2VLCD +1.0 | V | S1 to S52 1/2 Bias, Io=±20μA |
| | VMID2 | 1/2VLCD -1.0 | - | 1/2VLCD +1.0 | | COM1 to COM4 1/2 Bias, Io=±100μA |
| | VMID3 | 2/3VLCD -1.0 | - | 2/3VLCD +1.0 | | S1 to S52 1/3 Bias, Io=±20μA |
| | VMID4 | 1/3VLCD -1.0 | - | 1/3VLCD +1.0 | | S1 to S52 1/3 Bias, Io=±20μA |
| | VMID5 | 2/3VLCD -1.0 | - | 2/3VLCD +1.0 | | COM1 to COM4 1/3 Bias, Io=±100μA |
| | VMID6 | 1/3VLCD -1.0 | - | 1/3VLCD +1.0 | | COM1 to COM4 1/3 Bias, Io=±100μA |
| Current Consumption | IstVDD | - | 1 | 5 | μA | Input Pin ALL "L" Display off, Disable oscillator |
| | IstVLCD | - | 1 | 5 | | Input Pin ALL "L" Display off, Disable oscillator |
| | IVDD1 | - | 2 | 10 | | VDD=VLCD=5.0V, Output unloaded fFR=80Hz |
| | IVLCD1 | - | 40 | 95 | | VDD=VLCD=5.0V, Output unloaded 1/2 Bias, fFR=80Hz |
| | IVLCD2 | - | 65 | 140 | | VDD=VLCD=5.0V, Output unloaded 1/3 Bias, fFR=80Hz |

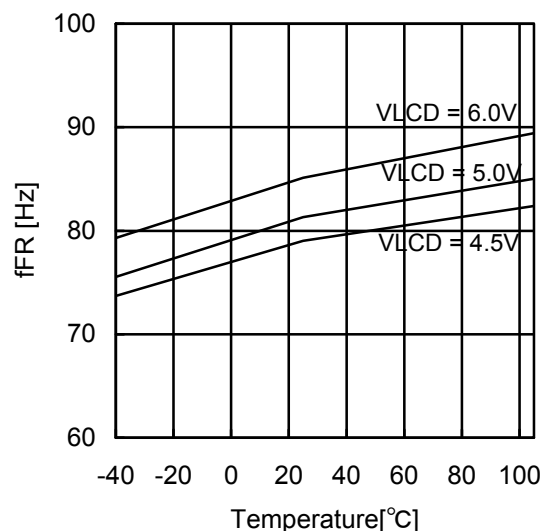
Electrical Characteristics – continued

Oscillation Characteristics (Ta=-40°C to +105°C, VDD=2.7 to 6.0V, VLCD=4.5V to 6.0V, VSS=0.0V)

| Parameters | Symbol | Limits | | | Unit | Conditions |
|--------------------------|--------|--------|-----|-----|------|--|
| | | MIN | TYP | MAX | | |
| Frame Frequency1 | fFR1 | 56 | 80 | 104 | Hz | VLCD=4.5V to 6.0V, fFR = 80Hz setting |
| Frame Frequency2 | fFR2 | 68 | 80 | 92 | Hz | VLCD=5.0V, fFR = 80Hz setting |
| External Clock Frequency | fFR3 | 30 | - | 600 | kHz | External clock mode (DRV CTRL1 setting : P2P1=11) |

Frame frequency is decided external frequency and dividing ratio of DRV CTRL1 setting.

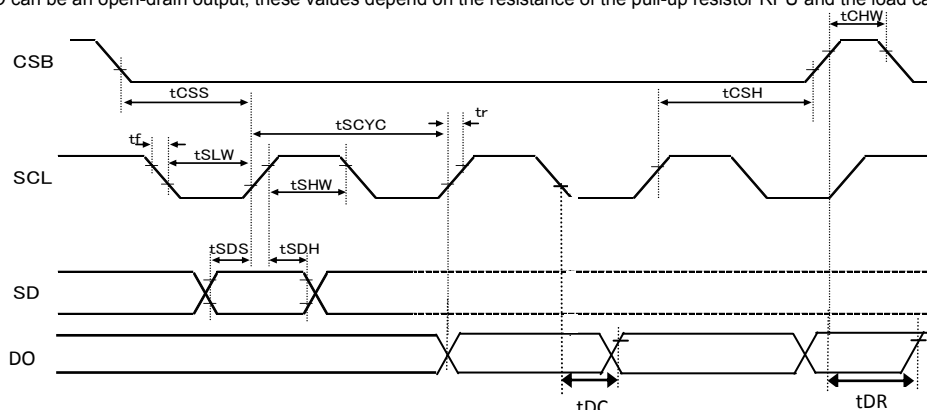
【Reference Data】

**Figure 4. Typical temperature characteristics**

MPU interface Characteristics (Ta=-40 to +105°C, VDD=2.7V to 6.0V, VLCD=4.5 to 6.0V, VSS=0.0V)

| Parameters | Symbol | Limits | | | Unit | Conditions |
|----------------------|--------|--------|-----|-----|------|-------------------------------|
| | | MIN | TYP | MAX | | |
| Input Rise Time | tr | - | - | 80 | ns | |
| Input Fall Time | tf | - | - | 80 | ns | |
| SCL Cycle Time | tSCYC | 400 | - | - | ns | |
| "H" SCL Pulse Width | tSHW | 100 | - | - | ns | |
| "L" SCL Pulse Width | tSLW | 100 | - | - | ns | |
| SD Setup Time | tSDS | 20 | - | - | ns | |
| SD Hold Time | tSDH | 20 | - | - | ns | |
| CSB Setup Time | tCSS | 50 | - | - | ns | |
| CSB Hold Time | tCSH | 50 | - | - | ns | |
| "H" CSB Pulse Width | tCHW | 50 | - | - | ns | |
| DO Output Delay Time | tDC | - | - | 1.5 | μs | DO RPU=4.7kΩ, CL=10pF (Note4) |
| DO Rise Time | tDR | - | - | 1.5 | μs | DO RPU=4.7kΩ, CL=10pF (Note4) |

(Note4) Since DO can be an open-drain output; these values depend on the resistance of the pull-up resistor RPU and the load capacitance CL.

**Figure 5. 3-wire Serial Interface Timing**

I/O equivalent circuit

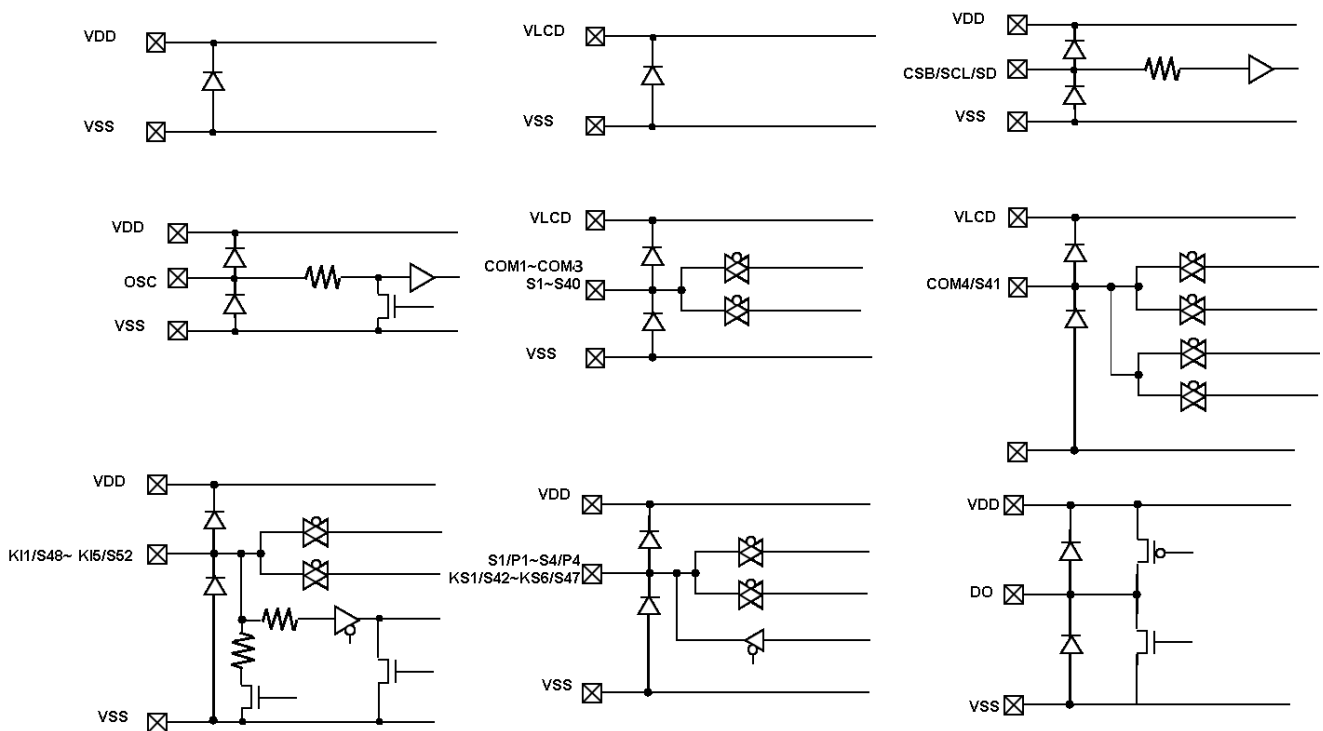


Figure 6. I/O equivalent circuit

Function descriptions

Command and Data Transfer Method

3-SPI (3-wire Serial Interface)

This device is controlled by a 3-wire signal (CSB, SCL, and SD).

First, Interface counter is initialized with CSB="H".

Setting CSB="L" enables SD and SCL inputs.

First, Interface counter is initialized with CSB="H", and then CSB="L" makes SD and SCL input enable.

The protocol of 3-SPI transfer is shown as follows.

Each command starts with D7 bit as MSB data, followed by D6 to D0 (this is while CSB = "L").

(Internal data is latched at the rising edge of SCL, then the data is converted to an 8-bit parallel data at the falling edge of the 8th CLK.)

When you rise CSB = "H", in case command less than 8bit, command and data are canceled.

(1) Write Mode

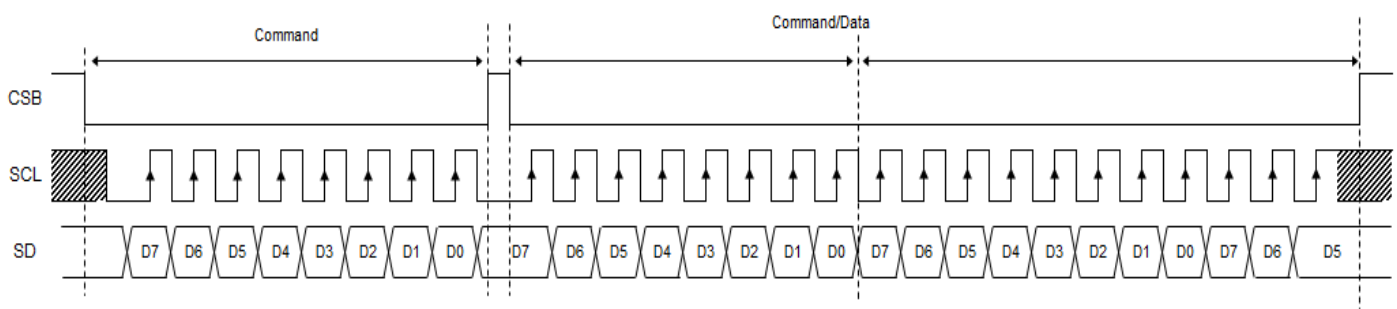


Figure 7. 3-SPI Data Transfer Format

(2) Read Mode (KEY RD command only)

The following occurs when Key Read by KEY RD command.

If KEY RD command is recognized at the rising edge of 8th CLK, it enters Read mode after the falling edge of 8th CLK and then key data is output through DO.

Setting CSB="H" can exit Read mode after or during Serial Data Transfer.

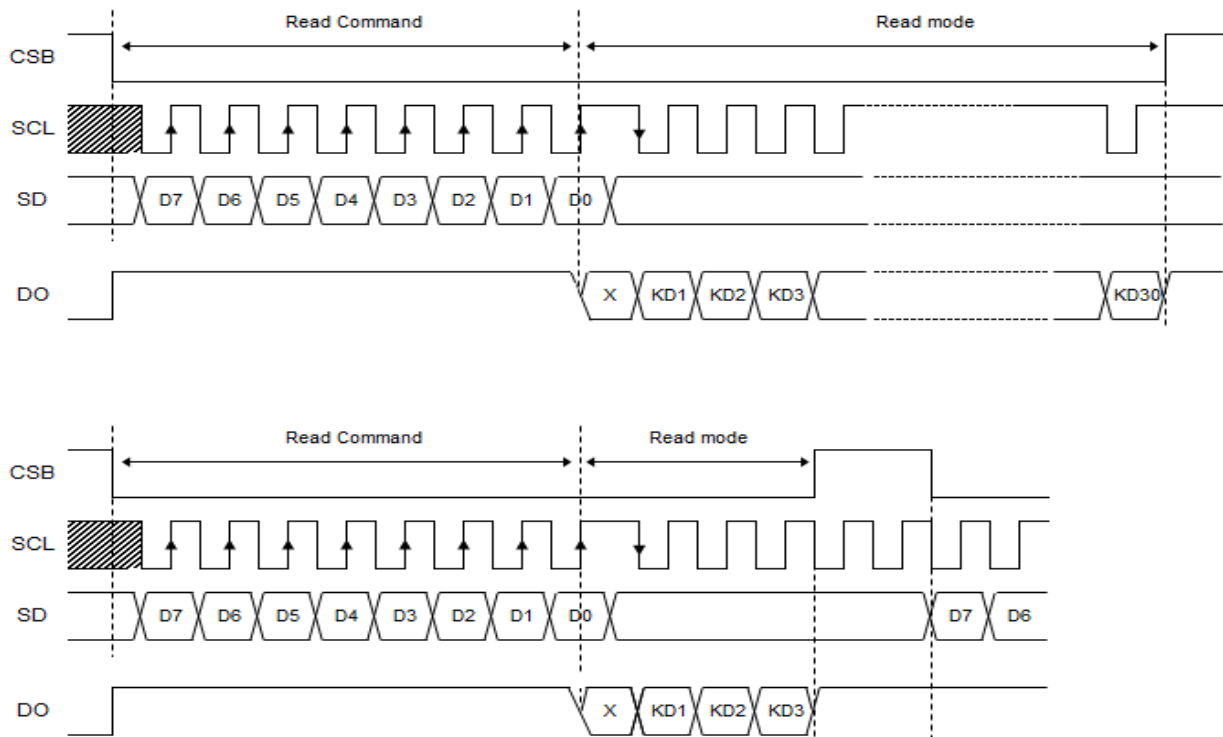


Figure 8. Serial Data Output Format

Command Transfer Method

After CSB="H"→"L", the 1st byte shall be a command.

Please refer to "Command Table".

When set command except Data write(DATAWR), the next byte will be (continuously) a command.

When set DATAWR command, the following bytes will be display data bytes.

| | | | | | |
|---------|---------|---------|---------|--------------|-----|
| Command | Command | Command | Command | Display Data | ... |
|---------|---------|---------|---------|--------------|-----|

(DATAWR)

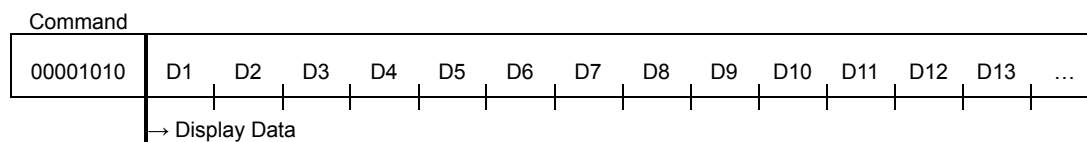
Once it becomes display data transfer mode, it will not be able to send command.

If you send command again, please rise CSB="H".

Display Data Transfer Method

This LSI has Display Data RAM (DDRAM) of 51×4=204bit.

The relationship between data input and display data, DDRAM data and address are as follows.



Display data will be stored in DDRAM. The address to be written is specified by Address set (ADSET) command and the address is automatically incremented in every 4bit data if 1/4 Duty mode or in every 3 bit if 1/3 Duty mode respectively.

1/3 Duty Mode

| DDRAM Address/Segment Outputs | | | | | | | | | | | | | |
|-------------------------------|-----|-----|-----|-----|-----|------|------|------|-----|------|------|------|------|
| | 00h | 01h | 02h | ... | 27h | 28h | 29h | ... | 31h | 32h | 33h | | |
| BIT | 0 | D1 | D4 | D7 | | D118 | D121 | D124 | | D148 | D151 | D154 | COM1 |
| | 1 | D2 | D5 | D8 | | D119 | D122 | D125 | | D149 | D152 | D155 | COM2 |
| | 2 | D3 | D6 | D9 | | D120 | D123 | D126 | | D150 | D153 | D156 | COM3 |
| | S1 | S2 | S3 | | S40 | S41 | S42 | | S50 | S51 | S52 | | |

Transferred data is written to the DDRAM by every 3bits. The write operation is cancelled if it changes CSB="L"→"H" before 3bits data transfer.

1/4 Duty Mode

Duty Mode

| DDRAM Address/ Segment Outputs | | | | | | | | | | | | | |
|--------------------------------|-----|-----|-----|-----|-----|------|------|------|-----|------|------|------|------|
| | 00h | 01h | 02h | ... | 27h | 28h | 29h | ... | 30h | 31h | 32h | | |
| BIT | 0 | D1 | D5 | D9 | | D157 | D161 | D165 | | D193 | D197 | D201 | COM1 |
| | 1 | D2 | D6 | D10 | | D158 | D162 | D166 | | D194 | D198 | D202 | COM2 |
| | 2 | D3 | D7 | D11 | | D159 | D163 | D167 | | D195 | D199 | D203 | COM3 |
| | 3 | D4 | D8 | D12 | | D160 | D164 | D168 | | D196 | D200 | D204 | COM4 |
| | S1 | S2 | S3 | | S40 | S42 | S43 | | S50 | S51 | S52 | | |

Transferred Data is written to the DDRAM by every 4bits. The write operation is cancelled if it changes CSB="L"→"H" before 4bits data transfer.

Relationship between Display Data and Segment Output Pins

1/3 Duty Mode

| output terminal | COM1 | COM2 | COM3 | Address | output terminal | COM1 | COM2 | COM3 | address |
|-----------------|------|------|------|---------|-----------------|------|------|------|---------|
| S1/P1 | D1 | D2 | D3 | 00 | S27 | D79 | D80 | D81 | 1A |
| S2/P2 | D4 | D5 | D6 | 01 | S28 | D82 | D83 | D84 | 1B |
| S3/P3 | D7 | D8 | D9 | 02 | S29 | D85 | D86 | D87 | 1C |
| S4/P4 | D10 | D11 | D12 | 03 | S30 | D88 | D89 | D90 | 1D |
| S5 | D13 | D14 | D15 | 04 | S31 | D91 | D92 | D93 | 1E |
| S6 | D16 | D17 | D18 | 05 | S32 | D94 | D95 | D96 | 1F |
| S7 | D19 | D20 | D21 | 06 | S33 | D97 | D98 | D99 | 20 |
| S8 | D22 | D23 | D24 | 07 | S34 | D100 | D101 | D102 | 21 |
| S9 | D25 | D26 | D27 | 08 | S35 | D103 | D104 | D105 | 22 |
| S10 | D28 | D29 | D30 | 09 | S36 | D106 | D107 | D108 | 23 |
| S11 | D31 | D32 | D33 | 0A | S37 | D109 | D110 | D111 | 24 |
| S12 | D34 | D35 | D36 | 0B | S38 | D112 | D113 | D114 | 25 |
| S13 | D37 | D38 | D39 | 0C | S39 | D115 | D116 | D117 | 26 |
| S14 | D40 | D41 | D42 | 0D | S40 | D118 | D119 | D120 | 27 |
| S15 | D43 | D44 | D45 | 0E | COM4/S41 | D121 | D122 | D123 | 28 |
| S16 | D46 | D47 | D48 | 0F | KS1/S42 | D124 | D125 | D126 | 29 |
| S17 | D49 | D50 | D51 | 10 | KS2/S43 | D127 | D128 | D129 | 2A |
| S18 | D52 | D53 | D54 | 11 | KS3/S44 | D130 | D131 | D132 | 2B |
| S19 | D55 | D56 | D57 | 12 | KS4/S45 | D133 | D134 | D135 | 2C |
| S20 | D58 | D59 | D60 | 13 | KS5/S46 | D136 | D137 | D138 | 2D |
| S21 | D61 | D62 | D63 | 14 | KS6/S47 | D139 | D140 | D141 | 2E |
| S22 | D64 | D65 | D66 | 15 | KI1/S48 | D142 | D143 | D144 | 2F |
| S23 | D67 | D68 | D69 | 16 | KI2/S49 | D145 | D146 | D147 | 30 |
| S24 | D70 | D71 | D72 | 17 | KI3/S50 | D148 | D149 | D150 | 31 |
| S25 | D73 | D74 | D75 | 18 | KI4/S51 | D151 | D152 | D153 | 32 |
| S26 | D76 | D77 | D78 | 19 | KI5/S52 | D154 | D155 | D156 | 33 |

(Note5) In case of S1/P1~S4/P4, COM4/S41, KS1/S42~KS6/S47 and KI1/S48~KI5/S52 are selected for segment output.

For example, S11 output case

| Bits in a DDRAM | | | Segment Output Pin (S11) |
|-----------------|-----|-----|--|
| D31 | D32 | D33 | |
| 0 | 0 | 0 | Off-state of the LCD elements corresponding to COM1, 2 and 3 |
| 0 | 0 | 1 | On-state of the LCD element corresponding to COM3 |
| 0 | 1 | 0 | On-state of the LCD element corresponding to COM2 |
| 0 | 1 | 1 | On-state of the LCD elements corresponding to COM2 and 3 |
| 1 | 0 | 0 | On-state of the LCD element corresponding to COM1 |
| 1 | 0 | 1 | On-state of the LCD elements corresponding to COM1 and 3 |
| 1 | 1 | 0 | On-state of the LCD elements corresponding to COM1 and 2 |
| 1 | 1 | 1 | On-state of the LCD elements corresponding to COM1, 2 and 3 |

1/4 duty

| output terminal | COM1 | COM2 | COM3 | COM4 | Address |
|-----------------|------|------|------|------|---------|
| S1/P1 | D1 | D2 | D3 | D4 | 00 |
| S2/P2 | D5 | D6 | D7 | D8 | 01 |
| S3/P3 | D9 | D10 | D11 | D12 | 02 |
| S4/P4 | D13 | D14 | D15 | D16 | 03 |
| S5 | D17 | D18 | D19 | D20 | 04 |
| S6 | D21 | D22 | D23 | D24 | 05 |
| S7 | D25 | D26 | D27 | D28 | 06 |
| S8 | D29 | D30 | D31 | D32 | 07 |
| S9 | D33 | D34 | D35 | D36 | 08 |
| S10 | D37 | D38 | D39 | D40 | 09 |
| S11 | D41 | D42 | D43 | D44 | 0A |
| S12 | D45 | D46 | D47 | D48 | 0B |
| S13 | D49 | D50 | D51 | D52 | 0C |
| S14 | D53 | D54 | D55 | D56 | 0D |
| S15 | D57 | D58 | D59 | D60 | 0E |
| S16 | D61 | D62 | D63 | D64 | 0F |
| S17 | D65 | D66 | D67 | D68 | 10 |
| S18 | D69 | D70 | D71 | D72 | 11 |
| S19 | D73 | D74 | D75 | D76 | 12 |
| S20 | D77 | D78 | D79 | D80 | 13 |
| S21 | D81 | D82 | D83 | D84 | 14 |
| S22 | D85 | D86 | D87 | D88 | 15 |
| S23 | D89 | D90 | D91 | D92 | 16 |
| S24 | D93 | D94 | D95 | D96 | 17 |
| S25 | D97 | D98 | D99 | D100 | 18 |
| S26 | D101 | D102 | D103 | D104 | 19 |

| output terminal | COM1 | COM2 | COM3 | COM4 | address |
|-----------------|------|------|------|------|---------|
| S27 | D105 | D106 | D107 | D108 | 1A |
| S28 | D109 | D110 | D111 | D112 | 1B |
| S29 | D113 | D114 | D115 | D116 | 1C |
| S30 | D117 | D118 | D119 | D120 | 1D |
| S31 | D121 | D122 | D123 | D124 | 1E |
| S32 | D125 | D126 | D127 | D128 | 1F |
| S33 | D129 | D130 | D131 | D132 | 20 |
| S34 | D133 | D134 | D135 | D136 | 21 |
| S35 | D137 | D138 | D139 | D140 | 22 |
| S36 | D141 | D142 | D143 | D144 | 23 |
| S37 | D145 | D146 | D147 | D148 | 24 |
| S38 | D149 | D150 | D151 | D152 | 25 |
| S39 | D153 | D154 | D155 | D156 | 26 |
| S40 | D157 | D158 | D159 | D160 | 27 |
| KS1/S42 | D161 | D162 | D163 | D164 | 28 |
| KS2/S43 | D165 | D166 | D167 | D168 | 29 |
| KS3/S44 | D169 | D170 | D171 | D172 | 2A |
| KS4/S45 | D173 | D174 | D175 | D176 | 2B |
| KS5/S46 | D177 | D178 | D179 | D180 | 2C |
| KS6/S47 | D181 | D182 | D183 | D184 | 2D |
| KI1/S48 | D185 | D186 | D187 | D188 | 2E |
| KI2/S49 | D189 | D190 | D191 | D192 | 2F |
| KI3/S50 | D193 | D194 | D195 | D196 | 30 |
| KI4/S51 | D197 | D198 | D199 | D200 | 31 |
| KI5/S52 | D201 | D202 | D203 | D204 | 32 |

(Note6) In case of S1/P1~S4/P4, KS1/S42~KS6/S47 and KI1/S48~KI5/S52 are selected for segment output.

For example, S11 output case

| Bits in the DDRAM | | | | Segment Output Pin (S11) |
|-------------------|-----|-----|-----|--|
| D41 | D42 | D43 | D44 | |
| 0 | 0 | 0 | 0 | Off-state of the LCD elements corresponding to COM1,2,3 and4 |
| 0 | 0 | 0 | 1 | On-state of the LCD element corresponding to COM4 |
| 0 | 0 | 1 | 0 | On-state of the LCD element corresponding to COM3 |
| 0 | 0 | 1 | 1 | On-state of the LCD elements corresponding to COM3 and 4 |
| 0 | 1 | 0 | 0 | On-state of the LCD element corresponding to COM2 |
| 0 | 1 | 0 | 1 | On-state of the LCD elements corresponding to COM2 and 4 |
| 0 | 1 | 1 | 0 | On-state of the LCD elements corresponding to COM2 and 3 |
| 0 | 1 | 1 | 1 | On-state of the LCD elements corresponding to COM2,3 and 4 |
| 1 | 0 | 0 | 0 | On-state of the LCD element corresponding to COM1 |
| 1 | 0 | 0 | 1 | On-state of the LCD elements corresponding to COM1 and 4 |
| 1 | 0 | 1 | 0 | On-state of the LCD elements corresponding to COM1 and 3 |
| 1 | 0 | 1 | 1 | On-state of the LCD elements corresponding to COM1, 3 and 4 |
| 1 | 1 | 0 | 0 | On-state of the LCD elements corresponding to COM1 and 2 |
| 1 | 1 | 0 | 1 | On-state of the LCD elements corresponding to COM1,2 and 4 |
| 1 | 1 | 1 | 0 | On-state of the LCD elements corresponding to COM1,2 and 3 |
| 1 | 1 | 1 | 1 | On-state of the LCD elements corresponding to COM1,2,3 and 4 |

Serial Data Output

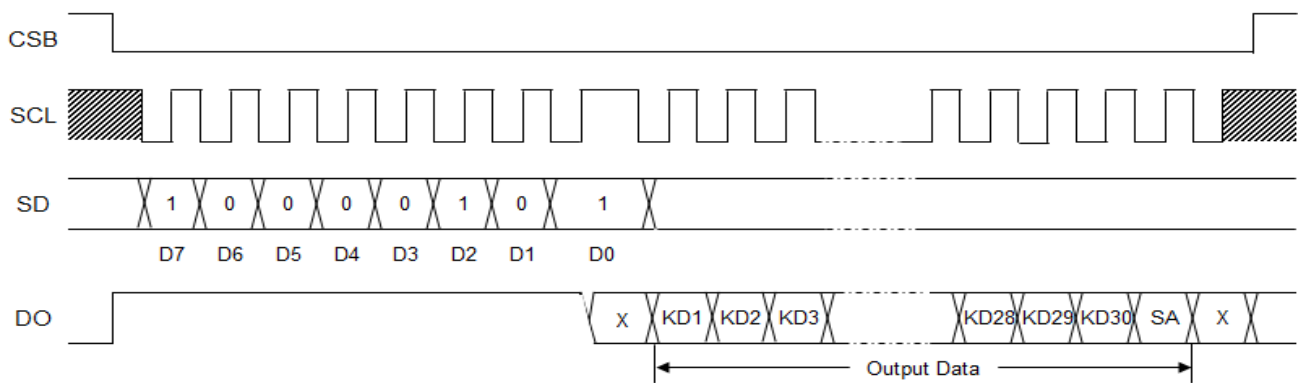


Figure 9. Serial Data Output

KD1 to KD30: Key Data

SA: Sleep Acknowledge Data

Key Data Read Command (KEY RD): 1000_0101

(Note7) If a key data operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data(SA) will be invalid.

Output Data

KD1 to KD30: Key Data

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

| | KI1 | KI2 | KI3 | KI4 | KI5 |
|-----|------|------|------|------|------|
| KS1 | KD1 | KD2 | KD3 | KD4 | KD5 |
| KS2 | KD6 | KD7 | KD8 | KD9 | KD10 |
| KS3 | KD11 | KD12 | KD13 | KD14 | KD15 |
| KS4 | KD16 | KD17 | KD18 | KD19 | KD20 |
| KS5 | KD21 | KD22 | KD23 | KD24 | KD25 |
| KS6 | KD26 | KD27 | KD28 | KD29 | KD30 |

SA: Sleep Acknowledge Data

This output data is used to set the state when the key is pressed. In this case, DO will go to the low level. If serial data is input during this period and the mode is set (normal mode or sleep mode), the IC will be set to that mode. SA is set to 0 in the sleep mode and to 1 in the normal mode.

Key Scan Operation

Key Scan Timing

The key scan period is 288T(s). To reliably determine the on/off state of the keys, the BU91501KV-M scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 610T(s) after starting a key scan. If the key data does not agree and a key is pressed at that point, it scans the keys again. Thus, BU91501KV-M cannot detect a key press shorter than 610T(s).

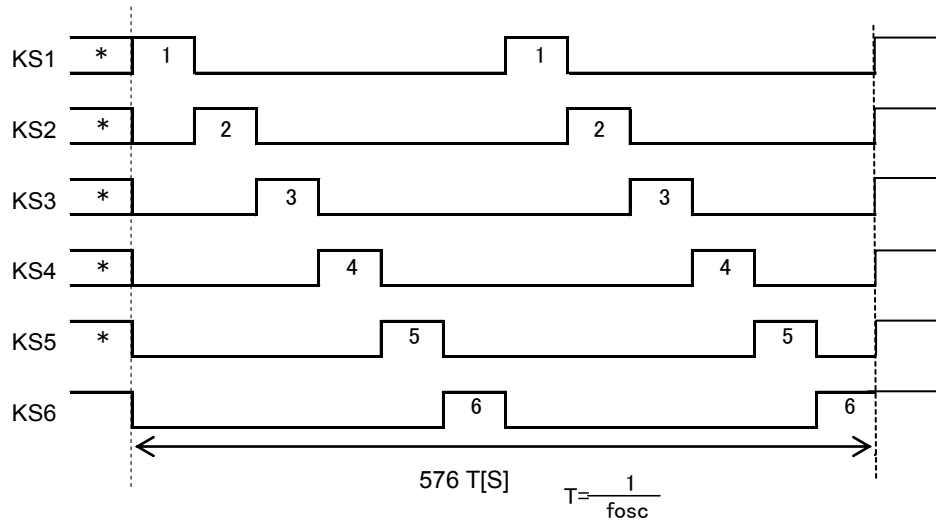


Figure 10. Key Scan Timing

Normal Mode

KS1/S42 - KS6/S47 pins are set high.

When a key is pressed, a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than 610 T(s) (Where $T = 1/f_{osc}$ (When External clock input, f_{osc} is a quarter of external clock)), the BU91501KV-M outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CSB is "L" during a serial data transfer, DO will be set high.

After the controller reads the key data, the key data read request is cleared (DO is set high) and BU91501KV-M performs another key scan. Also note that DO can be controlled to be an open-drain output or a CMOS output. If set to be an open-drain output, a pull-up resistor (between 1 and 10KΩ) is required.

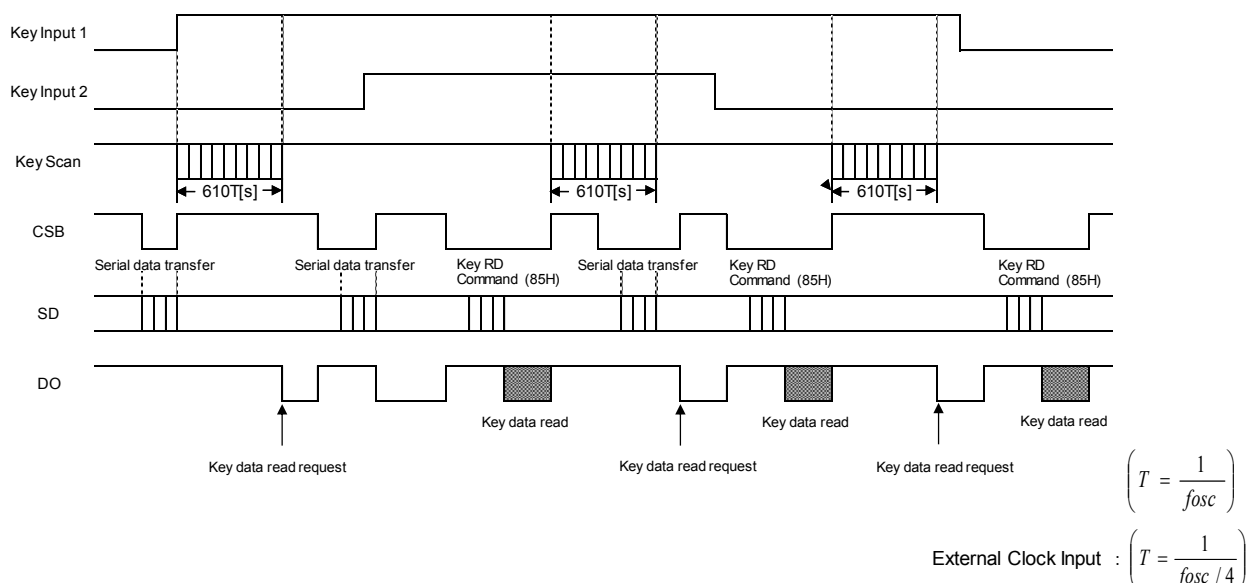


Figure 11. Key scan operation in normal mode

Sleep Mode

KS1/S42 - KS6/S47 pins are set high or low by SLP CTRL P3,P2 data. (Refer to the SLP CTRL description).

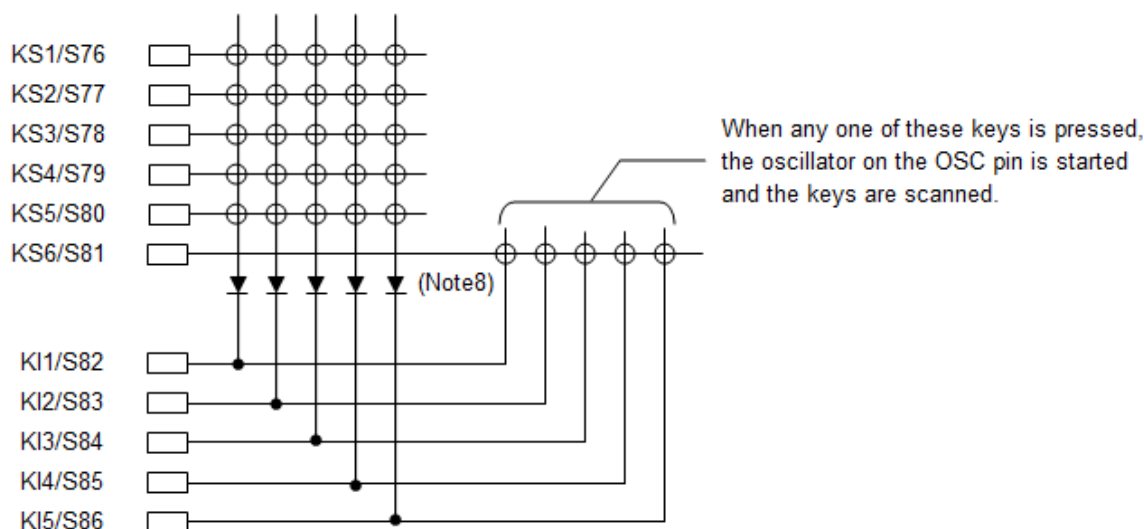
If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than $610T(s)$ (Where $T=1/\text{fosc}$ (When External clock input, fosc is a quarter of external clock)) the BU91501KV-M outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CSB is "L" during a serial data transfer, DO will be set high.

After the controller reads the key data, the key data read request is cleared (DO is set high) and the BU91501KV-M performs another key scan. However, this does not clear sleep mode. Also note that DO can be controlled to be an open-drain output or a CMOS output. During open-drain output selection, DO is an open-drain output so a pull-up resistor (between 1 K Ω and 10K Ω) is required.

Sleep mode key scan example

Example: when SLP CTRL P3= [0], P2= [1] (sleep with only KS6 high)



(Note8) These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.

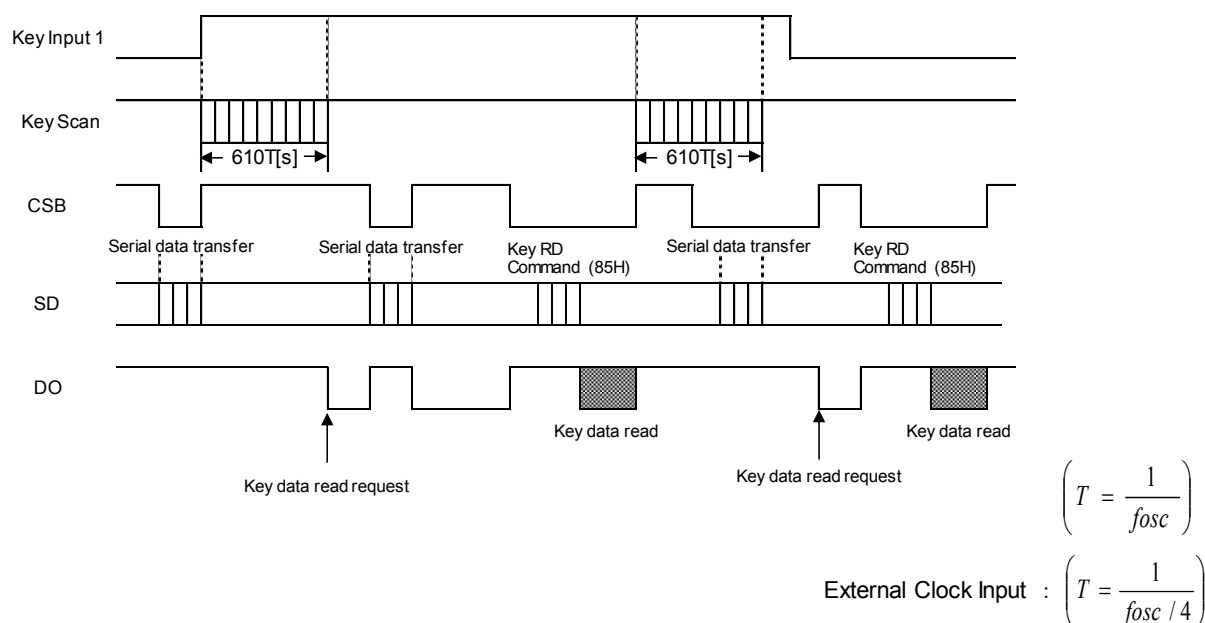


Figure 12. Key scan operation in sleep mode

Multiple Key Presses

Although the BU91501KV-M is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bit and ignore such data.

OSCILLATOR

Several kinds of clock for logic and analog circuits are generated from internal oscillation circuit or external clock. The OSC pins are open or connected to VSS if the internal oscillator is used.

(Note9) To use external clock mode, please set in DRV CTRL1 command.

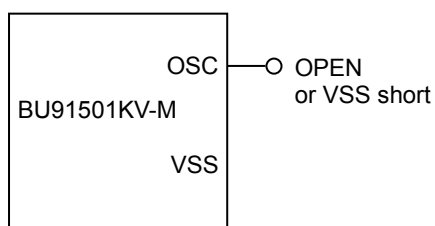


Figure 13. Internal clock mode

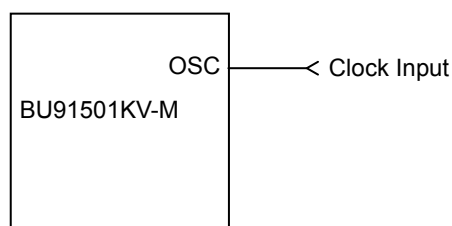


Figure 14. External clock mode

LCD Driver Bias/Duty Circuit

This LSI generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
* 1/3 or 1/2Bias and line or frame inversion mode can be selected by DRV CTRL2.
* 1/4 or 1/3Duty can be selected by DRV CTRL1 command.
Refer to “LCD waveform” about each LCD waveform.

LCD waveform

1/4duty, 1/3bias
Line inversion

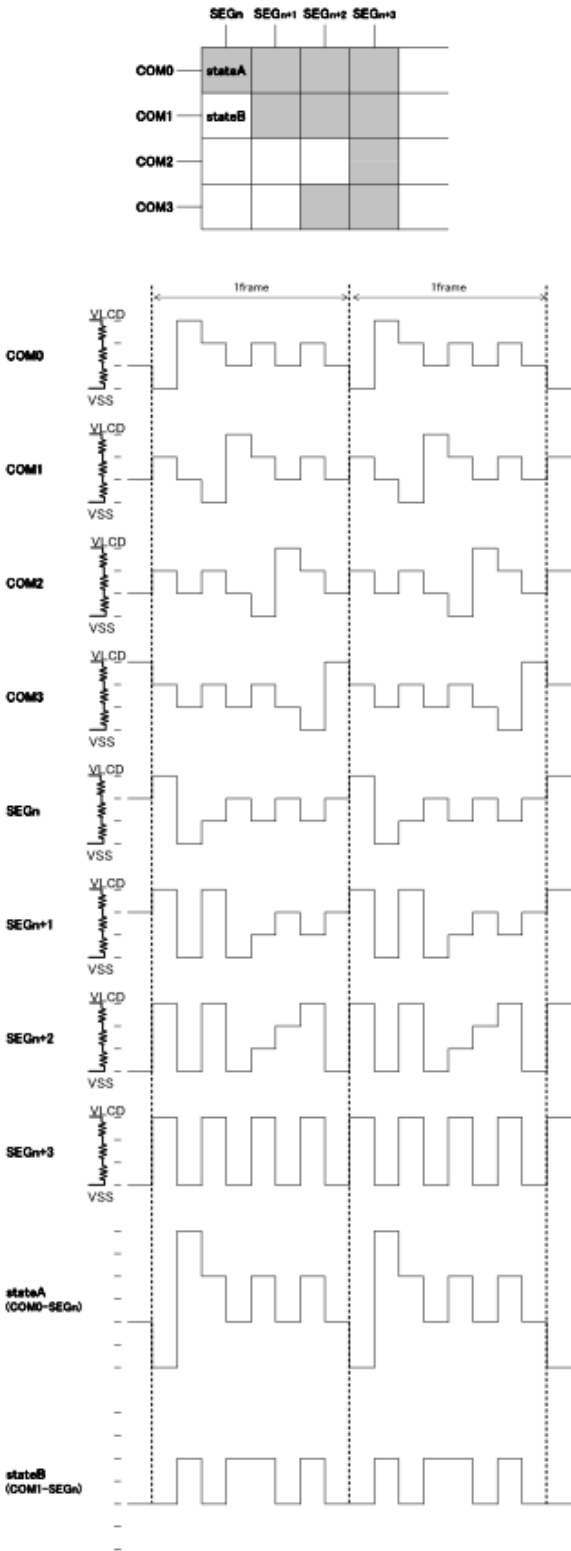


Figure 15. LCD waveform in line inversion

Frame inversion

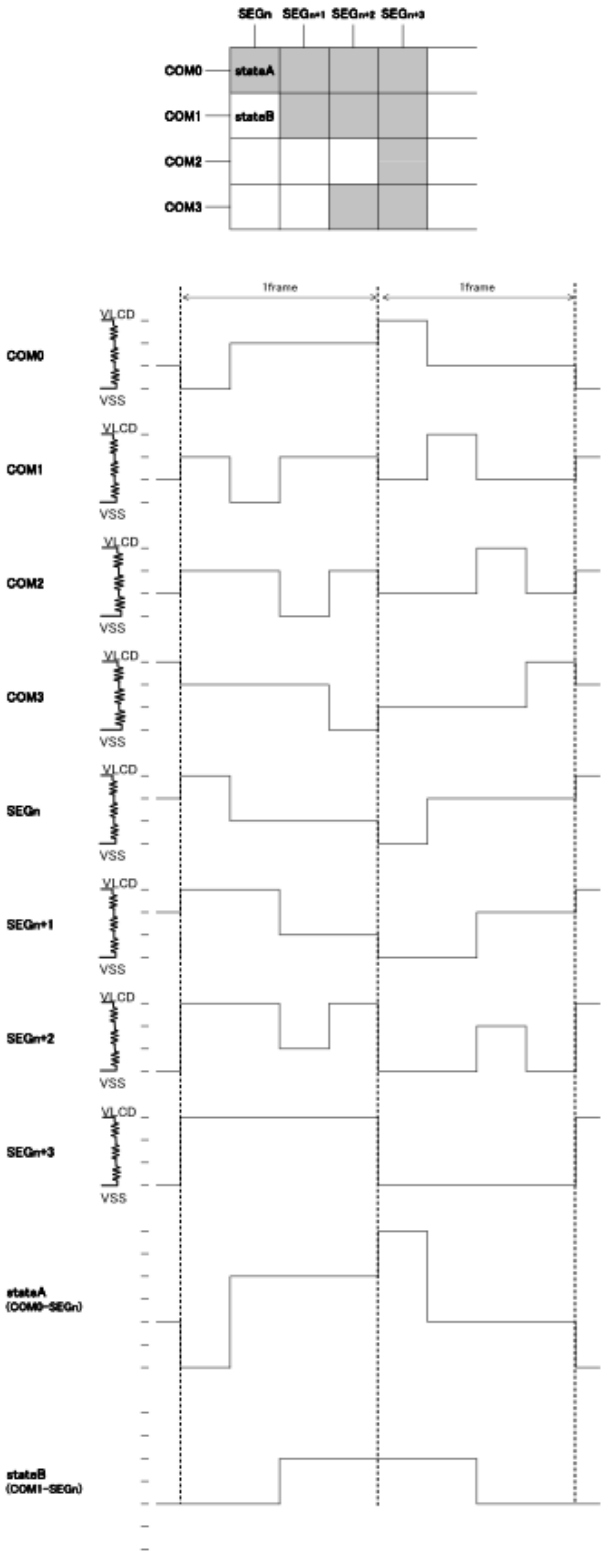


Figure 16. LCD waveform in frame inversion

1/4duty, 1/2bias
Line inversion

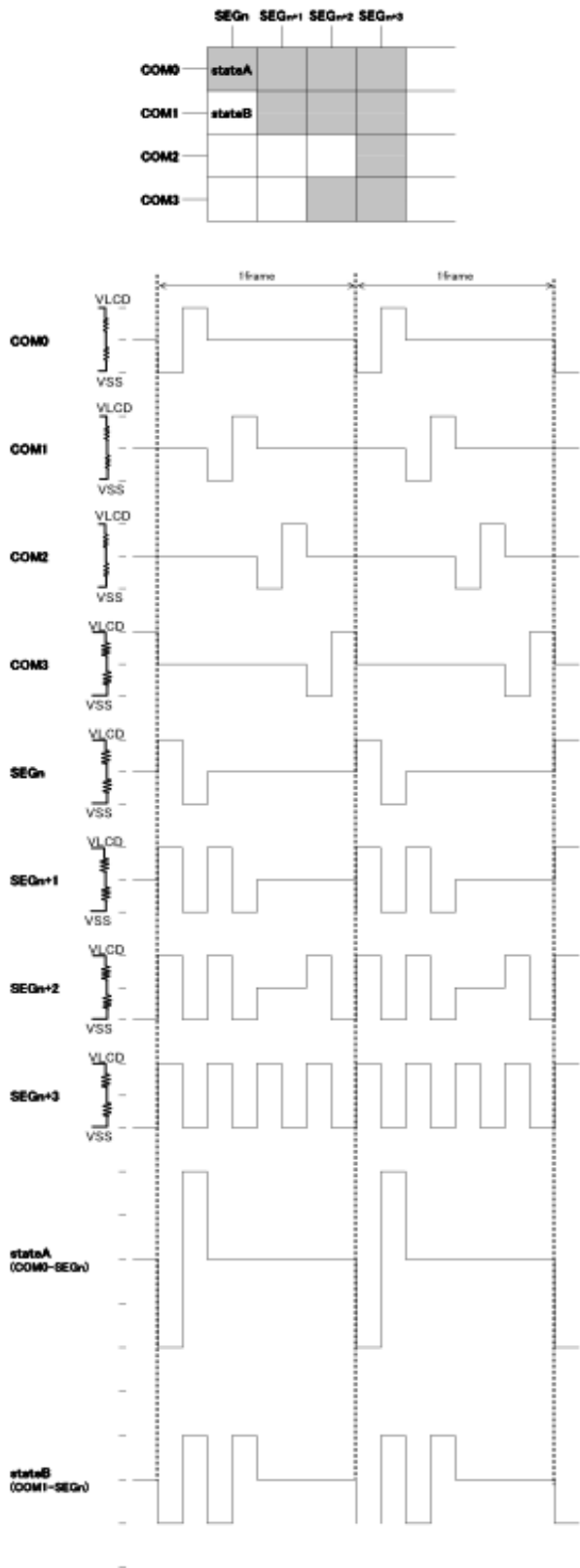


Figure 17. LCD waveform in line inversion

Frame inversion

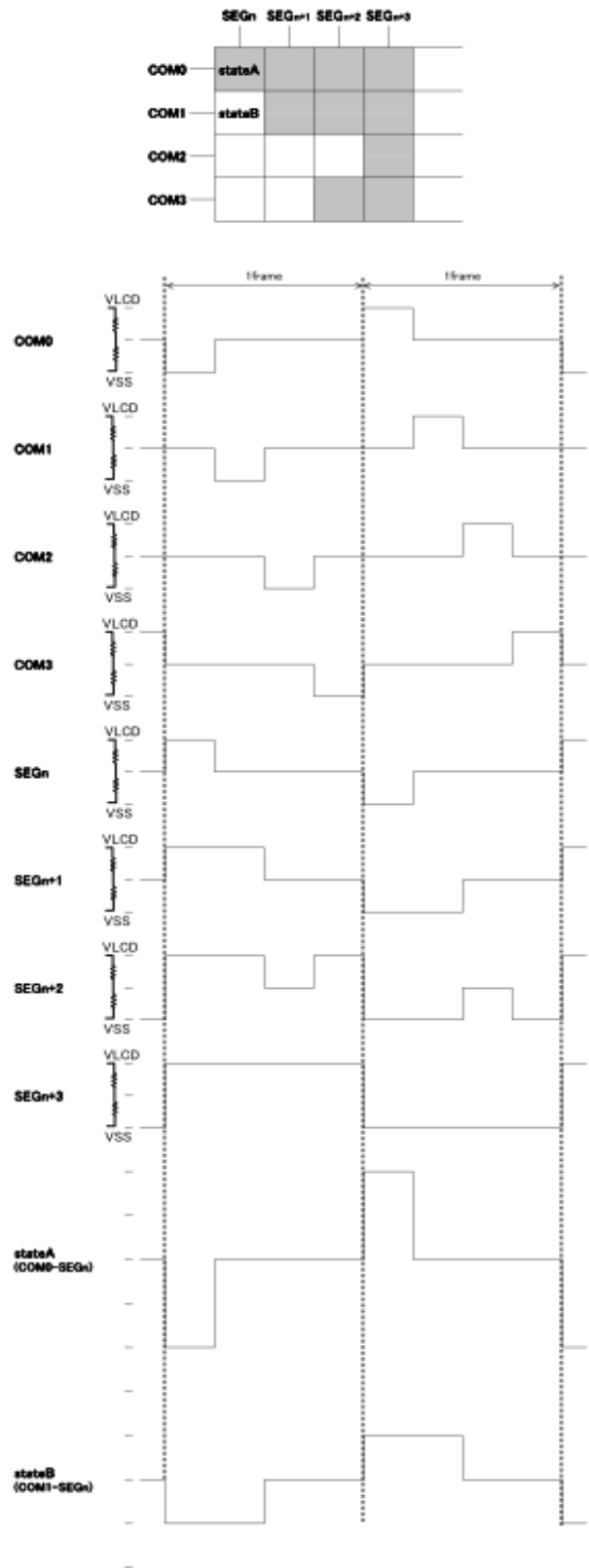


Figure 18. LCD waveform in frame inversion

1/3duty, 1/3bias
Line inversion

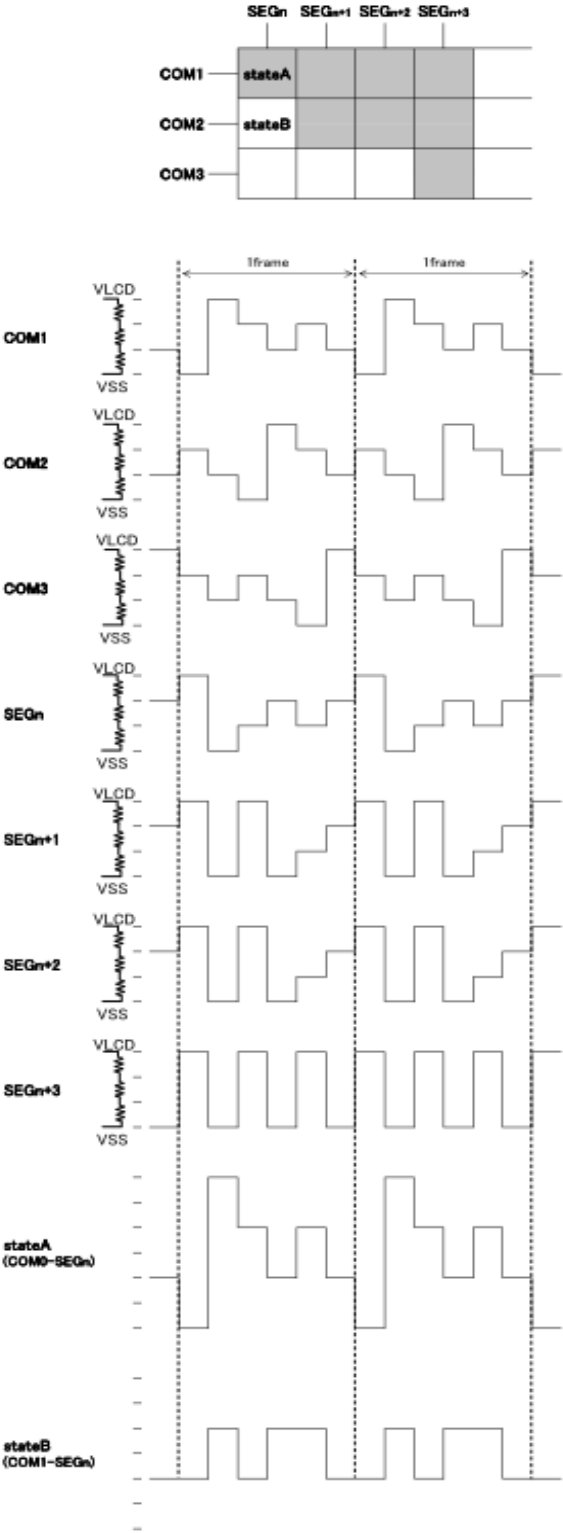


Figure 19. LCD waveform in line inversion

Frame inversion

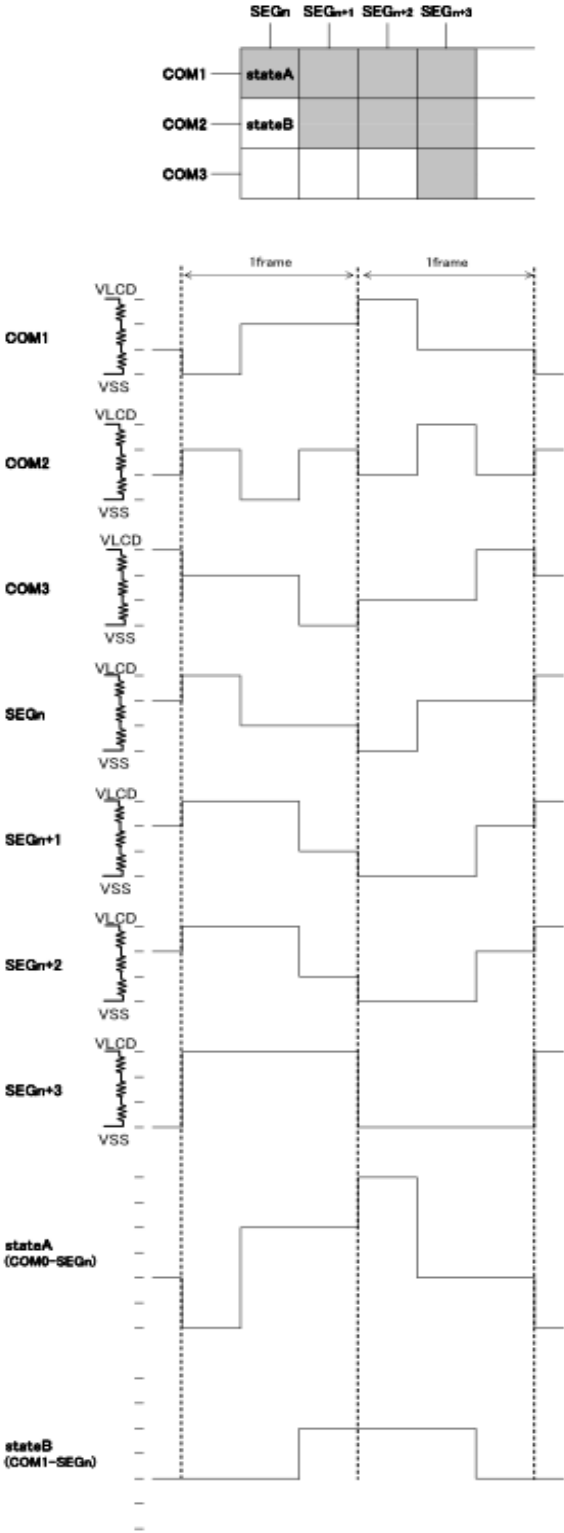


Figure 20. LCD waveform in frame inversion

1/3duty, 1/2bias
Line inversion

Frame inversion

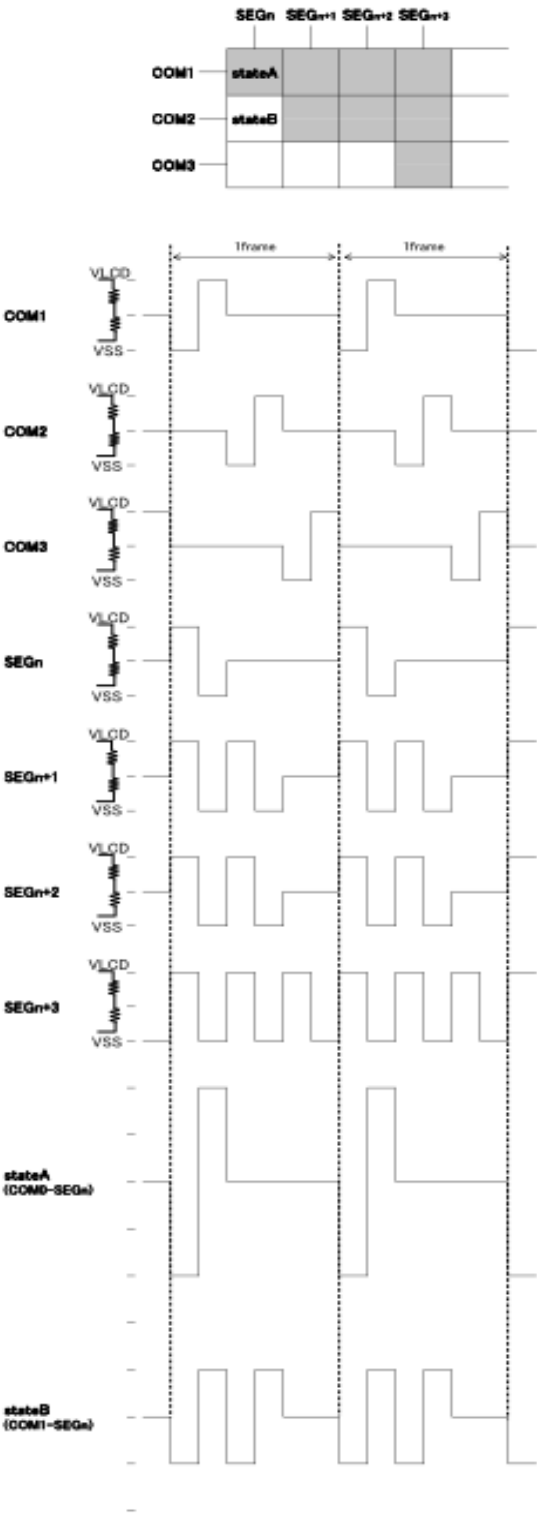


Figure 21. LCD waveform in line inversion

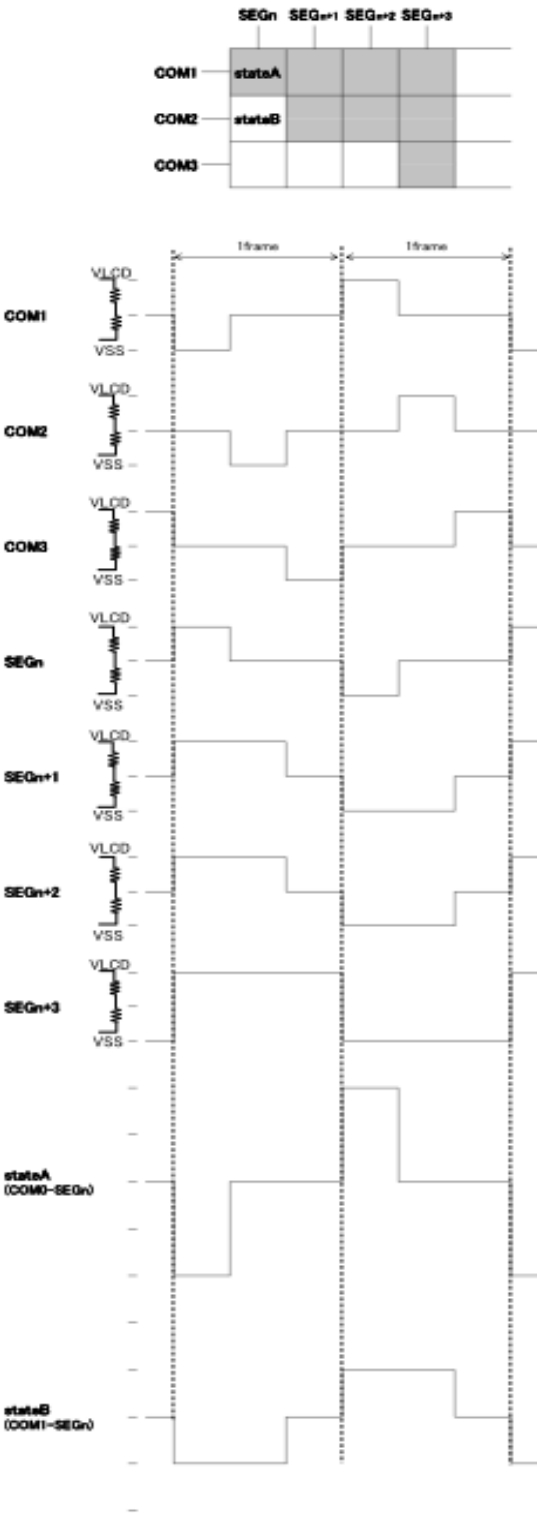


Figure 22. LCD waveform in frame inversion

Command Table

| Command. | BIN | | | | | | | | Descriptions |
|-----------|-----|----|----|----|----|----|----|----|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| SLP CTRL | 1 | 0 | 0 | 1 | P3 | P2 | * | * | Sleep Control |
| SEG CTRL | 1 | 0 | 1 | 1 | P3 | P2 | P1 | * | Segment Control |
| DRV CTRL1 | 1 | 1 | 0 | 0 | P3 | P2 | P1 | 0 | Drive Control1 (Duty Set, OSC Control) |
| DRV CTRL2 | 1 | 1 | 0 | 1 | 0 | P2 | P1 | 0 | Drive Control2 (Bias Set, Inversion Mode) |
| DRV CTRL3 | 1 | 0 | 1 | 0 | P3 | P2 | * | P0 | Drive Control3 (Keyscan Output Set, DO Set) |
| KEY RD | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Key Data Read |
| SWRST | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Software Reset |
| DISCTRL | 1 | 1 | 1 | 1 | 1 | 0 | P1 | * | Display Control (Display On/Off) |
| ADSET | 0 | 1 | P5 | P4 | P3 | P2 | P1 | P0 | Address Set |
| DATA WR | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Data Write |

(* : Don't care)

Detailed command description

Sleep Control (SLP CTRL)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | P3 | P2 | * | * |

(* : Don't care)

P3, P2: Normal mode/Sleep mode switching control data

These control data bits select Key Scan Output Pins KS1 to KS6 States of during Key Scan Standby.

| Control bits | | Mode | Internal OSC | Segment outputs/Common Outputs | Output Pin States During Key Scan Standby | | | | | | Reset Conditions |
|--------------|----|--------|--------------|--------------------------------|---|-----|-----|-----|-----|-----|------------------|
| P3 | P2 | | | | KS1 | KS2 | KS3 | KS4 | KS5 | KS6 | |
| 0 | 0 | Normal | enabled | Operating | H | H | H | H | H | H | |
| 0 | 1 | Sleep | disabled | Low(VSS) | L | L | L | L | L | H | ○ |
| 1 | 0 | Sleep | | | L | L | L | L | H | H | |
| 1 | 1 | Sleep | | | H | H | H | H | H | H | |

(Note10) When DRV CTRL3 (P3, P2) = (1, 1), KS1 to KS6 outputs are selected as Segment outputs.

Segment Control (SEG CTRL)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 1 | 1 | P3 | P2 | P1 | * |

(* : Don't care)

P3 to P1 : Segment Output / General purpose output switching control data

These control bits select the function of the S1/P1 to S4/P4 output pins.

(Segment Output Pins or General Purpose Output Pins).

| Control bits | | | Status of the pins | | | | Reset conditions |
|--------------|----|----|--------------------|-------|-------|-------|------------------|
| P3 | P2 | P1 | S1/P1 | S2/P2 | S3/P3 | S4/P4 | |
| 0 | 0 | 0 | S1 | S2 | S3 | S4 | ○ |
| 0 | 0 | 1 | P1 | S2 | S3 | S4 | |
| 0 | 1 | 0 | P1 | P2 | S3 | S4 | |
| 0 | 1 | 1 | P1 | P2 | P3 | S4 | |
| 1 | 0 | 0 | P1 | P2 | P3 | P4 | |

(Note11) Sn(n=1 to 4) : assigned as a Segment Output pin
 Pn(n=1 to 4) : assigned as a General Purpose Output pin

Relationship of bit assignment between general purpose output pin and bit in DDRAM

| Output Pin | Corresponding bit in DDRAM | |
|------------|----------------------------|----------|
| | 1/3 Duty | 1/4 Duty |
| S1/P1 | D1 | D1 |
| S2/P2 | D4 | D5 |
| S3/P3 | D7 | D9 |
| S4/P4 | D10 | D13 |

In case of 1/4 Duty mode and S4/P4 is configured as a general purpose output pins.

S4/P4 is set to HIGH (VLCD level) if D13 is set to "1" in DDRAM.

S4/P4 is cleared to LOW (VSS level) if D13 is set to "0" in DDRAM.

Drive Control1 (DRV CTRL1)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 0 | 0 | P3 | P2 | P1 | 0 |

P3: 1/3 duty drive or 1/4 duty drive switching control data

This control data bit selects either 1/3 duty drive or 1/4 duty drive.

| P3 | Duty mode | Status of (COM4/ S41) | Reset conditions |
|----|-----------|--------------------------|---------------------|
| 0 | 1/4 | COM4 | ○ |
| 1 | 1/3 | S41 | |

(Note12) COM4: COMMON output
S41: SEGMENT output

P2,P1 : Frame frequency switching control data

These control data bits select Frame frequency setting.

| Setting | P2 | P1 | Reset conditions |
|-------------------------|----|----|---------------------|
| 80Hz | 0 | 0 | ○ |
| 100Hz | 0 | 1 | |
| 120Hz | 1 | 0 | |
| External Clock input | 1 | 1 | |

Relationships between Frame frequency (fFR) and Divide number

| P2 | P1 | Divide number | | fFR [Hz] | |
|----|----|---------------|----------|----------|----------|
| | | 1/3 Duty | 1/4 Duty | 1/3 Duty | 1/4 Duty |
| 0 | 0 | 510 | 512 | 80 | 80 |
| 0 | 1 | 408 | 408 | 100 | 100 |
| 1 | 0 | 342 | 344 | 120 | 120 |
| 1 | 1 | 2040 | 2048 | - | - |

Formula to calculate Frame frequency from frequency and Divide number:
"Frame frequency = frequency / Divide number"

Ex) In case, 1/4 Duty mode, (P2,P1) = (0,0)

$$fFR = 40.96[\text{KHz}] / 512 = 80[\text{Hz}]$$

(Note13) Built-in Oscillator circuit frequency = 40.96 KHz (typ).

Drive Control2 (DRV CTRL2)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 0 | 1 | 0 | P2 | P1 | 0 |

P2: 1/3 bias drive or 1/2 bias drive switching control data

This control data bit selects either 1/3 bias drive or 1/2 bias drive.

| P2 | Bias mode | Reset conditions |
|----|-----------|---------------------|
| 0 | 1/2 | |
| 1 | 1/3 | ○ |

P1: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion drive or frame inversion drive.

| P1 | Inversion mode | Reset conditions |
|----|-------------------|---------------------|
| 0 | Line | ○ |
| 1 | Frame | |

Drive Control3 (DRV CTRL3)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 1 | 0 | P3 | P2 | * | P0 |

(* : Don't care)

P3 to P2: Key Scan output port/Segment output port switching control data

These control data bits select Key Scan outputs or Segment outputs.

| Control Bits | | Output Pin State | | | | | | Maximum Number of Input keys | Reset Conditions |
|--------------|----|------------------|-------------|-------------|-------------|-------------|-------------|------------------------------|------------------|
| P3 | P2 | KS1/ S42 | KS2/ S43 | KS3/ S44 | KS4/ S45 | KS5/ S46 | KS6/ S47 | | |
| 0 | 0 | KS1 | KS2 | KS3 | KS4 | KS5 | KS6 | 30 | |
| 0 | 1 | S42 | KS2 | KS3 | KS4 | KS5 | KS6 | 25 | |
| 1 | 0 | S42 | S43 | KS3 | KS4 | KS5 | KS6 | 20 | |
| 1 | 1 | S42 | S43 | S44 | S45 | S46 | S47 | 0 | ○ |

When (P3,P2)=(1,1), Keyscan doesn't function. Key scan pins are all segment outputs.

Thus, maximum segment display number and RAM last address change based on this value.

| Control Bits | | Status of Pins | | | | | | Maximum Segment Display Number | | Last Address | |
|--------------|----|----------------|-------------|-------------|-------------|-------------|-------------|--------------------------------|----------|--------------|----------|
| P3 | P2 | KS1/ S42 | KS2/ S43 | KS3/ S44 | KS4/ S45 | KS5/ S46 | KS6/ S47 | 1/3 Duty | 1/4 Duty | 1/3 Duty | 1/4 Duty |
| 0 | 0 | KS1 | KS2 | KS3 | KS4 | KS5 | KS6 | 123 | 160 | 28h | 27h |
| 0 | 1 | S42 | KS2 | KS3 | KS4 | KS5 | KS6 | 126 | 164 | 29h | 28h |
| 1 | 0 | S42 | S43 | KS3 | KS4 | KS5 | KS6 | 129 | 168 | 2Ah | 29h |
| 1 | 1 | S42 | S43 | S44 | S45 | S46 | S47 | 156 | 204 | 33h | 32h |

P0: Output setting for DO

This control data bit selects either open drain output or CMOS output.

| P0 | Setting | Reset Conditions |
|----|-------------------|------------------|
| 0 | open drain output | ○ |
| 1 | CMOS output | |

Pull up resistor (1kΩ - 10kΩ) is required when selecting Open Drain Output setting for DO.

Be careful the Pull up voltage not to be higher than VDD voltage.

Key Data Read (KEY RD)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

Display Control (DISCTRL)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 1 | 0 | P1 | * |

(* : Don't care)

P1: Segment on/off control data

This control data bit controls the on/off state of the segments.

| P1 | Display status | Reset conditions |
|----|----------------|------------------|
| 1 | ON | |
| 0 | OFF | ○ |

Software Reset (SWRST)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

This is the Software Reset command.

After sending this command, each register, DDRAM data and DDRAM address are initialized.

Address Set (ADSET)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | P5 | P4 | P3 | P2 | P1 | P0 |

Address which could be set starts from 00(Hex) until RAM last address.

Setting of values other than the above is not allowed. (Otherwise, address is set to 0.)

Refer to "Display Data Transfer Method" for RAM last address.

Data Write (DATAWR)

| MSB | | | | LSB | | | |
|-----|----|----|----|-----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

Data transfer can be started by this command.

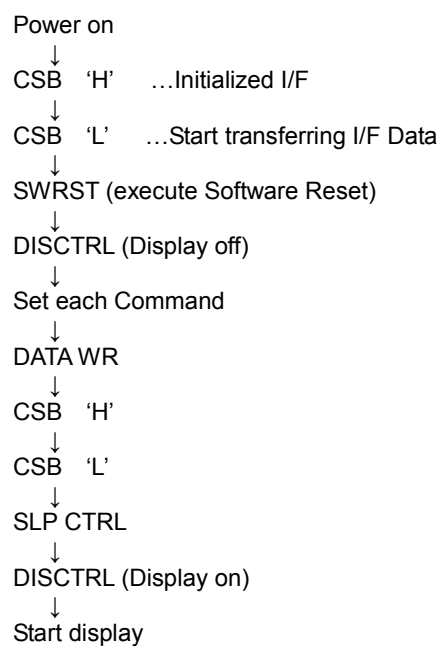
Set the CSB pin to High to terminate the data transfer.

Refer to "Command and Data Transfer Method".

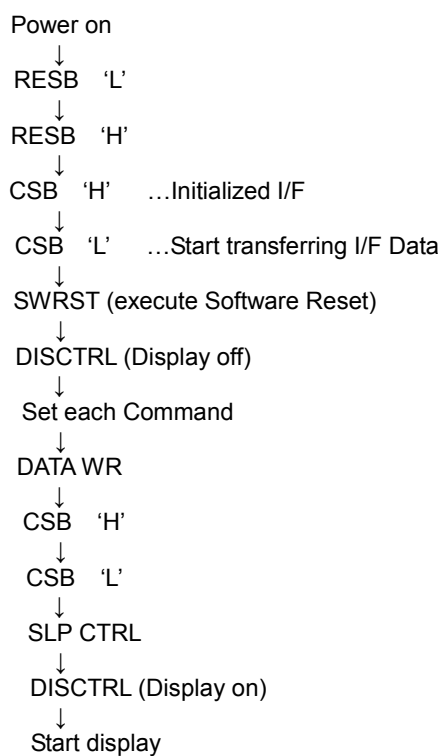
Initialize sequence

Recommended sequence after Power-On to set this device to initial condition.

Software reset sequence



Hardware reset sequence



(Note14) Each register value, DDRAM address and DDRAM data are random condition after power on till initialize sequence is executed.

(Note15) Each register value, DDRAM address are reset by a hardware reset operation.

Cautions in Power-On Sequence

Power-On Reset (POR) Circuit

This LSI has "P.O.R" (Power-On Reset) circuit and Software Reset function.
When the power is ON, IC internal circuit and reset pass through unstable low-voltage region.
Internal IC is not totally reset because VDD rises and this may result to malfunction.
Thus, POR circuit and function of software reset are installed in order to prevent this.
Please follow the following recommended Power-On sequences to allow the reset action to complete.

Set the power up conditions to meet the recommended t_R , t_F , t_{OFF} , and V_{bot} spec below in order to ensure P.O.R operation.

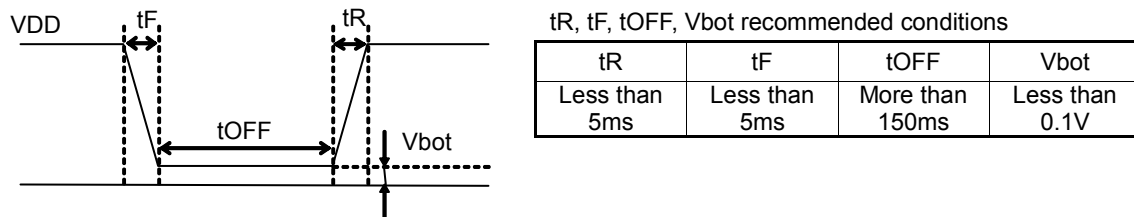


Figure 23. Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.

- (1) Set CSB to High
- (2) Clear CSB to Low and then issue a SWRST command.

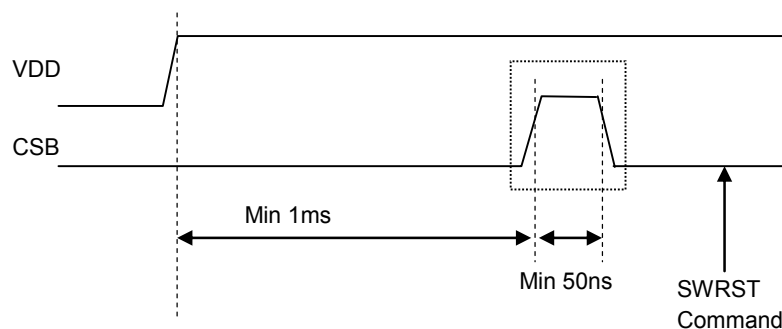


Figure 24. SWRST Command Sequence

Power Up Sequence and Power Down Sequence

To prevent incorrect display, malfunction and abnormal current,
VDD must be turned on before VLCD in power up sequence.
VDD must be turned off after VLCD in power down sequence.
Please satisfies $VLCD \geq VDD$, $t_1 > 0ns$, $t_2 > 0ns$

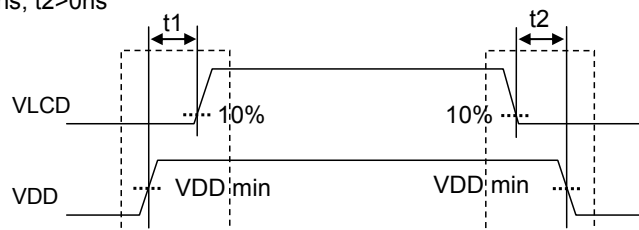


Figure 25. Power On/Off Sequence

DISPLAY DDRAM DATA EXAMPLE

If LCD layout pattern is shown as in Figure 26 and 27 and DDRAM data is shown as in Table2, display pattern will be shown as in Figure 28.

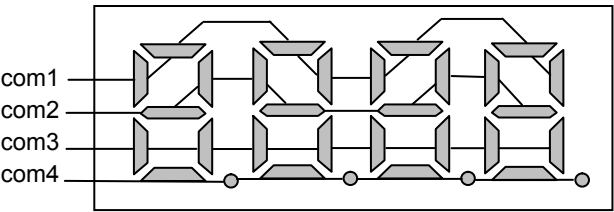


Figure 26. Example COM Line pattern

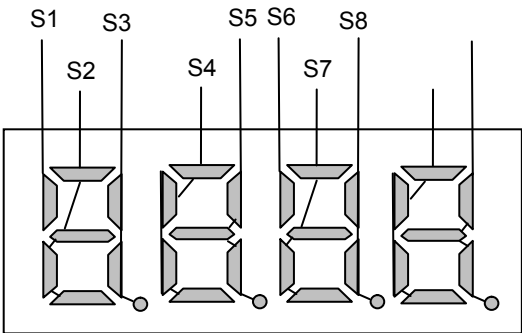


Figure 27. Example of SEG Line pattern

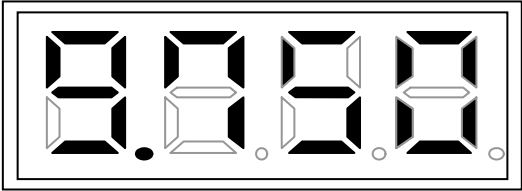


Figure 28. Example of display pattern

| | | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | S | |
|---------|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
| COM1 | D0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COM2 | D1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COM3 | D2 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COM4 | D3 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Address | | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h |

Table 2. DDRAM Data map

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued**11. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

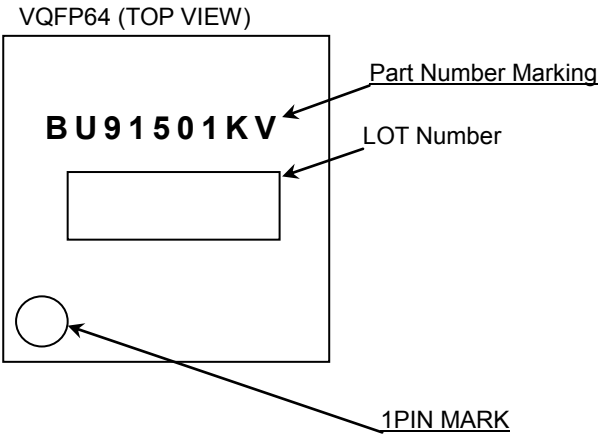
14. Data transmission

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

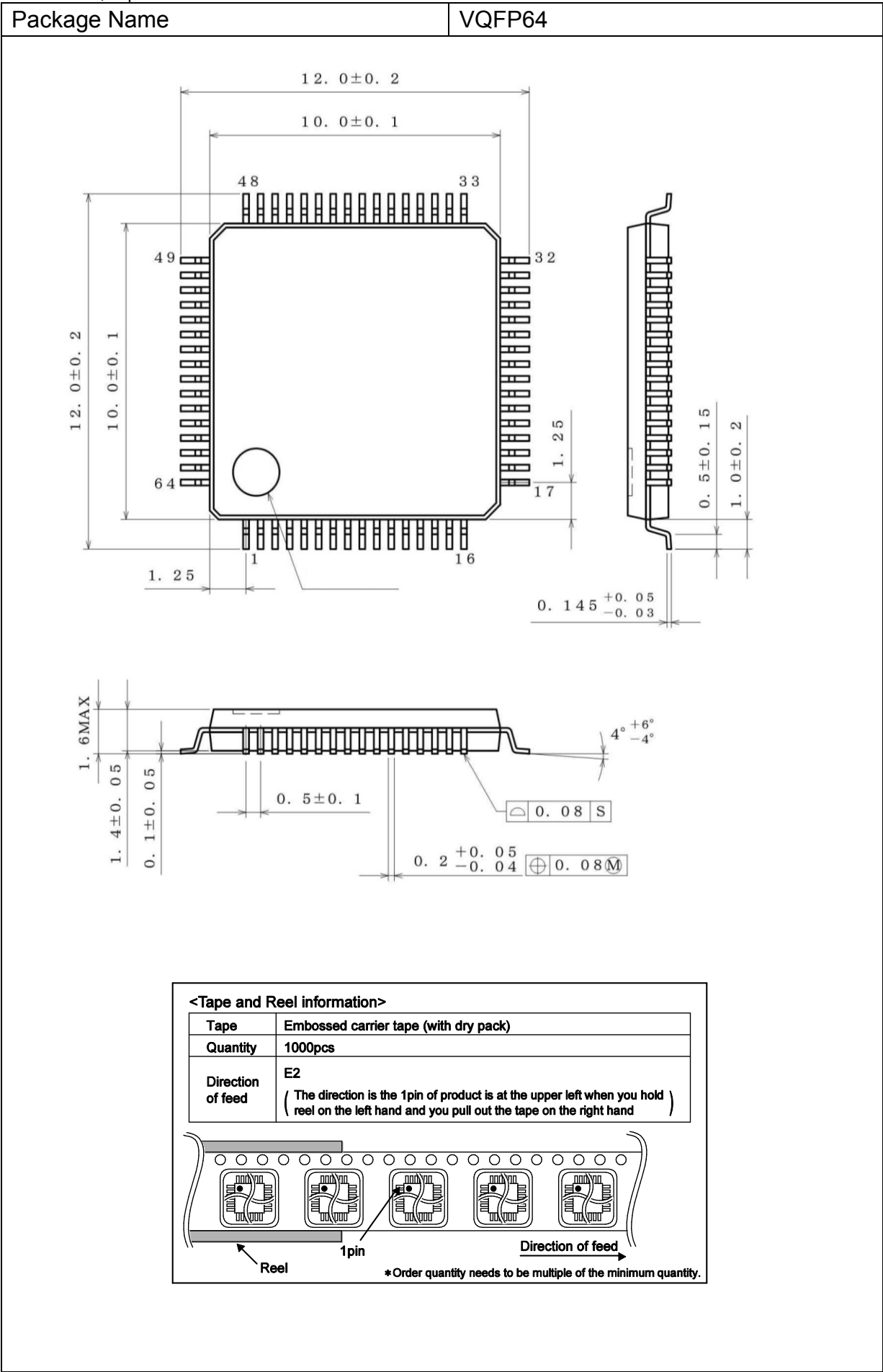
Ordering Information

| | | | | | | | | | | | | |
|-------------------|--|--|--|--|--|--|--|--|--|-------------|-------------------------------------|--|
| B U 9 1 5 0 1 K V | | | | | | | | | | - | M E 2 | |
| Part Number | | | | | | | | | | Package | Packaging and forming specification | |
| | | | | | | | | | | KV : VQFP64 | M: for Automotive | |
| | | | | | | | | | | | E2: Embossed tape and reel | |
| | | | | | | | | | | | (VQFP64) | |

Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

| Version | Date | Description |
|---------|-------------|-------------|
| 001 | 8.July.2015 | New edition |

Notice

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| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BU91501KV-M - Web Page

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| | |
|-----------------------------|-------------|
| Part Number | BU91501KV-M |
| Package | VQFP64 |
| Unit Quantity | 1000 |
| Minimum Package Quantity | 1000 |
| Packing Type | Taping |
| Constitution Materials List | inquiry |
| RoHS | Yes |