

Serial-in / Parallel-out Driver Series

4-input Serial-in / Parallel-out Drivers

BU2099FV

Description

BU2099FV is an open drain output driver. It incorporates a built-in shift register and a latch circuit to turn on a maximum of 12 output by a 4-line interface, linked to a microcontroller.

An open drain output provides maximum 25mA current.

Features

- LED can be driven directly
- 12bit parallel outputs
- This product can be operated on low voltage

Applications

- Drive of LED
- Drive of Solenoid
- Drive of Relay

Key Specifications

- Power supply voltage range: +2.7V to +5.5V
- Output voltage: 0V to +25.0V
- Operating temperature range: -40°C to +85°C

Package

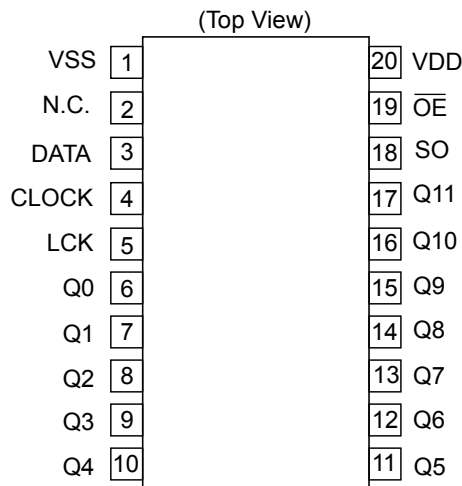
SSOP-B20

W(Typ) x D(Typ) x H(Max)
6.50mm x 6.40mm x 1.45mm

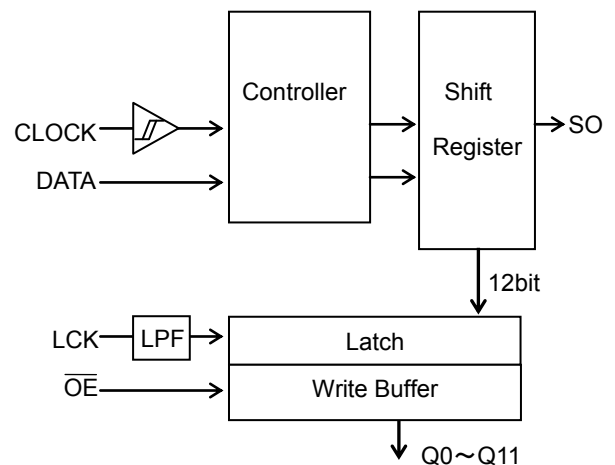


SSOP-B20
BU2092FV

Pin Configurations



Block Diagrams



Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	VSS	-	Ground
2	N.C.	-	Non Connected
3	DATA	I	Serial Data Input
4	CLOCK	I	Shift clock of DATA (Rising Edge Trigger)
5	LCK	I	Latch clock of DATA (Rising Edge Trigger)
6	Q0	O	Parallel Data Output (Nch Open Drain)
7	Q1		
8	Q2		
9	Q3		
10	Q4		
11	Q5		
12	Q6		
13	Q7		
14	Q8		
15	Q9		
16	Q10		
17	Q11		
18	SO	O	Serial Data Output
19	$\overline{\text{OE}}$	I	Output Enable ("H" level : output FET is OFF)
20	VDD	-	Power Supply

Latch Data	L	H
Output	ON	OFF

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Voltage	V_O	V_{SS} to +25.0	V
Operating Temperature	T_{opr}	-40 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	0.75 (Note 1)	W

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 7.5mW per 1°C above 25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions ($T_A=25^\circ\text{C}$, $V_{SS}=0\text{V}$)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	+2.7 to +5.5	V
Output Voltage	V_O	0 to +25.0	V

Electrical Characteristics

DC Characteristics (Unless otherwise specified, $V_{DD}=5.0V$, $V_{SS}=0V$, $T_A=25^\circ C$)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input high-level Voltage	V_{IH}	3.5	-	-	V	-
Input low-level Voltage	V_{IL}	-	-	1.5	V	-
Output Hi-level Voltage (SO)	V_{OH}	$V_{DD}-0.5$	-	-	V	$I_{OH}=-400\mu A$
Output low-level Voltage1 (Qx)	V_{OL1}	-	-	1.0	V	$I_{OL1}=10mA$
		-	-	1.5		$I_{OL1}=15mA$
		-	-	2.0		$I_{OL1}=20mA$
Output low-level Voltage 2 (SO)	V_{OL2}	-	-	0.4	V	$I_{OL2}=1.5mA$
Output high-level Leak Current (Qx)	I_{OZH}	-	-	10	μA	$V_O=25.0V$
Output low-level Leak Current (Qx)	I_{OZL}	-	-	-5.0	μA	$V_O=0V$
Pull-down Current (\overline{OE})	I_{PD}	-	-	150	μA	$\overline{OE}=V_{DD}$
Reset Voltage at Low Supply Voltage	V_{CLR}	1.1	-	2.4	V	-
Quiescent Current	I_{DD}	-	-	200	μA	$V_{IN}=V_{SS}$ or V_{DD} , OUTPUT:OPEN

Timing Characteristics (Unless otherwise specified $V_{SS}=0V$, $T_A=25^\circ C$)

Parameter	Symbol	Limit			Unit	$V_{DD}(V)$	Condition
		Min	Typ	Max			
Minimum Clock Pulse Width (CLOCK)	t_W	1000	-	-	ns	3	-
		500	-	-	ns	5	
Minimum Latch Pulse Width (LCK)	t_W (LCK)	1000	-	-	ns	3	-
		500	-	-	ns	5	
Setup Time (LCK→CLOCK)	t_S	400	-	-	ns	3	-
		200	-	-	ns	5	
Setup Time (DATA→CLOCK)	t_{SU}	400	-	-	ns	3	-
		200	-	-	ns	5	
Hole Time (CLOCK→DATA)	t_H	400	-	-	ns	3	-
		200	-	-	ns	5	
Propagation (SO)	t_{PLH}	-	-	500	ns	3	-
	t_{PHL}	-	-	250	ns	5	-
Propagation (LCK→Q _x)	t_{PLZ} (LCK)	-	360	-	ns	3	RL=5kΩ CL=10pF
		-	170	-	ns	5	
	t_{PZL} (LCK)	-	260	-	ns	3	RL=5kΩ CL=10pF
		-	175	-	ns	5	
Propagation (\overline{OE} →Q _x)	t_{PLZ}	-	115	-	ns	3	RL=5kΩ CL=10pF
		-	85	-	ns	5	
	t_{PZL}	-	175	-	ns	3	RL=5kΩ CL=10pF
		-	65	-	ns	5	
Noise Pulse Suppression Time (LCK)	t_i	-	30	-	ns	5	-
		-	20	-	ns	5	

Electrical Characteristics - continued

Waveform of Timing Characteristics

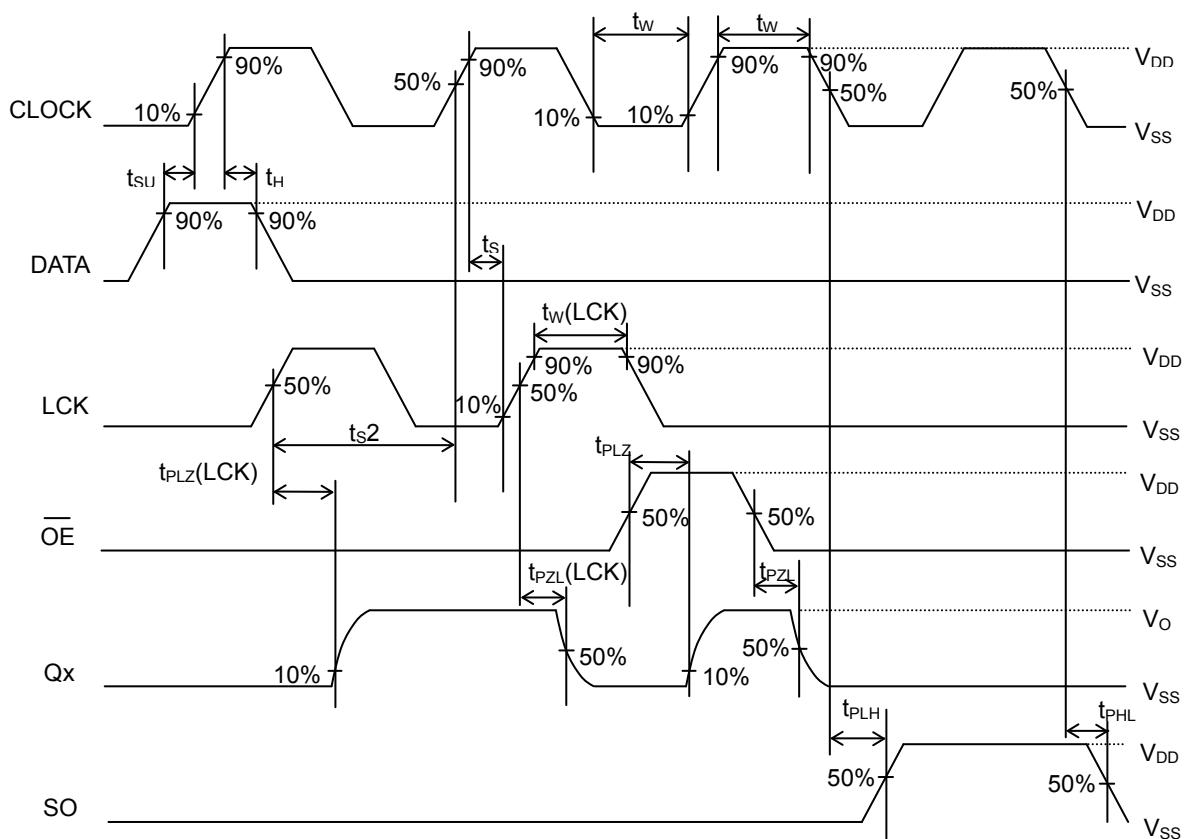


Figure 1. Waveform of Timing Characteristics

Test Circuits

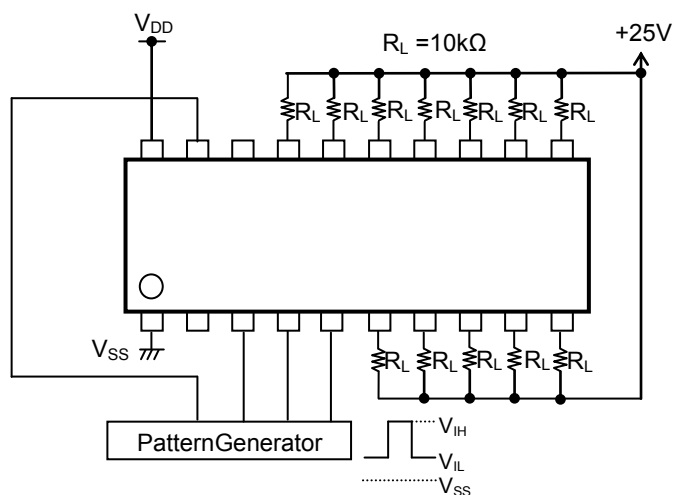


Figure 2. Test Circuit of Input Voltage

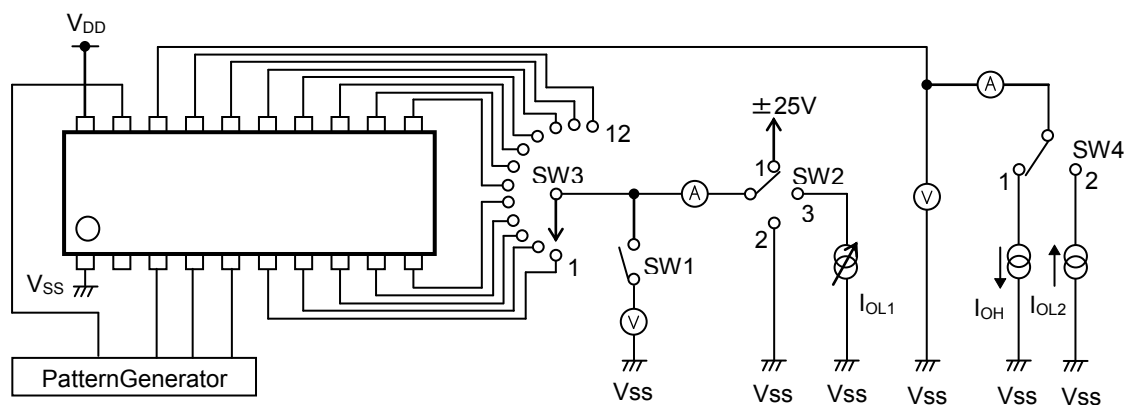


Figure 3. Test Circuit of Output Voltage

Test condition

V_{OL1} : Set all data "L". SW1="ON", SW2="3", SW3="1"~"12".

V_{OL2} : Set output data "L" to SO and SW4 is positioned to "2", then voltage is measured at I_{OL2} .

V_{OH} : Set output data "H" to SO and SW4 is positioned to "1", then voltage is measured at I_{OH} .

Test Circuits - continued

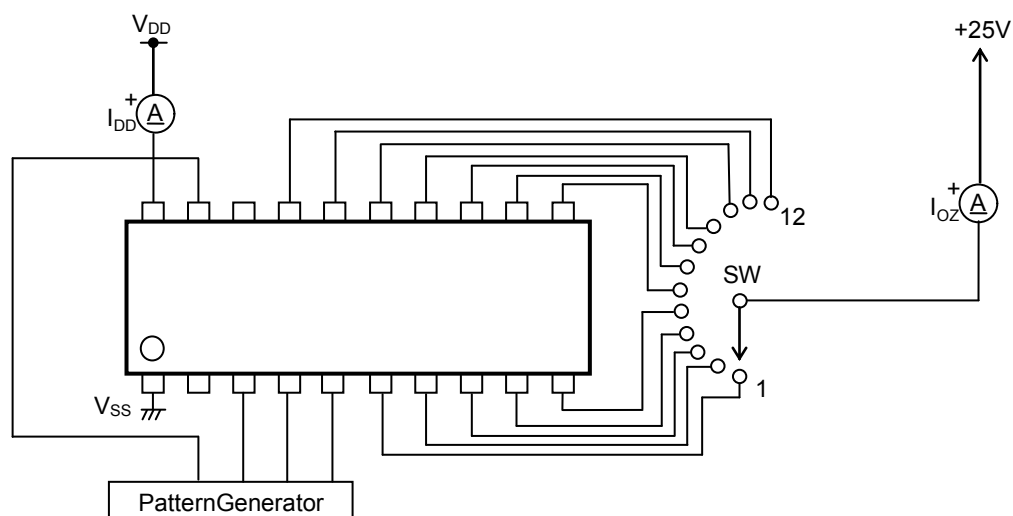


Figure 4. Test Circuit of Output Leak Current / Static Dissipation Current

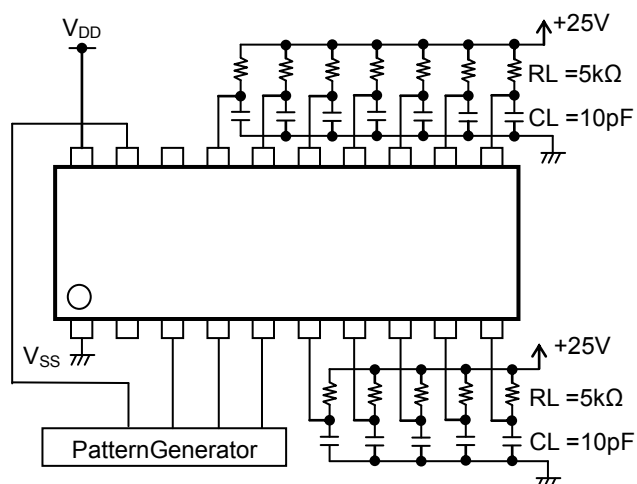


Figure 5. Test Circuit of Timing Characteristics

Timing Chart

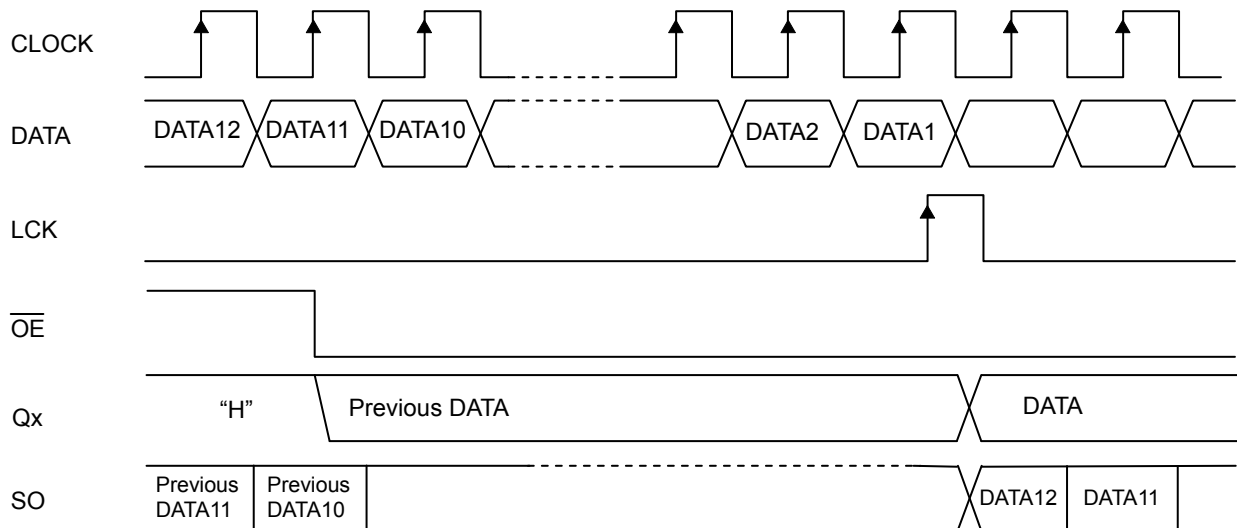


Figure 6 . Timing Chart

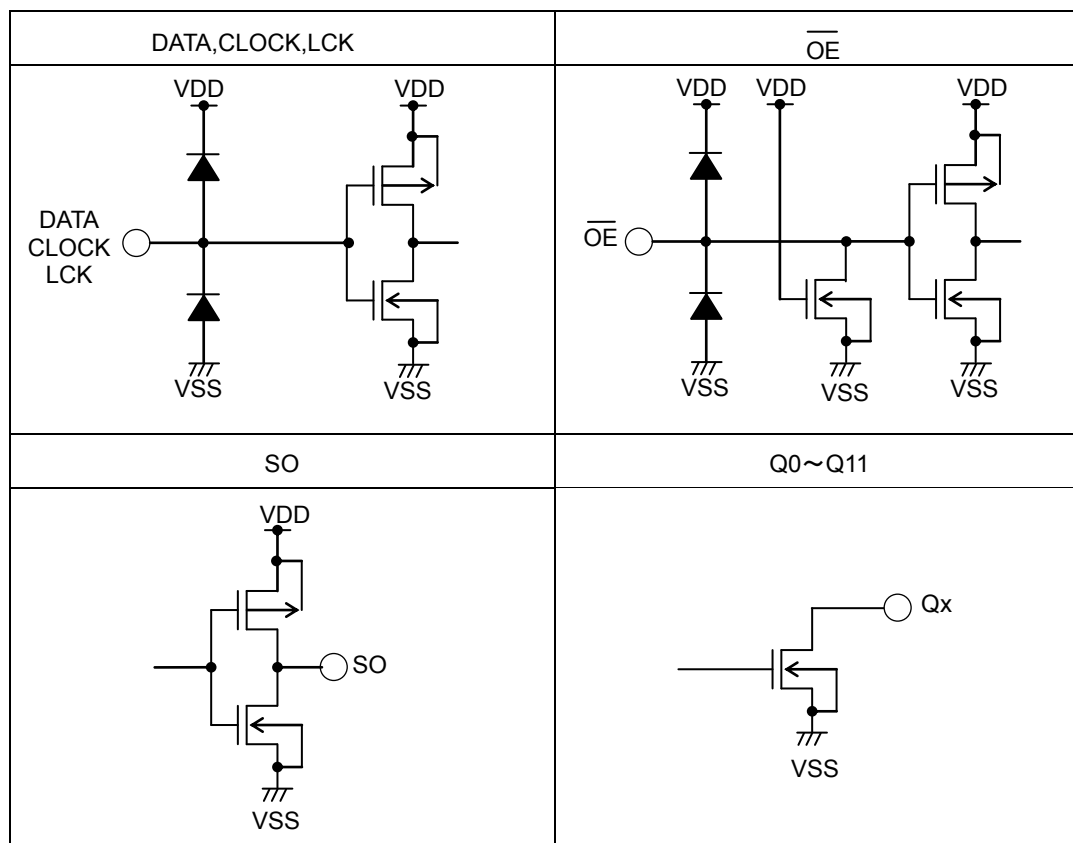
1. After the power is turned on and the voltage is stabilized, LCK should be activated, after clocking 12 data bits into the DATA terminal.
2. Qx parallel output data of the shift register is set after the 12th clock by the LCK.
3. Since the LCK is a label latch, data is retained in the "L" section and renewed in the "H" section of the LCK.
4. Data retained in the internal latch circuit is output when the \overline{OE} is in the "L" section.
5. The final stage data of the shift register is output to the SO by synchronizing with the rise time of the CLOCK.

[Truth Table]

Input				Function
CLOCK	DATA	LCK	\overline{OE}	
x	x	x	H	All the output data output "H" with pull-up.
x	x	x	L	The Q0~Q11 output can be enable and output the data of storage register.
\downarrow	L	x	x	Store "L" in the first stage data of shift register, the previous stage data in the others. (The conditions of storage register and output have no change.)
\downarrow	H	x	x	Store "H" in the first stage data of shift register, the previous stage data in the others. (The conditions of storage register and output have no change.)
\downarrow	x	x	x	The data of shift register has no change. SO outputs the final stage data of shift register with synchronized falling edge of CLOCK, not controlled by \overline{OE} .
x	x	\downarrow	x	The data of shift register is transferred to the storage register.
x	x	\downarrow	x	The data of storage register has no change.

(Note 2) The Q0~Q11 output have a Nch open drain FET. The FET is ON when data from shift register is "L", and the FET is OFF when data is "H".

I/O Equivalence Circuits



Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at $T_A=25^\circ\text{C}$ (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θ_{JA} ($^\circ\text{C}/\text{W}$). The temperature of IC inside the package can be estimated by this thermal resistance. Figure 7 shows the model of thermal resistance of the package. Thermal resistance θ_{JA} , ambient temperature T_A , maximum junction temperature T_{Jmax} , and power dissipation P_D can be calculated by the equation below:

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad (^\circ\text{C}/\text{W})$$

Derating curve in Figure 8 indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{JA} . Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition.

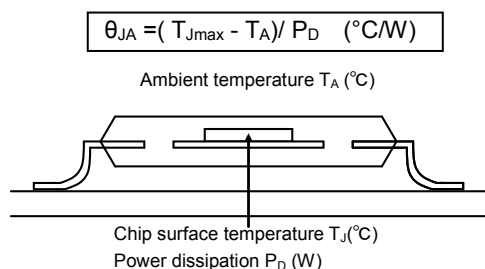


Figure 7. Thermal resistance

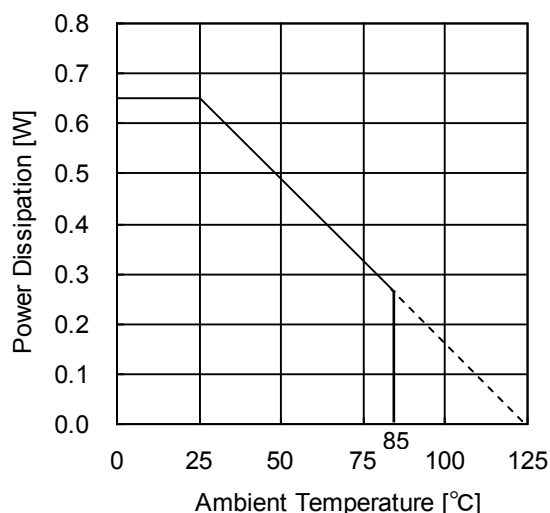


Figure 8. Derating Curve

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

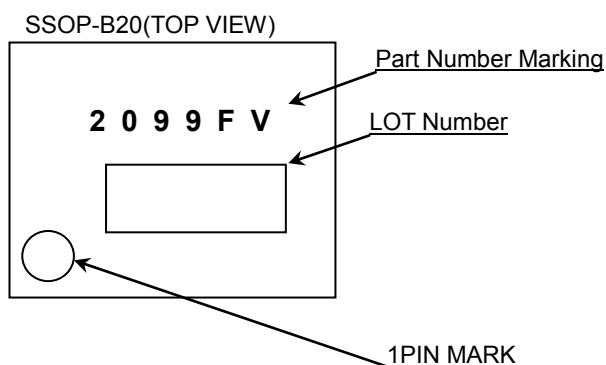
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

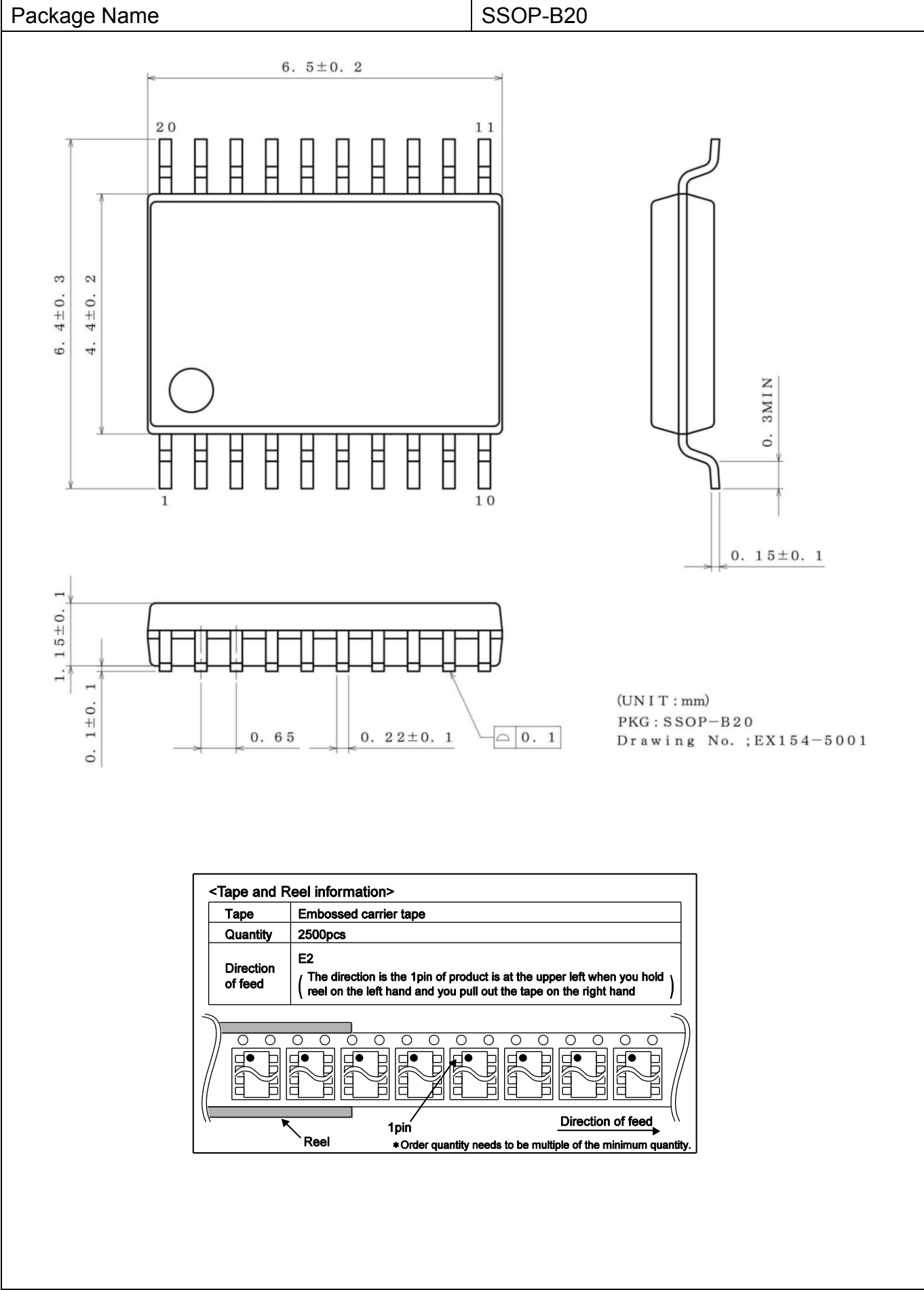
Ordering Information

B U 2 0 9 9 F V	-	E 2
Part Number	Package FV:SSOP-B20	Packaging and forming specification E2: Embossed tape and reel

Marking Diagrams



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
26.Dec.2013	001	New Release
18.Sep.2015	002	Page.1 Block Diagrams : Add SO signal.

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BU2099FV - Web Page

[Distribution Inventory](#)

Part Number	BU2099FV
Package	SSOP-B20
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes