Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A "full pack" plastic package intended for use in circuits where high static and dynamic dV/dt and high dl/dt can occur. This "series C" triac will commutate the full rated RMS current at the maximum rated junction temperature without the aid of a snubber.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High voltage capability
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only

3. Applications

- Electronic thermostats
- High power motor controls e.g. washing machines and vacuum cleaners
- · Rectifier-fed DC inductive loads e.g. DC motors and solenoids
- Refrigeration and air conditioning compressors

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage		-	-	800	V
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 20 \text{ ms}$; Fig. 4; Fig. 5	-	-	140	Α
I _{T(RMS)}	RMS on-state current	full sine wave; $T_h \le 45$ °C; Fig. 1; Fig. 2; Fig. 3	-	-	16	Α
Static characte	eristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	2	-	35	mA





Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + \text{ G-;}$ $T_j = 25 \text{ °C; } \frac{\text{Fig. 7}}{\text{C}}$	2	-	35	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- \text{G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	2	-	35	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	mb	T2—T1
2	T2	main terminal 2		G sym051
3	G	gate		·
mb	n.c.	mounting base; isolated		
			TO-220F (SOT186A)	

6. Ordering information

Table 3. Ordering information

Type number	Package							
	Name	Description	Version					
BTA316X-800C	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A					
BTA316X-800C/L01	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A					

7. Marking

Table 4. Marking codes

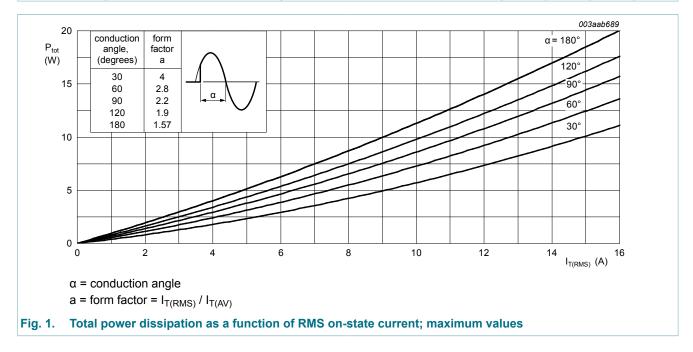
Type number	Marking code
BTA316X-800C	BTA316X-800C
BTA316X-800C/L01	

8. Limiting values

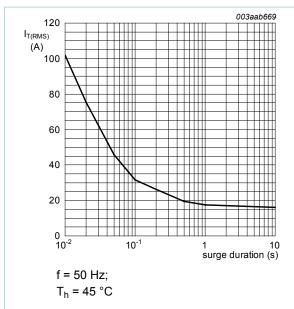
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_h \le 45$ °C; Fig. 1; Fig. 2; Fig. 3	-	16	А
I _{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 20 \text{ ms}$; $Fig. 4$; $Fig. 5$	-	140	А
		full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 16.7 \text{ ms}$	-	150	А
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	98	A ² s
dI _T /dt	rate of rise of on-state current	$I_T = 20 \text{ A}; I_G = 0.2 \text{ A}; dI_G/dt = 0.2 \text{ A/}\mu\text{s}$	-	100	A/µs
I _{GM}	peak gate current		-	2	Α
P _{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	125	°C



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20 003aab667 I_{T(RMS)} (A) 16 12 8 4 4 0 0 50 100 T_h (°C) 150

Fig. 3. RMS on-state current as a function of heatsink temperature; maximum values

Fig. 2. RMS on-state current as a function of surge duration; maximum values

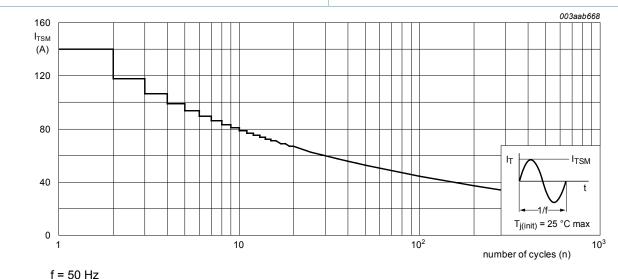
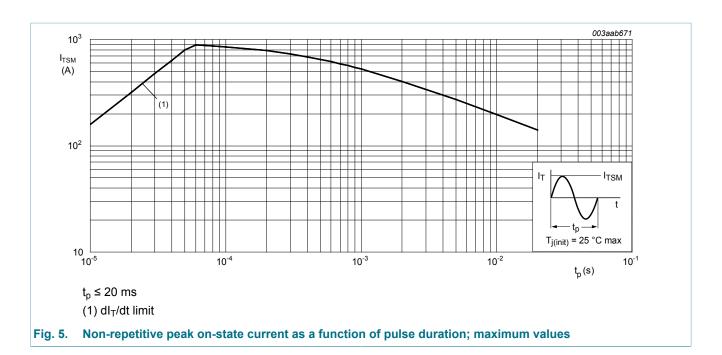


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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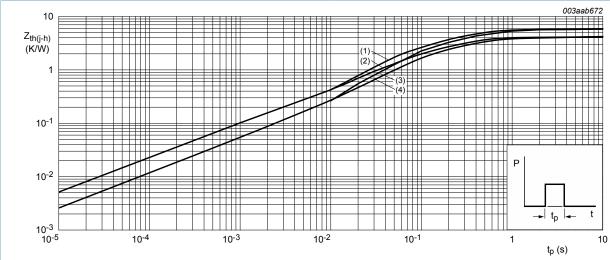


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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-h)} thermal resistance from junction to heatsink		full cycle or half cycle; with heatsink compound; Fig. 6	-	-	4	K/W
		full cycle or half cycle; without heatsink compound; Fig. 6	-	-	5.5	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	-	55	-	K/W



- (1) Unidirectional (half cycle) without heatsink compound
- (2) Unidirectional (half cycle) with heatsink compound
- (3) Bidirectional (full cycle) without heatsink compound
- (4) Bidirectional (full cycle) with heatsink compound

Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

10. Isolation characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{isol(RMS)}	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz \leq f \leq 60 Hz; RH \leq 65 %; T _h = 25 °C	-	-	2500	V
C _{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T _h = 25 °C	-	10	-	pF

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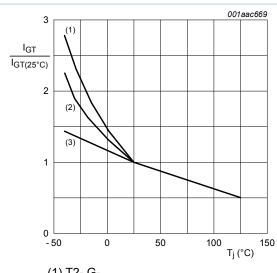
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11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	2	-	35	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2+ \text{ G-;}$ $T_j = 25 \text{ °C; } \underline{\text{Fig. 7}}$	2	-	35	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; T2- G-;}$ $T_j = 25 \text{ °C; } Fig. 7$	2	-	35	mA
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	50	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	60	mA
		$V_D = 12 \text{ V; } I_G = 0.1 \text{ A; T2- G-;}$ $T_j = 25 \text{ °C; } \underline{\text{Fig. 8}}$	-	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	35	mA
V _T	on-state voltage	I _T = 18 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.5	V
V_{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	0.8	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.25	0.4	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic cl	naracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 535 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/ μ s; (snubberless condition); gate open circuit	-	A/ms		

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- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

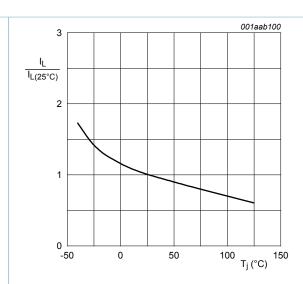


Fig. 8. Normalized latching current as a function of junction temperature

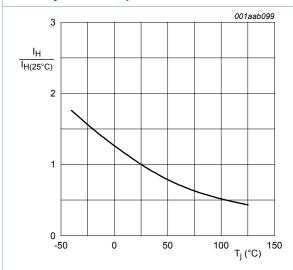
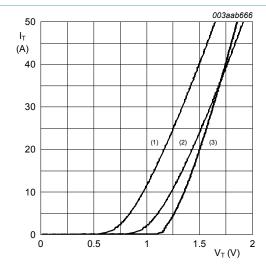


Fig. 9. Normalized holding current as a function of junction temperature



 V_o = 1.024 V; R_s = 0.021 Ω

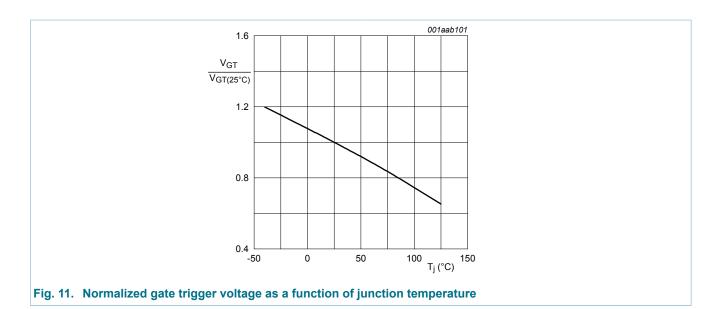
(1) T_i = 125 °C; typical values

(2) T_i = 125 °C; maximum values

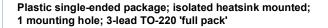
(3) T_i = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

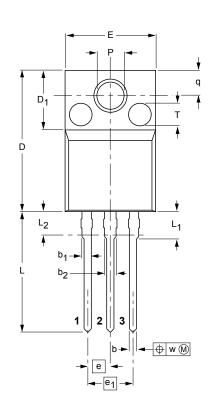
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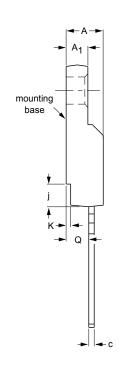


12. Package outline



SOT186A





0 5 10 mm

DIMENSIONS (mm are the original dimensions)

UN	ГА	A	I	b	b ₁	b ₂	С	D	D ₁	E	е	e ₁	j	к	L	L ₁	L ₂ ⁽¹⁾ max.	Р	Q	q	T ⁽²⁾	w
mn	4.6 4.0	2.9 2.5	0).9).7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

- 1. Terminal dimensions within this zone are uncontrolled.
- 2. Both recesses are # 2.5×0.8 max. depth

OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT186A		3-lead TO-220F				-02-04-09 06-02-14

Fig. 12. Package outline TO-220F (SOT186A)

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