

## 1. General description

Planar passivated four quadrant triac in a SOT404 (DPAK) surface-mountable plastic package intended for use in bidirectional switching and phase control applications.

## 2. Features and benefits

- High blocking voltage capability
- Less sensitive gate for improved noise immunity
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants

## 3. Applications

- General purpose motor control
- General purpose switching

## 4. Quick reference data

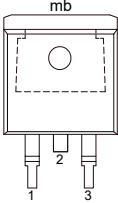

Table 1. Quick reference data

| Symbol                        | Parameter                            | Conditions  | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|---|-----|-----|-----|------|
| $V_{\text{DRM}}$              | repetitive peak off-state voltage    |   | -   | -   | 800 | V    |
| $I_{\text{T(RMS)}}$           | RMS on-state current                 | full sine wave; $T_{\text{mb}} \leq 102\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>         | -   | -   | 8   | A    |
| $I_{\text{TSM}}$              | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | -   | 65  | A    |
|                               |                                      | full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 16.7\text{ ms}$   | -   | -   | 71  | A    |
| $T_{\text{j}}$                | junction temperature                 |   | -   | -   | 125 | °C   |
| <b>Static characteristics</b> |                                      |   |     |     |     |      |
| $I_{\text{GT}}$               | gate trigger current                 | $V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2+ G+; $T_{\text{j}} = 25\text{ °C}$ ; <a href="#">Fig. 7</a>         | -   | 5   | 35  | mA   |
|                               |                                      | $V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2+ G-; $T_{\text{j}} = 25\text{ °C}$ ; <a href="#">Fig. 7</a>         | -   | 8   | 35  | mA   |
|                               |                                      | $V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2- G-; $T_{\text{j}} = 25\text{ °C}$ ; <a href="#">Fig. 7</a>         | -   | 11  | 35  | mA   |
|                               |                                      | $V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2- G+; $T_{\text{j}} = 25\text{ °C}$ ; <a href="#">Fig. 7</a>         | -   | 30  | 70  | mA   |

| Symbol                         | Parameter                             | Conditions  |  | Min | Typ | Max  | Unit             |
|--------------------------------|---------------------------------------|---|--|-----|-----|------|------------------|
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 9</a>   |  | -   | 5   | 20   | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 10\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 10</a>  |  | -   | 1.3 | 1.65 | V                |
| <b>Dynamic characteristics</b> |                                       |   |  |     |     |      |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit |  | 100 | 250 | -    | V/ $\mu\text{s}$ |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 95\text{ }^{\circ}\text{C}$ ; $dI_{com}/dt = 3.6\text{ A/ms}$ ; $I_T = 8\text{ A}$ ; gate open circuit      |  | -   | 20  | -    | V/ $\mu\text{s}$ |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                    | Simplified outline  | Graphic symbol  |
|-----|--------|--------------------------------|---|---|
| 1   | T1     | main terminal 1                |  <p><b>D2PAK (SOT404)</b></p> |  <p>sym051</p> |
| 2   | T2     | main terminal 2                |   |   |
| 3   | G      | gate                           |   |   |
| mb  | T2     | mounting base; main terminal 2 |   |   |

6. Ordering information

Table 3. Ordering information

| Type number | Package |  |         |
|-------------|---------|--|---------|
|             | Name    | Description  | Version |
| BT137B-800  | D2PAK   | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404  |

7. Limiting values

Table 4. Limiting values  
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol       | Parameter                            | Conditions   | Min | Max | Unit                   |
|--------------|--------------------------------------|--|-----|-----|------------------------|
| $V_{DRM}$    | repetitive peak off-state voltage    |  | -   | 800 | V                      |
| $I_{T(RMS)}$ | RMS on-state current                 | full sine wave; $T_{mb} \leq 102\text{ }^{\circ}\text{C}$ ; Fig. 1; Fig. 2; Fig. 3                 | -   | 8   | A                      |
| $I_{TSM}$    | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; Fig. 4; Fig. 5 | -   | 65  | A                      |
|              |                                      | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$                | -   | 71  | A                      |
| $I^2t$       | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; SIN   | -   | 21  | $\text{A}^2\text{s}$   |
| $di_T/dt$    | rate of rise of on-state current     | $I_G = 150\text{ mA}$  | -   | 50  | $\text{A}/\mu\text{s}$ |
| $I_{GM}$     | peak gate current                    |  | -   | 2   | A                      |
| $P_{GM}$     | peak gate power                      |  | -   | 5   | W                      |
| $P_{G(AV)}$  | average gate power                   | over any 20 ms period  | -   | 0.5 | W                      |
| $T_{stg}$    | storage temperature                  |  | -40 | 150 | $^{\circ}\text{C}$     |
| $T_j$        | junction temperature                 |  | -   | 125 | $^{\circ}\text{C}$     |

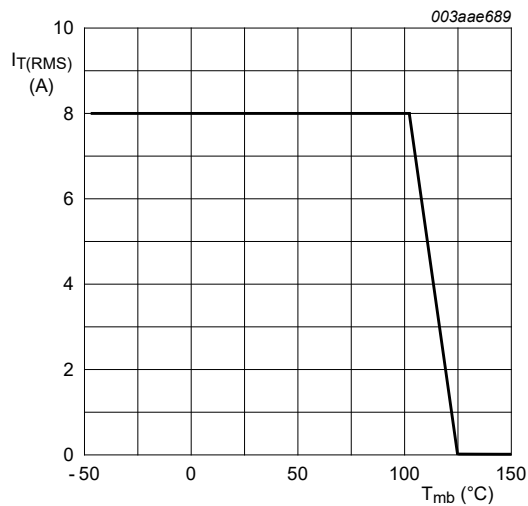


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

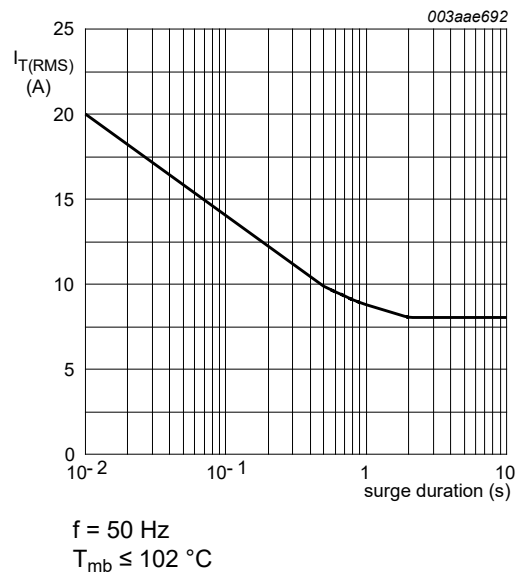
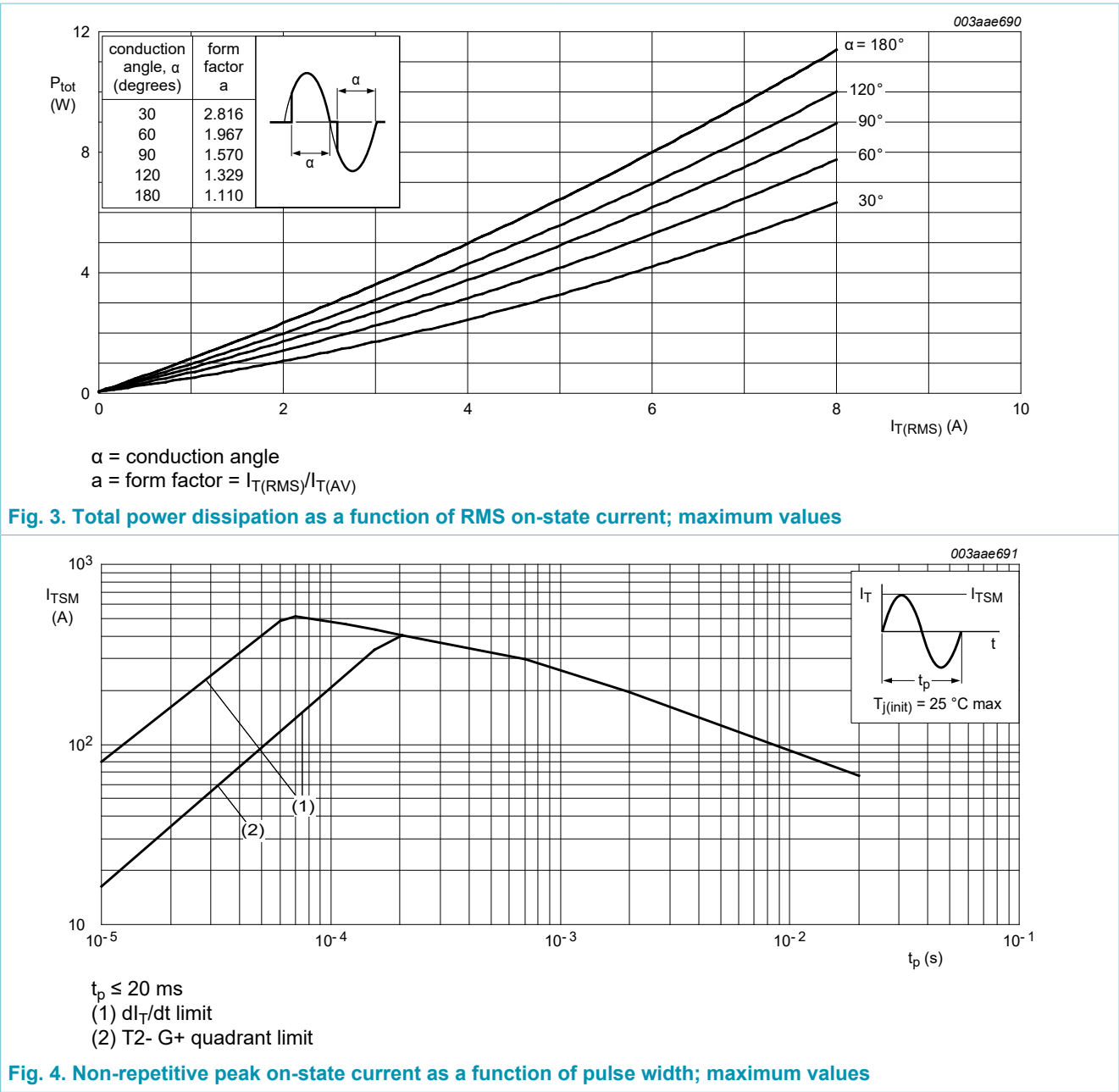
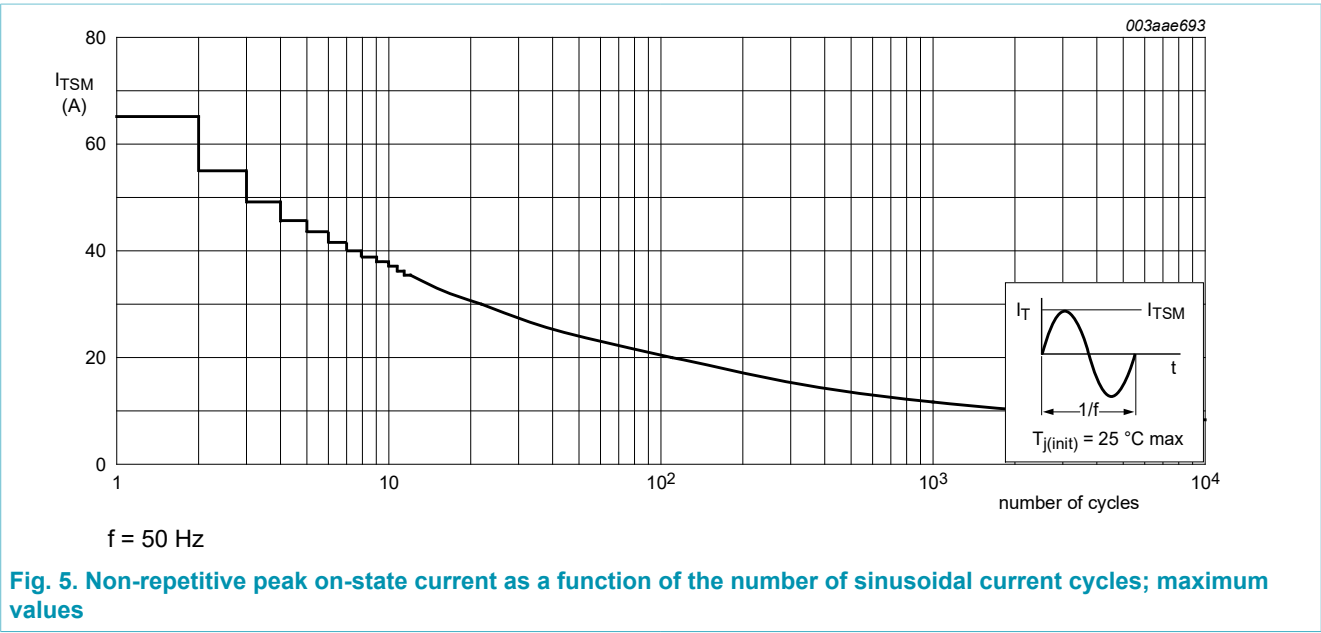


Fig. 2. RMS on-state current as a function of surge duration; maximum values





8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol                | Parameter  | Conditions                           |  | Min | Typ | Max | Unit |
|-----------------------|--|--------------------------------------|--|-----|-----|-----|------|
| R <sub>th(j-mb)</sub> | thermal resistance from junction to mounting base    | half cycle; Fig. 6                   |  | -   | -   | 2.4 | K/W  |
|                       |  | full cycle; Fig. 6                   |  | -   | -   | 2   | K/W  |
| R <sub>th(j-a)</sub>  | thermal resistance from junction to ambient free air | PCB (FR4) mounted; minimum pad sizes |  | -   | 55  | -   | K/W  |

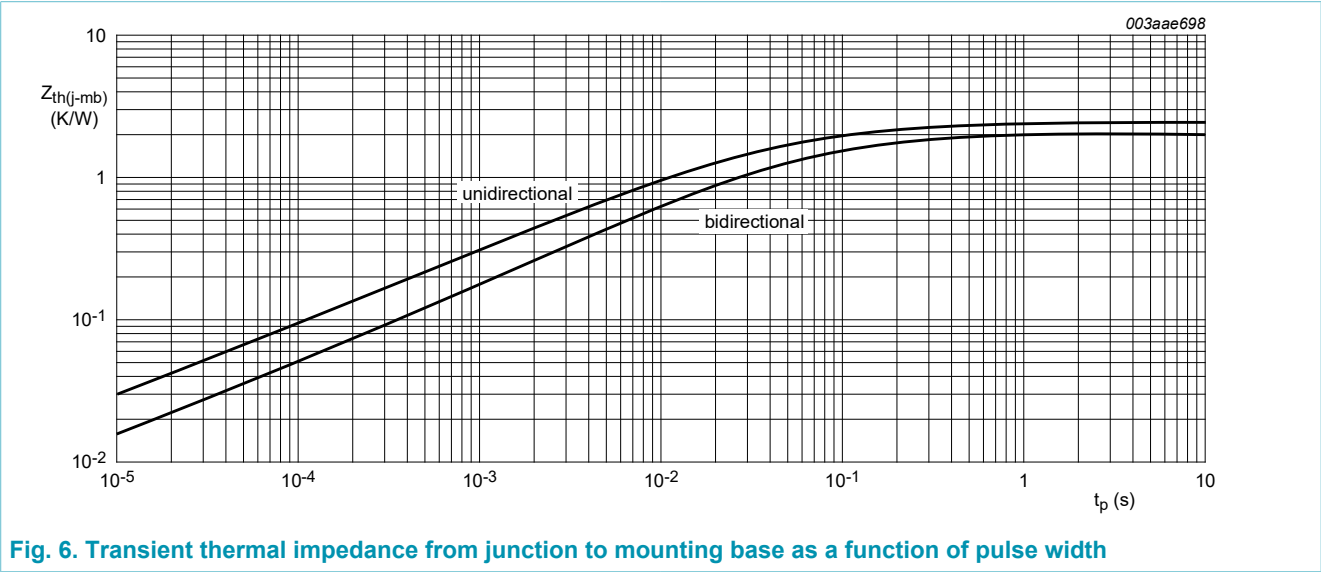
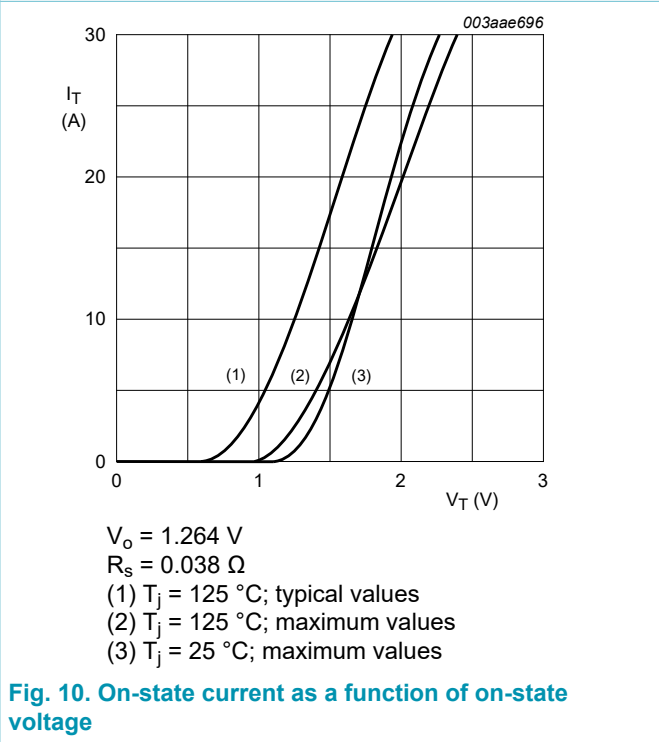
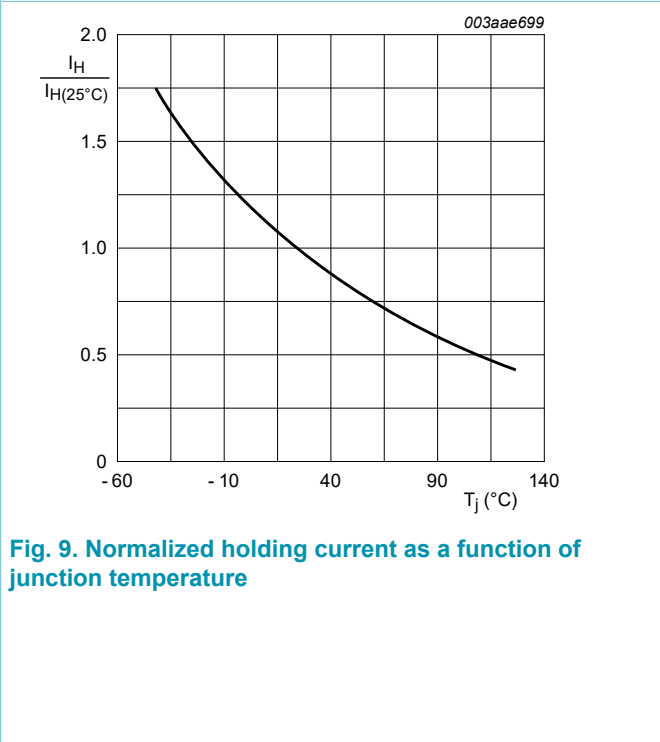
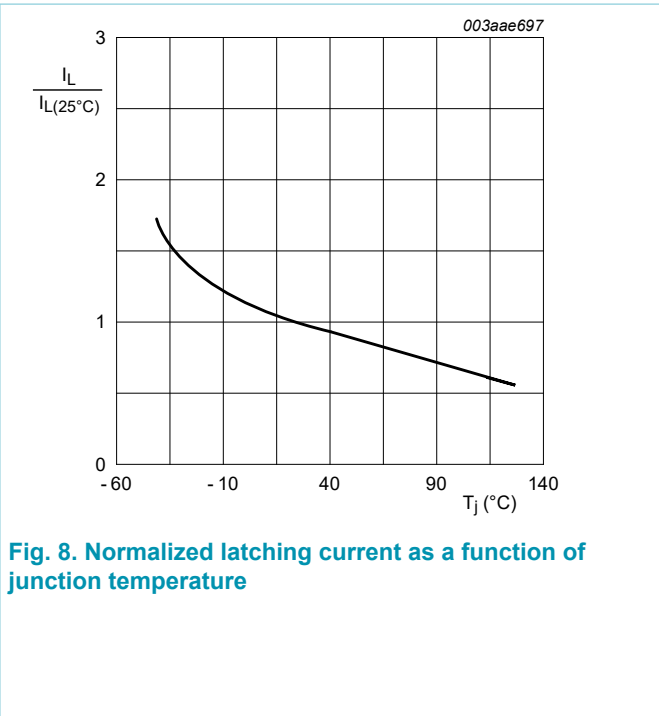
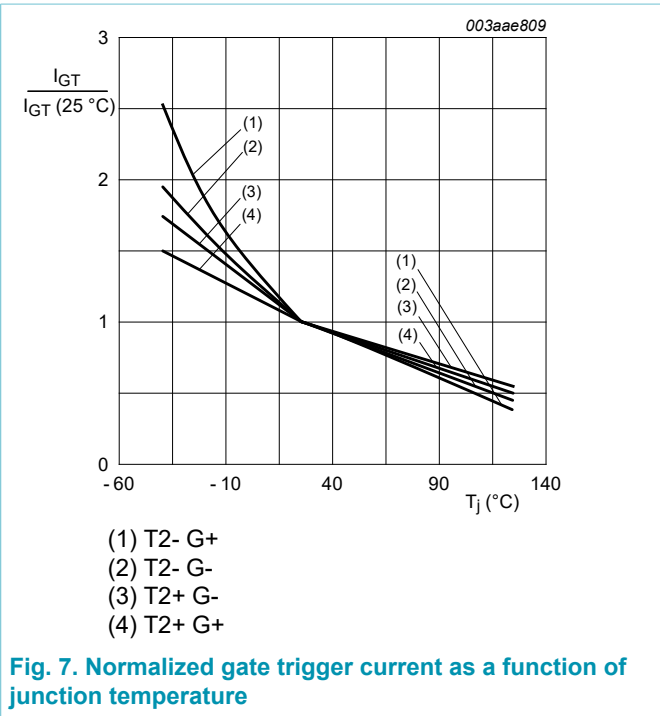


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

## 9. Characteristics

Table 6. Characteristics

| Symbol                         | Parameter                             | Conditions  |  | Min  | Typ | Max  | Unit             |
|--------------------------------|---------------------------------------|---|--|------|-----|------|------------------|
| <b>Static characteristics</b>  |                                       |   |  |      |     |      |                  |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 5   | 35   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 8   | 35   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 11  | 35   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>                       |  | -    | 30  | 70   | mA               |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 7   | 30   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 16  | 45   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 5   | 30   | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+;<br>$T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>                       |  | -    | 7   | 45   | mA               |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>   |  | -    | 5   | 20   | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 10\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>  |  | -    | 1.3 | 1.65 | V                |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                              |  | -    | 0.7 | 1    | V                |
|                                |                                       | $V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ;<br><a href="#">Fig. 11</a>                            |  | 0.25 | 0.4 | -    | V                |
| $I_D$                          | off-state current                     | $V_D = 800\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$  |  | -    | 0.1 | 0.5  | mA               |
| <b>Dynamic characteristics</b> |                                       |   |  |      |     |      |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit |  | 100  | 250 | -    | V/ $\mu\text{s}$ |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 95\text{ }^\circ\text{C}$ ; $dI_{com}/dt = 3.6\text{ A/ms}$ ; $I_T = 8\text{ A}$ ; gate open circuit      |  | -    | 20  | -    | V/ $\mu\text{s}$ |





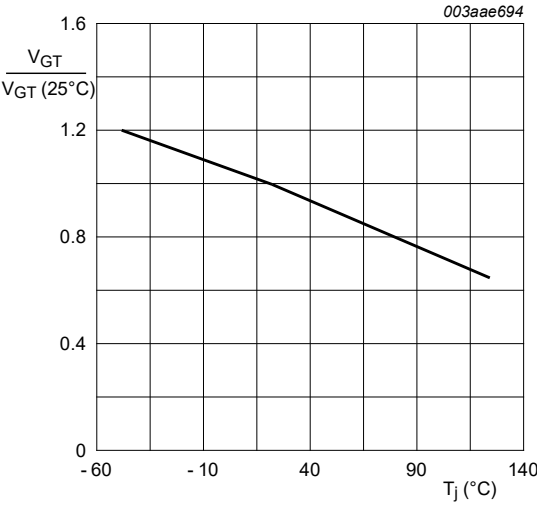
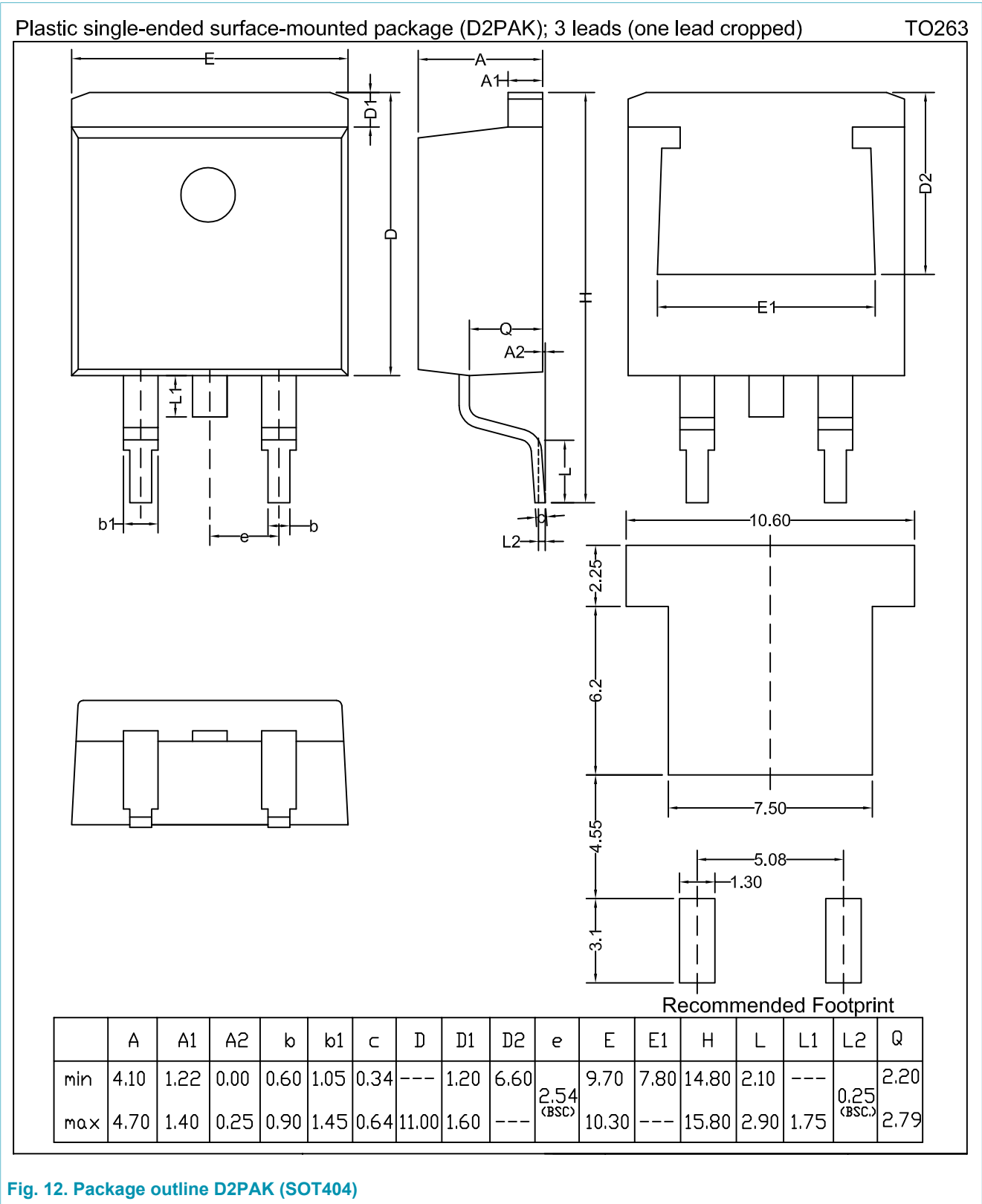


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

10. Package outline



## 11. Legal information

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| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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- [1] Please consult the most recently issued document before initiating or completing a design.
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## 12. Contents

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|                                 |    |
|---------------------------------|----|
| 1. General description.....     | 1  |
| 2. Features and benefits.....   | 1  |
| 3. Applications.....            | 1  |
| 4. Quick reference data.....    | 1  |
| 5. Pinning information.....     | 2  |
| 6. Ordering information.....    | 2  |
| 7. Limiting values.....         | 3  |
| 8. Thermal characteristics..... | 6  |
| 9. Characteristics.....         | 7  |
| 10. Package outline.....        | 10 |
| 11. Legal information.....      | 11 |

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