Freescale Semiconductor
Data Sheet: Technical Data

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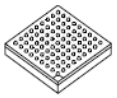
BSC9131

BSC9131 QorIQ Qonverge Multicore Baseband Processor



FC-PBGA–520
21 mm x 21 mm

The following list provides an overview of the feature set:

- High-performance 32-bit e500 core built on Power Architecture® technology:
  - 36-bit physical addressing
  - Double-precision floating-point support
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache
  - Enhanced hardware and software debug support
  - 800 MHz/1 GHz clock frequency
  - 256-Kbyte L2 cache with ECC; also configurable as SRAM and stashing memory
- One SC3850 core subsystem, which connects to the following:
  - 32 Kbyte 8-way level 1 data/instruction cache (L1 Dcache/ICache)
  - 512 Kbyte 8-way level 2 unified instruction/data cache (L2 cache/M2 memory)
  - Memory management unit (MMU)
  - Enhanced programmable interrupt controller (EPIC)
  - Debug and profiling unit (DPU)
  - Two 32-bit quad timers
- Multi Accelerator Platform Engine for Femto Base Station Baseband Processing (MAPLE-B2F)
  - Supports variable sizes in Fourier Transforms, Convolution, Filtering, Turbo, Viterbi, Chiprate
  - Consists of accelerators for UMTS chip rate processing, LTE UP/DL channel processing, Matrix Inversion operations, and CRC algorithms
- DDR3/DDR3L SDRAM memory controller supports 32-bit without ECC and 16-bit with ECC
- Integrated security engine (ULE CAAM)
  - Protocol support includes DES, AES, RNG, CRC, MDE, PKE, SHA, and MD5
- Secure boot capability
- Two enhanced three-speed Ethernet controllers (eTSECs)
  - 10/100/1000 Mbps support
  - TCP/IP acceleration, quality of service, and classification capabilities
  - IEEE Std 1588™ support
  - eTSEC1 supports RGMII and RMII interfaces
  - eTSEC2 supports an RGMII interface
- High-speed USB controller (USB 2.0)
  - Host and device support
  - Enhanced host controller interface (EHCI)
  - ULPI interface
- Enhanced secure digital (SD/MMC) host controller (eSDHC)
- Integrated Flash controller (IFC), supporting NAND, NOR, and general ASIC
- TDM with one TDM port
- Antenna interface controller (AIC), supporting three industry standard JESD/three custom parallel RF interfaces (two dual and one single port) and three MAXIM's MaxPHY serial interfaces
- Universal Subscriber Identity Module (USIM) interface
  - Facilitates communication to SIM cards or Eurochip pre-paid phone cards
- Four enhanced serial peripheral interfaces (eSPI)
- Programmable interrupt controller (PIC) compliant with OpenPIC standard
- One four-channel DMA controller
- Two I^2C interfaces
- Two dual UART (DUART) interfaces
- Two pulse-width modulator (PWM) interfaces
- 96 general-purpose I/O signals
- Eight 32-bit timers
- Operating temperature (Ta - T_j) range: 0–105° C

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This figure shows the major functional units.

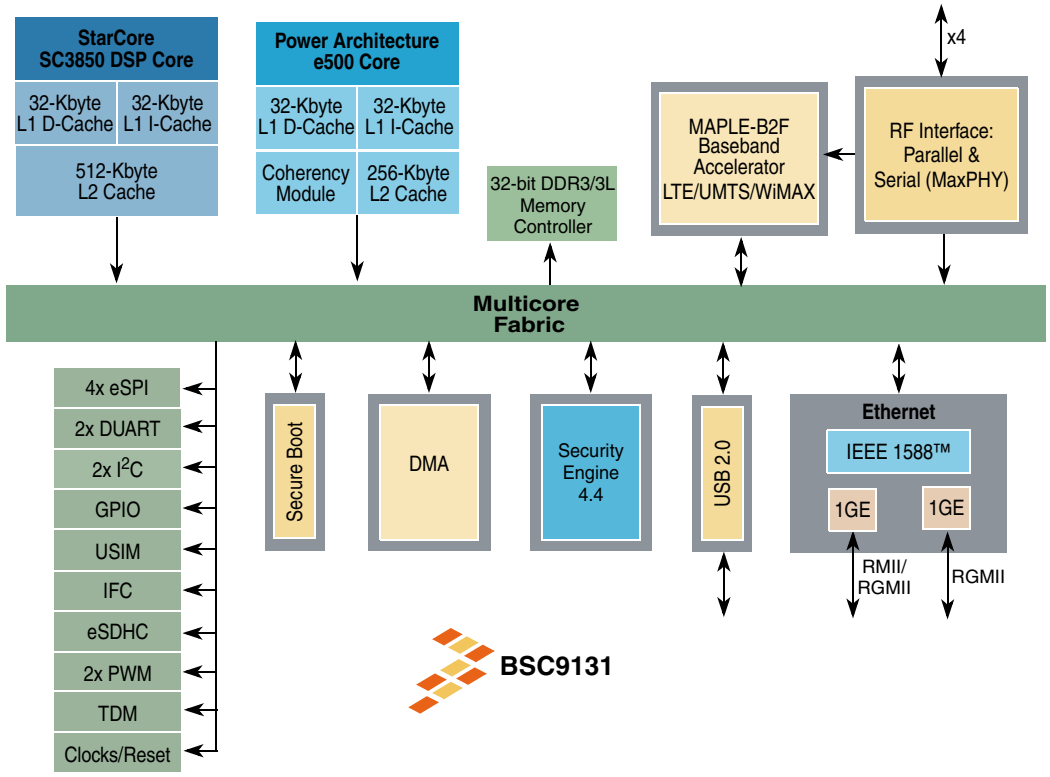


Figure 1. BSC9131 Block Diagram

1 Pin Assignments

This section contains a top-level ball layout diagram followed by four detailed quadrant views and a pinout listing table.

1.1 Ball Layout Diagrams

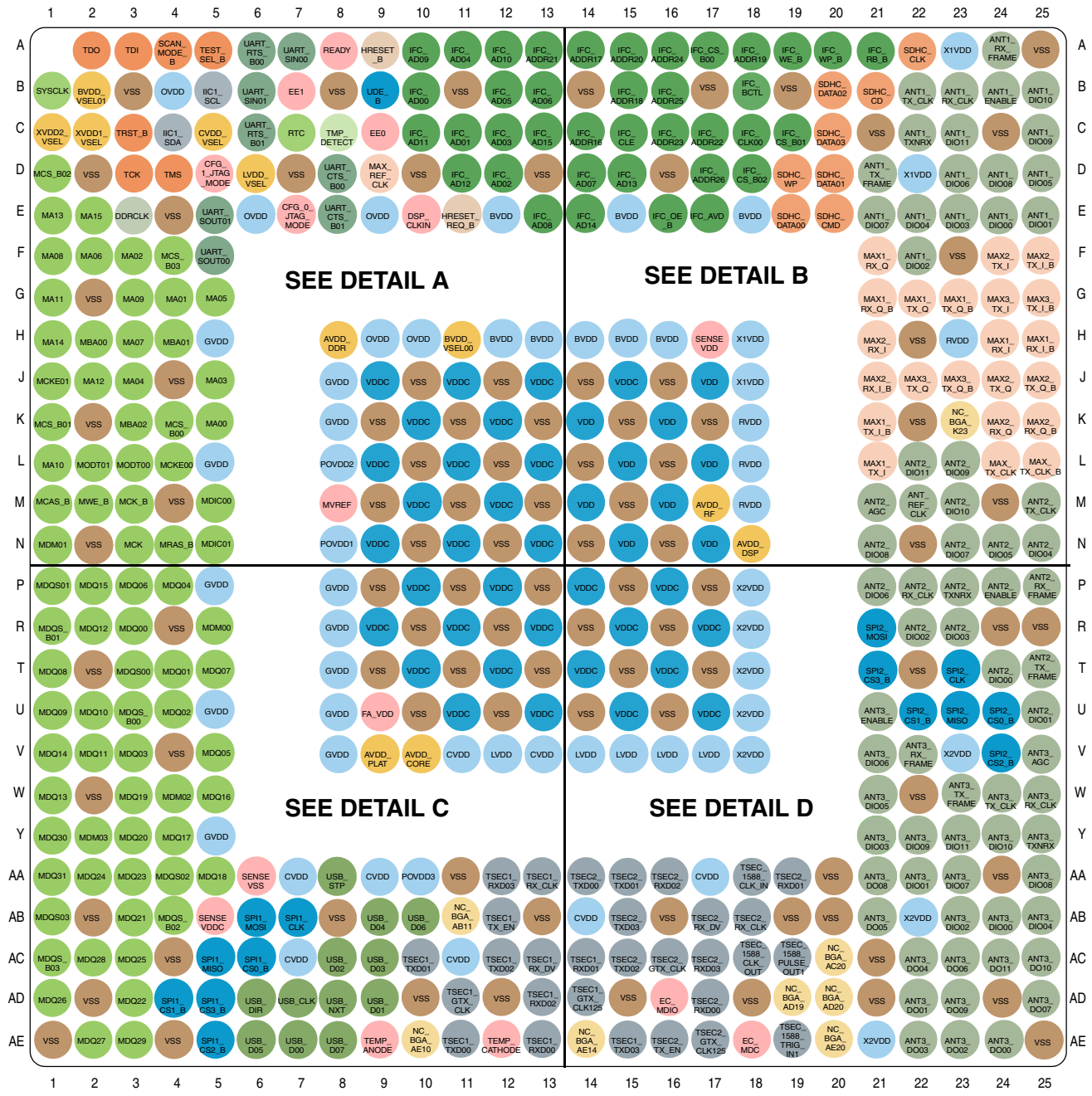


Figure 2. Ball Layout Diagram—Top-Level View

Figure 3 shows detailed view A.

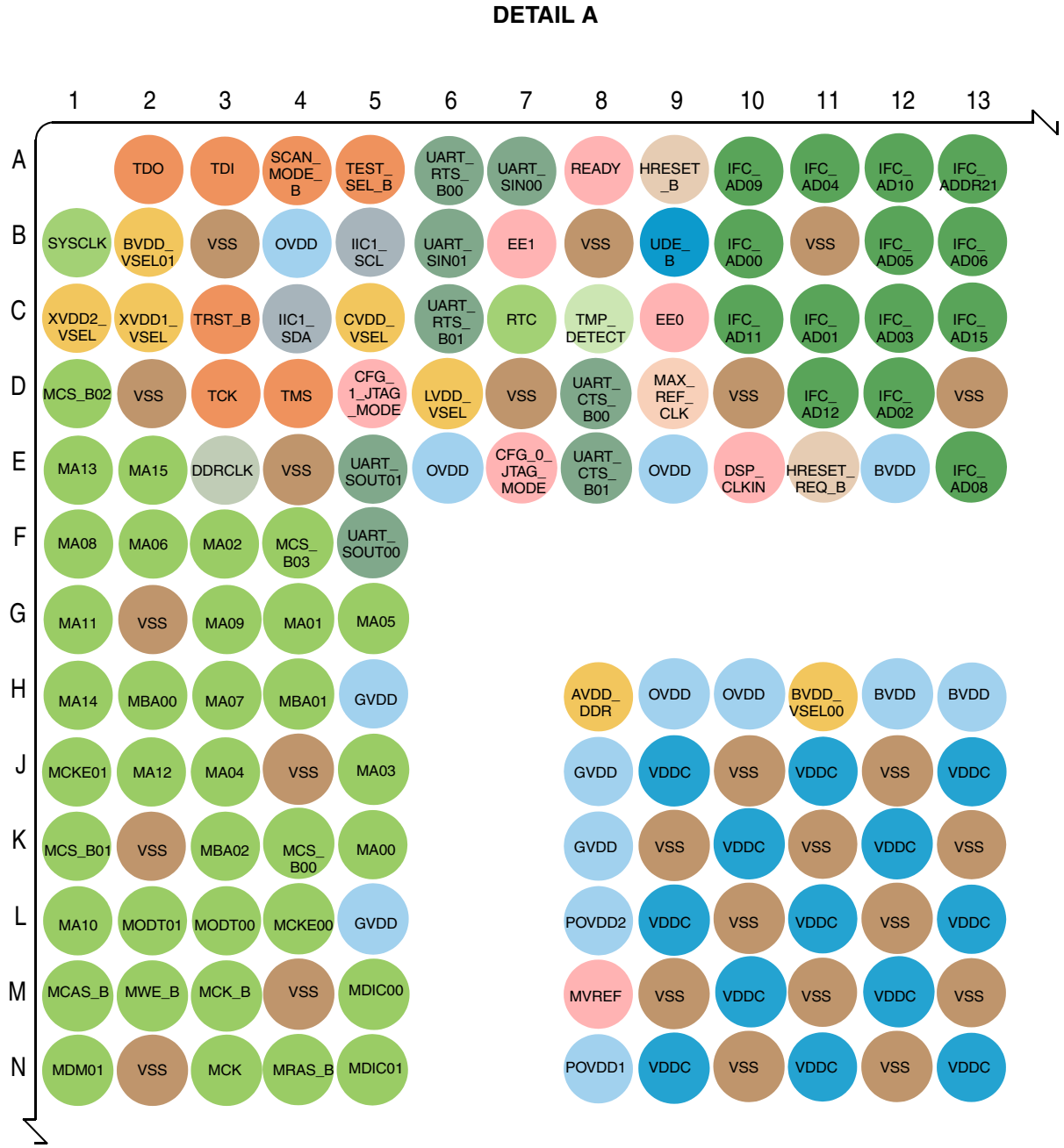


Figure 3. Ball Layout Diagram—Detail A

Figure 4 shows detailed view B.

Figure 4. Ball Layout Diagram—Detail B

Figure 5 shows detailed view C.

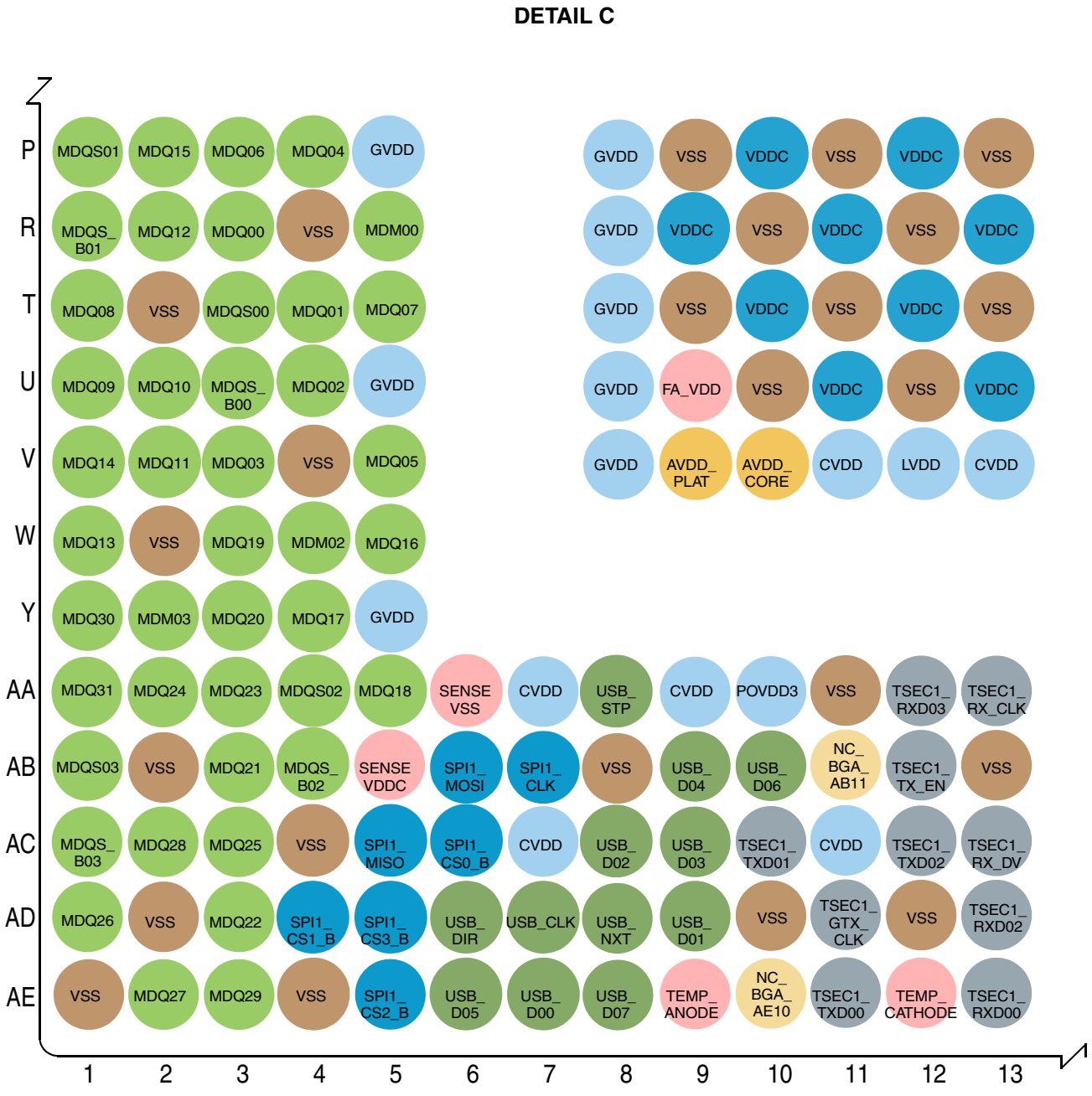


Figure 5. Ball Layout Diagram—Detail C

Figure 6 shows detailed view D.

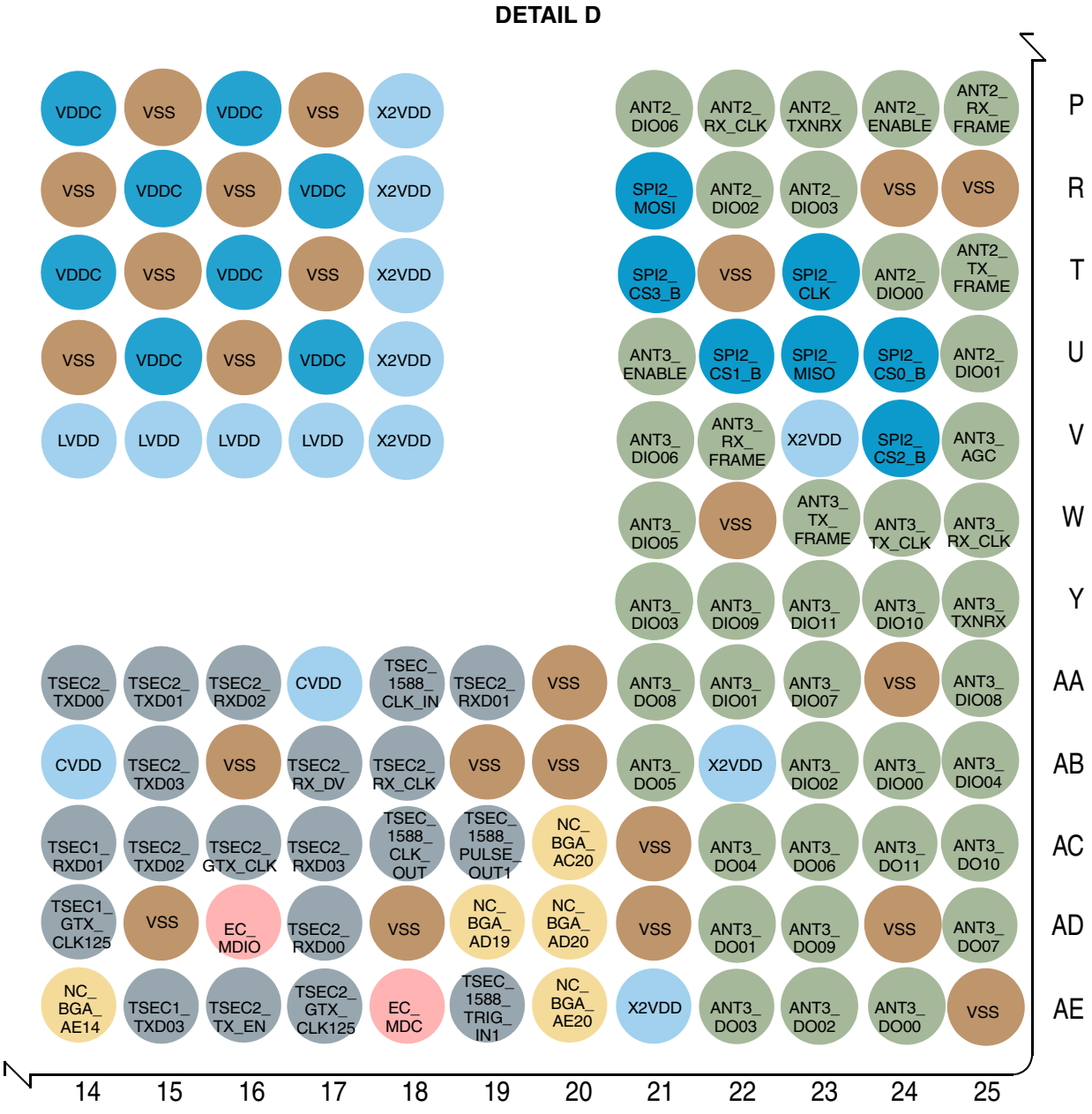


Figure 6. Ball Layout Diagram—Detail D

1.2 Pinout Assignments

This table provides the pinout listing.

Table 1. BSC9131 Pinout Listing

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
DDR (Power Architecture)					
MDQ00	Data	R3	I/O	GVDD	—
MDQ01	Data	T4	I/O	GVDD	—
MDQ02	Data	U4	I/O	GVDD	—
MDQ03	Data	V3	I/O	GVDD	—
MDQ04	Data	P4	I/O	GVDD	—
MDQ05	Data	V5	I/O	GVDD	—
MDQ06	Data	P3	I/O	GVDD	—
MDQ07	Data	T5	I/O	GVDD	—
MDQ08	Data	T1	I/O	GVDD	—
MDQ09	Data	U1	I/O	GVDD	—
MDQ10	Data	U2	I/O	GVDD	—
MDQ11	Data	V2	I/O	GVDD	—
MDQ12	Data	R2	I/O	GVDD	—
MDQ13	Data	W1	I/O	GVDD	—
MDQ14	Data	V1	I/O	GVDD	—
MDQ15	Data	P2	I/O	GVDD	—
MDQ16	Data	W5	I/O	GVDD	—
MDQ17	Data	Y4	I/O	GVDD	—
MDQ18	Data	AA5	I/O	GVDD	—
MDQ19	Data	W3	I/O	GVDD	—
MDQ20	Data	Y3	I/O	GVDD	—
MDQ21	Data	AB3	I/O	GVDD	—
MDQ22	Data	AD3	I/O	GVDD	—
MDQ23	Data	AA3	I/O	GVDD	—
MDQ24	Data	AA2	I/O	GVDD	—
MDQ25	Data	AC3	I/O	GVDD	—
MDQ26	Data	AD1	I/O	GVDD	—
MDQ27	Data	AE2	I/O	GVDD	—
MDQ28	Data	AC2	I/O	GVDD	—
MDQ29	Data	AE3	I/O	GVDD	—
MDQ30	Data	Y1	I/O	GVDD	—
MDQ31	Data	AA1	I/O	GVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
MDM00	Data Mask	R5	O	GVDD	—
MDM01	Data Mask	N1	O	GVDD	—
MDM02	Data Mask	W4	O	GVDD	—
MDM03	Data Mask	Y2	O	GVDD	—
MDQS00	Data Strobe	T3	I/O	GVDD	—
MDQS01	Data Strobe	P1	I/O	GVDD	—
MDQS02	Data Strobe	AA4	I/O	GVDD	—
MDQS03	Data Strobe	AB1	I/O	GVDD	—
MDQS_B00	Data Strobe	U3	I/O	GVDD	—
MDQS_B01	Data Strobe	R1	I/O	GVDD	—
MDQS_B02	Data Strobe	AB4	I/O	GVDD	—
MDQS_B03	Data Strobe	AC1	I/O	GVDD	—
MBA00	Bank Select	H2	O	GVDD	—
MBA01	Bank Select	H4	O	GVDD	—
MBA02	Bank Select	K3	O	GVDD	—
MA00	Address	K5	O	GVDD	—
MA01	Address	G4	O	GVDD	—
MA02	Address	F3	O	GVDD	—
MA03	Address	J5	O	GVDD	—
MA04	Address	J3	O	GVDD	—
MA05	Address	G5	O	GVDD	—
MA06	Address	F2	O	GVDD	—
MA07	Address	H3	O	GVDD	—
MA08	Address	F1	O	GVDD	—
MA09	Address	G3	O	GVDD	—
MA10	Address	L1	O	GVDD	—
MA11	Address	G1	O	GVDD	—
MA12	Address	J2	O	GVDD	—
MA13	Address	E1	O	GVDD	—
MA14	Address	H1	O	GVDD	—
MA15	Address	E2	O	GVDD	—
MWE_B	Write Enable	M2	O	GVDD	—
MRAS_B	Row Address Strobe	N4	O	GVDD	—
MCAS_B	Column Address Strobe	M1	O	GVDD	—
MCS_B00	Chip Select	K4	O	GVDD	—
MCS_B01	Chip Select	K1	O	GVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
MCS_B02	Chip Select	D1	O	GVDD	—
MCS_B03	Chip Select	F4	O	GVDD	—
MCKE00	Clock Enable	L4	O	GVDD	—
MCKE01	Clock Enable	J1	O	GVDD	—
MCK	Clock	N3	O	GVDD	—
MCK_B	Clock Complements	M3	O	GVDD	—
MODT00	On Die Termination	L3	O	GVDD	—
MODT01	On Die Termination	L2	O	GVDD	—
MDIC00	Driver Impedence Calibration	M5	I/O	VSS	17
MDIC01	Driver Impedence Calibration	N5	I/O	GVDD	17
Ethernet Management					
EC_MDC	Management Data Clock	AE18	O	LVDD	2
EC_MDIO	Management Data In/Out	AD16	I/O	LVDD	18
eTSEC 1 (RGMII)					
TSEC1_TXD00	RGMII Transmit Data	AE11	O	LVDD	2
TSEC1_TXD01	RGMII Transmit Data	AC10	O	LVDD	2
TSEC1_TXD02	RGMII Transmit Data	AC12	O	LVDD	2
TSEC1_TXD03	RGMII Transmit Data	AE15	O	LVDD	2
TSEC1_TX_EN	RGMII Transmit Enable	AB12	O	LVDD	—
TSEC1_RXD00	RGMII Receive Data	AE13	I	LVDD	—
TSEC1_RXD01	RGMII Receive Data	AC14	I	LVDD	—
TSEC1_RXD02	RGMII Receive Data	AD13	I	LVDD	—
TSEC1_RXD03/ TSEC1_RX_ER	RGMII Receive Data	AA12	I	LVDD	—
TSEC1_RX_DV	RGMII Receive Data Valid	AC13	I	LVDD	—
TSEC1_RX_CLK	RGMII Receive Clock	AA13	I	LVDD	—
TSEC1_GTX_CLK	RGMII Transmit Clock Out	AD11	O	LVDD	—
TSEC1_GTX_CLK125/ TSEC1_TX_CLK	RGMII Reference Clock	AD14	I	LVDD	—
eTSEC 1 (RMII)					
TSEC1_TXD00	RMII Transmit Data	AE11	O	LVDD	2
TSEC1_TXD01	RMII Transmit Data	AC10	O	LVDD	2
TSEC1_TX_EN	RMII Transmit Data Valid	AB12	O	LVDD	—
TSEC1_RXD00	RMII Receive Data	AE13	I	LVDD	—
TSEC1_RXD01	RMII Receive Data	AC14	I	LVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
TSEC1_RXD03/ **TSEC1_RX_ER**	RMII Receive Error	AA12	I	LVDD	—
TSEC1_RX_DV	RMII CRS_DV carrier sense/Data Valid	AC13	I	LVDD	—
TSEC1_GTX_CLK	RMII Transmit Clock feedback	AD11	O	LVDD	—
TSEC1_GTX_CLK125/ **TSEC1_TX_CLK**	RMII Reference Transmit/Receive Clock	AD14	I	LVDD	—
eTSEC 2 (RGMII)					
TSEC2_TXD00/ DMA_DACK_B00/ USB_NXT	RGMII Transmit Data	AA14	I/O	LVDD	—
TSEC2_TXD01/ DMA_DDONE_B00/ USB_D07	RGMII Transmit Data	AA15	I/O	LVDD	—
TSEC2_TXD02/ GPIO04/ IRQ04/ USB_D06	RGMII Transmit Data	AC15	I/O	LVDD	—
TSEC2_TXD03/ GPIO05/ IRQ05/ USB_D05	RGMII Transmit Data	AB15	I/O	LVDD	—
TSEC2_TX_EN	RGMII Transmit Enable	AE16	O	LVDD	—
TSEC2_RXD00/ DMA_DREQ_B00/ USB_D04	RGMII Receive Data	AD17	I/O	LVDD	—
TSEC2_RXD01/ USB_D03	RGMII Receive Data	AA19	I/O	LVDD	—
TSEC2_RXD02/ USB_D02	RGMII Receive Data	AA16	I/O	LVDD	—
TSEC2_RXD03/ USB_D01	RGMII Receive Data	AC17	I/O	LVDD	—
TSEC2_RX_DV/ USB_D00	RGMII Receive Data Valid	AB17	I/O	LVDD	—
TSEC2_RX_CLK/ GPIO06/ IRQ06/ USB_CLK	RGMII Receive Clock	AB18	I/O	LVDD	—
TSEC2_GTX_CLK/ USB_STP	RGMII Transmit Clock Out	AC16	O	LVDD	—
TSEC2_GTX_CLK125/ GPIO07/ IRQ07/ USB_DIR	RGMII Reference Clock	AE17	I/O	LVDD	—
eTSEC 1588					

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
TSEC_1588_CLK_IN	1588 Clock In	AA18	I	LVDD	—
TSEC_1588_CLK_OUT/ CLK_OUT	1588 Clock Out	AC18	O	LVDD	—
TSEC_1588_TRIG_IN1	1588 Trigger In	AE19	I	LVDD	—
TSEC_1588_PULSE_OUT1/ PPS_OUT	1588 Pulse Out	AC19	O	LVDD	2
IFC					
IFC_AD00	IFC Muxed Address, Data	B10	I/O	BVDD	2
IFC_AD01	IFC Muxed Address, Data	C11	I/O	BVDD	2
IFC_AD02	IFC Muxed Address, Data	D12	I/O	BVDD	2
IFC_AD03	IFC Muxed Address, Data	C12	I/O	BVDD	2
IFC_AD04	IFC Muxed Address, Data	A11	I/O	BVDD	2
IFC_AD05	IFC Muxed Address, Data	B12	I/O	BVDD	2
IFC_AD06	IFC Muxed Address, Data	B13	I/O	BVDD	2
IFC_AD07	IFC Muxed Address, Data	D14	I/O	BVDD	2
IFC_AD08/ GPIO34	IFC Muxed Address, Data	E13	I/O	BVDD	—
IFC_AD09/ GPIO35	IFC Muxed Address, Data	A10	I/O	BVDD	—
IFC_AD10/ GPIO36	IFC Muxed Address, Data	A12	I/O	BVDD	—
IFC_AD11/ GPIO37/ IRQ08	IFC Muxed Address, Data	C10	I/O	BVDD	—
IFC_AD12/ GPIO38/ IRQ09	IFC Muxed Address, Data	D11	I/O	BVDD	—
IFC_AD13/ GPIO39/ IRQ07	IFC Muxed Address, Data	D15	I/O	BVDD	—
IFC_AD14/ GPIO40/ IRQ06	IFC Muxed Address, Data	E14	I/O	BVDD	—
IFC_AD15/ GPIO41/ TIMER02	IFC Muxed Address, Data	C13	I/O	BVDD	—
IFC_ADDR16/ GPO08	IFC Address	C14	O	BVDD	2
IFC_ADDR17/ GPO09	IFC Address	A14	O	BVDD	2
IFC_ADDR18/ GPO10	IFC Address	B15	O	BVDD	2

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_ADDR19/ GPO11	IFC Address	A18	O	BVDD	2
IFC_ADDR20/ GPO12	IFC Address	A15	O	BVDD	2
IFC_ADDR21/ GPO13	IFC Address	A13	O	BVDD	2
IFC_ADDR22/ GPO14	IFC Address	C17	O	BVDD	2
IFC_ADDR23/ GPO15	IFC Address	C16	O	BVDD	2
IFC_ADDR24/ GPO16	IFC Address	A16	O	BVDD	2
IFC_ADDR25/ GPO17	IFC Address	B16	O	BVDD	2
IFC_ADDR26/ GPO18	IFC Address	D17	O	BVDD	2
IFC_AVD	IFC Address Valid	E17	O	BVDD	2
IFC_CS_B00	IFC Chip Select	A17	O	BVDD	18
IFC_CS_B01/ GPO64	IFC Chip Select	C19	O	BVDD	18
IFC_CS_B02/ GPO65	IFC Chip Select	D18	O	BVDD	18
IFC_WE_B	IFC Write Enable/GPCM Write Byte Select0/ Generic ASIC Interface Start of Frame	A19	O	BVDD	2
IFC_CLE	NAND Command Latch Enable/ GPCM Write Byte Select1	C15	O	BVDD	2
IFC_OE_B	NOR Output Enable/NAND Read Enable/ GPCM Output Enable/Generic ASIC Interface Read-Write Indicator	E16	O	BVDD	2
IFC_WP_B/ GPO66/ DSP_TDI	IFC Write Protect	A20	O	BVDD	3
IFC_RB_B	IFC Read Busy/GPCM External Transreciver/ Generic ASIC Interface Ready Indicator	A21	I	BVDD	18
IFC_BCTL/ GPO67/ DSP_TDO	Data Buffer Control	B18	O	BVDD	—
IFC_CLK00/ GPO68	IFC Clock	C18	O	BVDD	—
TDM over ANT3					
ANT3_DO00/ **TDM_TCK**/ GPIO46	TDM Transmit Clock	AE24	I	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT3_DO04/ **TDM_RCK**/ GPIO50/ IRQ00	TDM Receive Clock	AC22	I/O	X2VDD	—
ANT3_DO01/ **TDM_TFS**/ GPIO47	TDM Transmit Frame Sync	AD22	I/O	X2VDD	—
ANT3_DO05/ **TDM_RFS**/ GPIO51/ IRQ01	TDM Receive Frame Sync	AB21	I/O	X2VDD	—
ANT3_DO03/ **TDM_TXD**/ GPIO49	TDM Transmit Data	AE22	I/O	X2VDD	—
ANT3_DO02/ **TDM_RXD**/ GPIO48	TDM Receive Data	AE23	I/O	X2VDD	—
TDM over SDHC					
SDHC_CD/ **TDM_TCK**	TDM Transmit Clock	B21	I	BVDD	—
SDHC_DATA01/ SIM_SVEN/ **TDM_RCK**/ GPIO77	TDM Receive Clock	D20	I/O	BVDD	—
SDHC_WP/ **TDM_TFS**/ TIMER04	TDM Transmit Frame Sync	D19	I/O	BVDD	—
SDHC_DATA00/ SIM_TRXD/ **TDM_RFS**	TDM Receive Frame Sync	E19	I/O	BVDD	—
SDHC_DATA02/ **TDM_TXD**/ GPIO78	TDM Transmit Data	B20	I/O	BVDD	—
SDHC_DATA03/ **TDM_RXD**/ GPIO79/ IRQ10	TDM Receive Data	C20	I/O	BVDD	—
PWM					
UART_RTS_B00/ **PWM2**/ DSP_TCK/ GPO43	PWM1 Block Output	A6	O	OVDD	—
SPI1_CS3_B/ **ANT_TCXO_PWM**/ GPO76	PWM2 Block Output for RF Interface	AD5	O	CVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
Timers					
USB_DIR/ GPIO02/ **TIMER01**/ MCP_B	Timer 1	AD6	I/O	CVDD	—
IFC_AD15/ GPIO41/ **TIMER02**	Timer 2	C13	I/O	BVDD	—
USB_CLK/ UART_SIN02/ GPIO69/ IRQ11/ **TIMER03**	Timer 3	AD7	I/O	CVDD	—
SDHC_WP/ TDM_TFS/ **TIMER04**	Timer 4	D19	I/O	BVDD	—
ANT1_RX_CLK/ **TIMER05**/ TSEC_1588_TRIG_IN2/ GPIO95	Timer 5	B23	I/O	X1VDD	—
ANT1_DIO10/ **TIMER06**/ ANT2_DO10/ GPIO23	Timer 6	B25	I/O	X1VDD	—
ANT1_DIO11/ **TIMER07**/ ANT2_DO11/ GPIO24	Timer 7	C23	I/O	X1VDD	—
ANT2_DIO11/ **TIMER08**/ GPIO61	Timer 8	L22	I/O	X2VDD	—
eSDHC					
SDHC_CLK/ SIM_CLK	SDHC Clock	A22	O	BVDD	—
SDHC_CMD/ SIM_RST_B	SDHC Command	E20	I/O	BVDD	16
SDHC_DATA00/ SIM_TRXD/ TDM_RFS	SDHC Data	E19	I/O	BVDD	16
SDHC_DATA01/ SIM_SVEN/ TDM_RCK/ GPIO77	SDHC Data	D20	I/O	BVDD	16

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SDHC_DATA02/ TDM_TXD/ GPIO78	SDHC Data	B20	I/O	BVDD	16
SDHC_DATA03/ TDM_RXD/ GPIO79/ IRQ10	SDHC Data	C20	I/O	BVDD	16
SDHC_WP/ TDM_TFS/ TIMER04	SDHC Write Protect	D19	I	BVDD	—
SDHC_CD/ TDM_TCK	SDHC Card Detect	B21	I	BVDD	—
USIM					
SDHC_DATA01/ **SIM_SVEN**/ TDM_RCK/ GPIO77	SIM Enable	D20	O	BVDD	15
SPI1_MOSI/ UART_SIN03/ **SIM_SVEN**	SIM Enable	AB6	O	CVDD	15
SDHC_CMD/ **SIM_RST_B**	SIM Reset	E20	O	BVDD	15
SPI1_MISO/ UART_CTS_B03/ **SIM_RST_B**/ CKSTP_IN_B	SIM Reset	AC5	O	CVDD	15
SDHC_DATA00/ **SIM_TRXD**/ TDM_RFS	SIM TX RX Data	E19	I/O	BVDD	14
SPI1_CS0_B/ UART_RTS_B03/ **SIM_TRXD**	SIM TX RX Data	AC6	I/O	CVDD	14
SDHC_CLK/ **SIM_CLK**	SIM Clock	A22	O	BVDD	—
SPI1_CLK/ **SIM_CLK**	SIM Clock	AB7	O	CVDD	—
UART_CTS_B00/ **SIM_PD**/ DSP_TMS/ GPIO42/ IRQ04	SIM Present Detect	D8	I	OVDD	15
UART_CTS_B01/ **SIM_PD**/ SRESET_B/ GPIO44/ IRQ05	SIM Present Detect	E8	I	OVDD	15

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
USB					
USB_CLK/ UART_SIN02/ GPIO69/ IRQ11/ TIMER03	ULPI Clock	AD7	I	CVDD	—
USB_D07/ UART_SOUT02/ GPIO70	ULPI Data	AE8	I/O	CVDD	—
USB_D06/ UART_CTS_B02/ GPIO62	ULPI Data	AB10	I/O	CVDD	—
USB_D05/ UART_RTS_B02/ GPIO63	ULPI Data	AE6	I/O	CVDD	—
USB_D04/ GPIO00/ IRQ00	ULPI Data	AB9	I/O	CVDD	—
USB_D03/ GPIO01/ IRQ01	ULPI Data	AC9	I/O	CVDD	—
USB_D02/ IIC2_SDA/ GPIO71	ULPI Data	AC8	I/O	CVDD	—
USB_D01/ IIC2_SCL/ GPIO72	ULPI Data	AD9	I/O	CVDD	—
USB_D00/ IRQ02	ULPI Data	AE7	I/O	CVDD	—
USB_STP/ IRQ_OUT_B/ GPO73	ULPI Stop	AA8	O	CVDD	—
USB_DIR/ GPIO02/ TIMER01/ MCP_B	ULPI Data Direction	AD6	I	CVDD	—
USB_NXT/ GPIO03/ IRQ03/ TRIG_IN	ULPI Next Data Throttle Control	AD8	I	CVDD	—
USB over RF Interface					
ANT2_DIO09/ **USB_CLK**/ GPIO59	ULPI Clock	L23	I/O	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO07/ **USB_D07**/ GPIO32	ULPI Data	N23	I/O	X2VDD	—
ANT2_DIO06/ **USB_D06**/ GPIO31	ULPI Data	P21	I/O	X2VDD	—
ANT2_DIO05/ **USB_D05**/ GPIO30	ULPI Data	N24	I/O	X2VDD	—
ANT2_DIO04/ **USB_D04**/ GPIO29	ULPI Data	N25	I/O	X2VDD	—
ANT2_DIO03/ **USB_D03**/ GPIO28	ULPI Data	R23	I/O	X2VDD	—
ANT2_DIO02/ **USB_D02**/ GPIO27	ULPI Data	R22	I/O	X2VDD	—
ANT2_DIO01/ **USB_D01**/ GPIO26	ULPI Data	U25	I/O	X2VDD	—
ANT2_DIO00/ **USB_D00**/ GPIO25	ULPI Data	T24	I/O	X2VDD	—
ANT2_ENABLE/ **USB_STP**/ GPO92	ULPI Stop	P24	O	X2VDD	—
ANT2_DIO08/ **USB_DIR**/ GPIO33	ULPI Data Direction	N21	I	X2VDD	—
ANT2_DIO10/ **USB_NXT**/ GPIO60	ULPI Next Data Throttle Control	M23	I	X2VDD	—
USB over TSEC					
TSEC2_RX_CLK/ GPIO06/ IRQ06/ **USB_CLK**	ULPI Clock	AB18	I	LVDD	—
TSEC2_TXD01/ DMA_DDONE_B00/ USB_D07	ULPI Data	AA15	I/O	LVDD	—
TSEC2_TXD02/ GPIO04/ IRQ04/ USB_D06	ULPI Data	AC15	I/O	LVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
TSEC2_TXD03/ GPIO05/ IRQ05/ USB_D05	ULPI Data	AB15	I/O	LVDD	—
TSEC2_RXD00/ DMA_DREQ_B00/ USB_D04	ULPI Data	AD17	I/O	LVDD	—
TSEC2_RXD01/ USB_D03	ULPI Data	AA19	I/O	LVDD	—
TSEC2_RXD02/ USB_D02	ULPI Data	AA16	I/O	LVDD	—
TSEC2_RXD03/ USB_D01	ULPI Data	AC17	I/O	LVDD	—
TSEC2_RX_DV/ USB_D00	ULPI Data	AB17	I/O	LVDD	—
TSEC2_GTX_CLK/ USB_STP	ULPI Stop	AC16	O	LVDD	—
TSEC2_GTX_CLK125/ GPIO07/ IRQ07/ USB_DIR	ULPI Data Direction	AE17	I	LVDD	—
TSEC2_TXD00/ DMA_DACK_B00/ USB_NXT	ULPI Next Data Throttle Control	AA14	I	LVDD	—
SPI1					
SPI1_MOSI/ UART_SIN03/ SIM_SVEN	SPI Master Out Slave In Data	AB6	O	CVDD	—
SPI1_MISO/ UART_CTS_B03/ SIM_RST_B/ CKSTP_IN_B	SPI Master In Slave Out Data	AC5	I	CVDD	—
SPI1_CLK/ SIM_CLK	SPI Serial Clock	AB7	O	CVDD	—
SPI1_CS0_B/ UART_RTS_B03/ SIM_TRXD	SPI Slave Select	AC6	O	CVDD	14
SPI1_CS1_B/ UART_SOUT03/ GPO74	SPI Slave Select	AD4	O	CVDD	22
SPI1_CS2_B/ CKSTP_OUT_B/ GPO75	SPI Slave Select	AE5	O	CVDD	22

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI1_CS3_B/ ANT_TCXO_PWM/ GPO76	SPI Slave Select	AD5	O	CVDD	22
RF Interface SPI2[19]					
SPI2_CLK	SPI Serial Clock	T23	O	X2VDD	—
SPI2_MOSI	SPI Master Out Slave In Data	R21	O	X2VDD	2
SPI2_MISO	SPI Master In Slave Out Data	U23	I	X2VDD	—
SPI2_CS0_B	SPI Slave Select	U24	O	X2VDD	22
SPI2_CS1_B	SPI Slave Select	U22	O	X2VDD	22
SPI2_CS2_B/ GPO93	SPI Slave Select	V24	O	X2VDD	22
SPI2_CS3_B/ GPO94	SPI Slave Select	T21	O	X2VDD	22
SPI3 over RF Interface[1]					
ANT1_DIO02/ **SPI3_CLK**/ ANT2_DO02/ GPIO83	SPI Serial Clock	F22	O	X1VDD	—
ANT1_DIO00/ **SPI3_MOSI**/ ANT2_DO00/ GPIO81	SPI Master Out Slave In Data	E24	O	X1VDD	—
ANT1_DIO01/ **SPI3_MISO**/ ANT2_DO01/ GPIO82	SPI Master In Slave Out Data	E25	I	X1VDD	—
ANT1_DIO03/ **SPI3_CS0_B**/ ANT2_DO03/ GPIO84	SPI Slave Select	E23	O	X1VDD	22
SPI4 over RF Interface[1]					
ANT1_DIO06/ **SPI4_CLK**/ ANT2_DO06/ GPIO87/ IRQ10	SPI Serial Clock	D23	O	X1VDD	—
ANT1_DIO04/ **SPI4_MOSI**/ ANT2_DO04/ GPIO85	SPI Master Out Slave In Data	E22	O	X1VDD	—
ANT1_DIO05/ **SPI4_MISO**/ ANT2_DO05/ GPIO86	SPI Master In Slave Out Data	D25	I	X1VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO07/ **SPI4_CS0_B**/ ANT2_DO07/ GPIO88/ IRQ11	SPI Slave Select	E21	O	X1VDD	22
DUART 1					
UART_SOUT00	UART1 Transmit Data	F5	O	OVDD	2
UART_SIN00	UART1 Receive Data	A7	I	OVDD	—
UART_CTS_B00/ SIM_PD/ DSP_TMS/ GPIO42/ IRQ04	UART1 Clear to Send	D8	I	OVDD	—
UART_RTS_B00/ PWM2/ DSP_TCK/ GPO43	UART1 Ready to Send	A6	O	OVDD	—
UART_SOUT01	UART2 Transmit Data	E5	O	OVDD	2
UART_SIN01	UART2 Receive Data	B6	I	OVDD	—
UART_CTS_B01/ SIM_PD/ SRESET_B/ GPIO44/ IRQ05	UART2 Clear to Send	E8	I	OVDD	—
UART_RTS_B01/ PPS_LED/ GPO45	UART2 Ready to Send	C6	O	OVDD	—
DUART 2					
USB_D07/ **UART_SOUT02**/ GPIO70	UART3 Transmit Data	AE8	O	CVDD	—
USB_CLK/ **UART_SIN02**/ GPIO69/ IRQ11/ TIMER03	UART3 Receive Data	AD7	I	CVDD	—
USB_D06/ **UART_CTS_B02**/ GPIO62	UART3 Clear to Send	AB10	I	CVDD	—
USB_D05/ **UART_RTS_B02**/ GPIO63	UART3 Ready to Send	AE6	O	CVDD	—
SPI1_CS1_B/ **UART_SOUT03**/ GPO74	UART4 Transmit Data	AD4	O	CVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI1_MOSI/ **UART_SIN03**/ SIM_SVEN	UART4 Receive Data	AB6	I	CVDD	—
SPI1_MISO/ **UART_CTS_B03**/ SIM_RST_B/ CKSTP_IN_B	UART4 Clear to Send	AC5	I	CVDD	—
SPI1_CS0_B/ **UART_RTS_B03**/ SIM_TRXD	UART4 Ready to Send	AC6	O	CVDD	—
I^2C1					
IIC1_SDA	Serial Data	C4	I/O	OVDD	5
IIC1_SCL	Serial Clock	B5	I/O	OVDD	5
I^2C2					
USB_D02/ **IIC2_SDA**/ GPIO71	Serial Data	AC8	I/O	CVDD	5
USB_D01/ **IIC2_SCL**/ GPIO72	Serial Clock	AD9	I/O	CVDD	5
System Control/Power Management					
HRESET_B	Hard Reset	A9	I	OVDD	—
HRESET_REQ_B	Hard Reset Request Out	E11	O	OVDD	2, 4
READY/ ASLEEP/ DSP_TRST_B	Ready	A8	O	OVDD	3
READY/ **ASLEEP/** DSP_TRST_B	Asleep	A8	O	OVDD	3
UDE_B	Unconditional Debug Event	B9	I	OVDD	—
EE0	DSP Debug Request	C9	I	OVDD	—
EE1	DSP Debug Acknowledge	B7	O	OVDD	—
TMP_DETECT	Tamper Detect	C8	I	OVDD	—
Clocking					
SYSCLK	System Clock	B1	I	OVDD	—
DDRCLK	DDR PLL Reference Clock	E3	I	OVDD	—
RTC	Real Time Clock	C7	I	OVDD	—
DSP_CLKIN	DSP PLL Reference Clock	E10	I	OVDD	—
MAX_REF_CLK	MAX PHY PLL Reference Clock	D9	I	OVDD	—
I/O Voltage Select					

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
BVDD_VSEL00	BVDD Voltage Selection	H11	I	OVDD	—
BVDD_VSEL01	BVDD Voltage Selection	B2	I	OVDD	—
CVDD_VSEL	CVDD Voltage Selection	C5	I	OVDD	—
LVDD_VSEL	LVDD Voltage Selection	D6	I	OVDD	—
XVDD1_VSEL	XVDD 1 Voltage Selection	C2	I	OVDD	—
XVDD2_VSEL	XVDD 2 Voltage Selection	C1	I	OVDD	—
Test					
SCAN_MODE_B	Scan Mode	A4	I	OVDD	1
CFG_0_JTAG_MODE	JTAG mode selection 0	E7	I	OVDD	9
CFG_1_JTAG_MODE	JTAG mode selection 1	D5	I	OVDD	9
TEST_SEL_B	Test Select	A5	I	OVDD	10
JTAG (Power Architecture)					
TCK	Test Clock	D3	I	OVDD	—
TDI	Test Data In	A3	I	OVDD	3
TDO	Test Data Out	A2	O	OVDD	—
TMS	Test Mode Select	D4	I	OVDD	3
TRST_B	Test Reset	C3	I	OVDD	3
JTAG (DSP)					
UART_RTS_B00/ PWM2/ **DSP_TCK**/ GPO43	DSP Test Clock	A6	I	OVDD	—
IFC_WP_B/ GPO66/ **DSP_TDI**	DSP Test Data In	A20	I	BVDD	3
IFC_BCTL// **DSP_TDO**	DSP Test Data Out	B18	O	BVDD	—
UART_CTS_B00/ SIM_PD/ **DSP_TMS**/ GPIO42/ IRQ04	DSP Test Mode Select	D8	I	OVDD	3
READY/ ASLEEP/ **DSP_TRST_B**	DSP Test Reset	A8	I	OVDD	3
RF Interface 1[10]					
ANT1_TX_CLK/ TSEC_1588_ALARM_OUT2	Transmit Clock	B22	O	X1VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_RX_CLK/ TIMER05/ TSEC_1588_TRIG_IN2/ GPIO95	Receive Clock	B23	I	X1VDD	—
ANT1_TXNRX/ TSEC_1588_PULSE_OUT2/ GPO19	TX_RX Control	C22	O	X1VDD	—
ANT1_ENABLE/ TSEC_1588_ALARM_OUT1	Antenna Enable	B24	O	X1VDD	—
ANT1_TX_FRAME/ GPO20	Transmit Frame	D21	O	X1VDD	4,11
ANT1_RX_FRAME/ MAX3_LOCK/ GPIO80	Receive Frame	A24	I	X1VDD	—
ANT1_DIO00/ SPI3_MOSI/ ANT2_DO00/ GPIO81	Data	E24	I/O	X1VDD	—
ANT1_DIO01/ SPI3_MISO/ ANT2_DO01/ GPIO82	Data	E25	I/O	X1VDD	—
ANT1_DIO02/ SPI3_CLK/ ANT2_DO02/ GPIO83	Data	F22	I/O	X1VDD	—
ANT1_DIO03/ SPI3_CS0_B/ ANT2_DO03/ GPIO84	Data	E23	I/O	X1VDD	—
ANT1_DIO04/ SPI4_MOSI/ ANT2_DO04/ GPIO85	Data	E22	I/O	X1VDD	—
ANT1_DIO05/ SPI4_MISO/ ANT2_DO05/ GPIO86	Data	D25	I/O	X1VDD	—
ANT1_DIO06/ SPI4_CLK/ ANT2_DO06/ GPIO87/ IRQ10	Data	D23	I/O	X1VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO07/ SPI4_CS0_B/ ANT2_DO07/ GPIO88/ IRQ11	Data	E21	I/O	X1VDD	—
ANT1_DIO08/ MAX1_LOCK/ ANT2_DO08/ GPIO21/ IRQ08	Data	D24	I/O	X1VDD	—
ANT1_DIO09/ MAX2_LOCK/ ANT2_DO09/ GPIO22/ IRQ09	Data	C25	I/O	X1VDD	—
ANT1_DIO10/ TIMER06/ ANT2_DO10/ GPIO23	Data	B25	I/O	X1VDD	—
ANT1_DIO11/ TIMER07/ ANT2_DO11/ GPIO24	Data	C23	I/O	X1VDD	—
RF Interface 2[10]					
ANT_REF_CLK	Parallel Interface Reference Clock	M22	I	X2VDD	—
ANT2_AGC/ GPO89	AGC Control	M21	O	X2VDD	2
ANT2_TX_CLK/ GPO90	Transmit Clock	M25	O	X2VDD	—
ANT2_RX_CLK/ GPIO91	Receive Clock	P22	I	X2VDD	—
ANT2_TXNRX/ DMA_DACK_B00	TX_RX Control	P23	O	X2VDD	—
ANT2_ENABLE/ USB_STP/ GPO92	Antenna Enable	P24	O	X2VDD	—
ANT2_TX_FRAME/ DMA_DDONE_B00	Transmit Frame	T25	O	X2VDD	4,11
ANT2_RX_FRAME/ DMA_DREQ_B00	Receive Frame	P25	I	X2VDD	—
ANT2_DIO00/ USB_D00/ GPIO25	Data	T24	I/O	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO01/ USB_D01/ GPIO26	Data	U25	I/O	X2VDD	—
ANT2_DIO02/ USB_D02/ GPIO27	Data	R22	I/O	X2VDD	—
ANT2_DIO03/ USB_D03/ GPIO28	Data	R23	I/O	X2VDD	—
ANT2_DIO04/ USB_D04/ GPIO29	Data	N25	I/O	X2VDD	—
ANT2_DIO05/ USB_D05/ GPIO30	Data	N24	I/O	X2VDD	—
ANT2_DIO06/ USB_D06/ GPIO31	Data	P21	I/O	X2VDD	—
ANT2_DIO07/ USB_D07/ GPIO32	Data	N23	I/O	X2VDD	—
ANT2_DIO08/ USB_DIR/ GPIO33	Data	N21	I/O	X2VDD	—
ANT2_DIO09/ USB_CLK/ GPIO59	Data	L23	I/O	X2VDD	—
ANT2_DIO10/ USB_NXT/ GPIO60	Data	M23	I/O	X2VDD	—
ANT2_DIO11/ TIMER08/ GPIO61	Data	L22	I/O	X2VDD	—
RF Interface 3[10]					
ANT3_AGC/ GPO58	AGC Control	V25	O	X2VDD	2
ANT3_TX_CLK	Transmit Clock	W24	O	X2VDD	—
ANT3_RX_CLK	Receive Clock	W25	I	X2VDD	—
ANT3_TXNRX	TX_RX Control	Y25	O	X2VDD	—
ANT3_ENABLE	Antenna Enable	U21	O	X2VDD	—
ANT3_TX_FRAME	Transmit Frame	W23	O	X2VDD	—
ANT3_RX_FRAME	Receive Frame	V22	I	X2VDD	—
ANT3_DIO00	Data	AB24	I/O	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT3_DIO01	Data	AA22	I/O	X2VDD	4
ANT3_DIO02	Data	AB23	I/O	X2VDD	4
ANT3_DIO03	Data	Y21	I/O	X2VDD	4
ANT3_DIO04	Data	AB25	I/O	X2VDD	4
ANT3_DIO05	Data	W21	I/O	X2VDD	4
ANT3_DIO06	Data	V21	I/O	X2VDD	4
ANT3_DIO07	Data	AA23	I/O	X2VDD	—
ANT3_DIO08	Data	AA25	I/O	X2VDD	—
ANT3_DIO09	Data	Y22	I/O	X2VDD	2
ANT3_DIO10	Data	Y24	I/O	X2VDD	—
ANT3_DIO11	Data	Y23	I/O	X2VDD	—
ANT3_DO00// GPIO46	Data	AE24	O	X2VDD	—
ANT3_DO01/ TDM_TFS/ GPIO47	Data	AD22	O	X2VDD	—
ANT3_DO02/ TDM_RXD/ GPIO48	Data	AE23	O	X2VDD	—
ANT3_DO03/ TDM_TXD/ GPIO49	Data	AE22	O	X2VDD	—
ANT3_DO04/ TDM_RCK/ GPIO50/ IRQ00	Data	AC22	O	X2VDD	—
ANT3_DO05/ TDM_RFS/ GPIO51/ IRQ01	Data	AB21	O	X2VDD	—
ANT3_DO06/ TRIG_IN/ GPIO52/ IRQ02	Data	AC23	O	X2VDD	—
ANT3_DO07/ SRESET_B/ GPIO53/ IRQ03	Data	AD25	O	X2VDD	—
ANT3_DO08/ MCP_B/ GPIO54	Data	AA21	O	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT3_DO09/ CKSTP_IN_B/ GPIO55	Data	AD23	O	X2VDD	—
ANT3_DO10/ CKSTP_OUT_B/ GPIO56	Data	AC25	O	X2VDD	—
ANT3_DO11/ IRQ_OUT_B/ GPIO57	Data	AC24	O	X2VDD	—
RF Serial (MaxPHY) Interface[10]					
MAX1_TX_I	Data (pos)	L21	O	RVDD	—
MAX1_TX_I_B	Data (neg)	K21	O	RVDD	—
MAX1_TX_Q	Data (pos)	G22	O	RVDD	—
MAX1_TX_Q_B	Data (neg)	G23	O	RVDD	—
MAX2_TX_I	Data (pos)	F24	O	RVDD	—
MAX2_TX_I_B	Data (neg)	F25	O	RVDD	—
MAX2_TX_Q	Data (pos)	J24	O	RVDD	—
MAX2_TX_Q_B	Data (neg)	J25	O	RVDD	—
MAX3_TX_I	Data (pos)	G24	O	RVDD	—
MAX3_TX_I_B	Data (neg)	G25	O	RVDD	—
MAX3_TX_Q	Data (pos)	J22	O	RVDD	—
MAX3_TX_Q_B	Data (neg)	J23	O	RVDD	—
MAX1_RX_I	Data (pos)	H24	I	RVDD	—
MAX1_RX_I_B	Data (neg)	H25	I	RVDD	—
MAX1_RX_Q	Data (pos)	F21	I	RVDD	—
MAX1_RX_Q_B	Data (neg)	G21	I	RVDD	—
MAX2_RX_I	Data (pos)	H21	I	RVDD	—
MAX2_RX_I_B	Data (neg)	J21	I	RVDD	—
MAX2_RX_Q	Data (pos)	K24	I	RVDD	—
MAX2_RX_Q_B	Data (neg)	K25	I	RVDD	—
MAX_TX_CLK	Clock	L24	O	RVDD	—
MAX_TX_CLK_B	Clock (complement)	L25	O	RVDD	—
Programmable Interrupt Controller over USB					
USB_STP/ **IRQ_OUT_B**/ GPO73	Interrupt Output	AA8	O	CVDD	—
USB_D04/ GPIO00/ **IRQ00**	External Interrupt	AB9	I	CVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
USB_D03/ GPIO01/ **IRQ01**	External Interrupt	AC9	I	CVDD	—
USB_D00/ **IRQ02**	External Interrupt	AE7	I	CVDD	—
USB_NXT/ GPIO03/ **IRQ03**/ TRIG_IN	External Interrupt	AD8	I	CVDD	—
USB_CLK/ UART_SIN02/ GPIO69/ **IRQ11**/ TIMER03	External Interrupt	AD7	I	CVDD	—
Programmable Interrupt Controller over TSEC2					
TSEC2_TXD02/ GPIO04/ **IRQ04**/ USB_D06	External Interrupt	AC15	I	LVDD	—
TSEC2_TXD03/ GPIO05/ **IRQ05**/ USB_D05	External Interrupt	AB15	I	LVDD	—
TSEC2_RX_CLK/ GPIO06/ **IRQ06**/ USB_CLK	External Interrupt	AB18	I	LVDD	—
TSEC2_GTX_CLK125/ GPIO07/ **IRQ07**/ USB_DIR	External Interrupt	AE17	I/O	LVDD	—
Programmable Interrupt Controller over IFC					
IFC_AD14/ GPIO40/ **IRQ06**	External Interrupt	E14	I	BVDD	—
IFC_AD13/ GPIO39/ **IRQ07**	External Interrupt	D15	I	BVDD	—
IFC_AD11/ GPIO37/ **IRQ08**	External Interrupt	C10	I	BVDD	—
IFC_AD12/ GPIO38/ **IRQ09**	External Interrupt	D11	I	BVDD	—
Programmable Interrupt Controller over RF Interface 1					

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO08/ MAX1_LOCK/ ANT2_DO08/ GPIO21/ **IRQ08**	External Interrupt	D24	I	X1VDD	—
ANT1_DIO09/ MAX2_LOCK/ ANT2_DO09/ GPIO22/ **IRQ09**	External Interrupt	C25	I	X1VDD	—
ANT1_DIO06/ SPI4_CLK/ ANT2_DO06/ GPIO87/ **IRQ10**	External Interrupt	D23	I	X1VDD	—
ANT1_DIO07/ SPI4_CS0_B/ ANT2_DO07/ GPIO88/ **IRQ11**	External Interrupt	E21	I	X1VDD	—
Programmable Interrupt Controller over RF Interface 3					
ANT3_DO11/ **IRQ_OUT_B**/ GPIO57	Interrupt Output	AC24	O	X2VDD	—
ANT3_DO04/ TDM_RCK/ GPIO50/ **IRQ00**	External Interrupt	AC22	I	X2VDD	—
ANT3_DO05/ TDM_RFS/ GPIO51/ **IRQ01**	External Interrupt	AB21	I	X2VDD	—
ANT3_DO06/ TRIG_IN/ GPIO52/ **IRQ02**	External Interrupt	AC23	I	X2VDD	—
ANT3_DO07/ SRESET_B/ GPIO53/ **IRQ03**	External Interrupt	AD25	I	X2VDD	—
ANT3_DO08/ **MCP_B**/ GPIO54	Machine check processor	AA21	I	X2VDD	—
Programmable Interrupt Controller over UART					

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
UART_CTS_B00/ SIM_PD/ DSP_TMS/ GPIO42/ IRQ04	External Interrupt	D8	I	OVDD	—
UART_CTS_B01/ SI\M_PD/ SRESET_B/ GPIO44/ **IRQ05**	External Interrupt	E8	I	OVDD	—
Programmable Interrupt Controller over SDHC					
SDHC_DATA03/ TDM_RXD/ GPIO79/ **IRQ10**	External Interrupt	C20	I	BVDD	—
DMA over TSEC2					
TSEC2_TXD00/ **DMA_DACK_B00**/ USB_NXT	DMA Acknowledge	AA14	O	LVDD	—
TSEC2_RXD00/ **DMA_DREQ_B00**/ USB_D04	DMA Request	AD17	I	LVDD	—
TSEC2_TXD01/ **DMA_DDONE_B00**/ USB_D07	DMA Done	AA15	O	LVDD	—
DMA over RF Interface 2					
ANT2_TXNRX/ **DMA_DACK_B00**	DMA Acknowledge	P23	O	X2VDD	—
ANT2_RX_FRAME/ **DMA_DREQ_B00**	DMA Done	P25	I	X2VDD	—
ANT2_TX_FRAME/ **DMA_DDONE_B00**	DMA Request	T25	O	X2VDD	—
GPIO					
USB_D04/ **GPIO00**/ IRQ00	General Purpose I/O	AB9	I/O	CVDD	—
USB_D03/ **GPIO01**/ IRQ01	General Purpose I/O	AC9	I/O	CVDD	—
USB_DIR/ **GPIO02**/ TIMER01/ MCP_B	General Purpose I/O	AD6	I/O	CVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
USB_NXT/ **GPIO03**/ IRQ03/ TRIG_IN	General Purpose I/O	AD8	I/O	CVDD	—
TSEC2_TXD02/ **GPIO04**/ IRQ04/ USB_D06	General Purpose I/O	AC15	I/O	LVDD	—
TSEC2_TXD03/ **GPIO05**/ IRQ05/ USB_D05	General Purpose I/O	AB15	I/O	LVDD	—
TSEC2_RX_CLK/ **GPIO06**/ IRQ06/ USB_CLK	General Purpose I/O	AB18	I/O	LVDD	—
TSEC2_GTX_CLK125/ **GPIO07**/ IRQ07/ USB_DIR	General Purpose I/O	AE17	I/O	LVDD	—
ANT1_DIO08/ MAX1_LOCK/ ANT2_DO08/ **GPIO21**/ IRQ08	General Purpose I/O	D24	I/O	X1VDD	—
ANT1_DIO09/ MAX2_LOCK/ ANT2_DO09/ **GPIO22**/ IRQ09	General Purpose I/O	C25	I/O	X1VDD	—
ANT1_DIO10/ TIMER06/ ANT2_DO10/ **GPIO23**	General Purpose I/O	B25	I/O	X1VDD	—
ANT1_DIO11/ TIMER07/ ANT2_DO11/ **GPIO24**	General Purpose I/O	C23	I/O	X1VDD	—
ANT2_DIO00/ USB_D00/ **GPIO25**	General Purpose I/O	T24	I/O	X2VDD	—
ANT2_DIO01/ USB_D01/ **GPIO26**	General Purpose I/O	U25	I/O	X2VDD	—
ANT2_DIO02/ USB_D02/ **GPIO27**	General Purpose I/O	R22	I/O	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO03/ USB_D03/ **GPIO28**	General Purpose I/O	R23	I/O	X2VDD	—
ANT2_DIO04/ USB_D04/ **GPIO29**	General Purpose I/O	N25	I/O	X2VDD	—
ANT2_DIO05/ USB_D05/ **GPIO30**	General Purpose I/O	N24	I/O	X2VDD	—
ANT2_DIO06/ USB_D06/ **GPIO31**	General Purpose I/O	P21	I/O	X2VDD	—
ANT2_DIO07/ USB_D07/ **GPIO32**	General Purpose I/O	N23	I/O	X2VDD	—
ANT2_DIO08/ USB_DIR/ **GPIO33**	General Purpose I/O	N21	I/O	X2VDD	—
IFC_AD08/ **GPIO34**	General Purpose I/O	E13	I/O	BVDD	—
IFC_AD09/ **GPIO35**	General Purpose I/O	A10	I/O	BVDD	—
IFC_AD10/ **GPIO36**	General Purpose I/O	A12	I/O	BVDD	—
IFC_AD11/ **GPIO37**/ IRQ08	General Purpose I/O	C10	I/O	BVDD	—
IFC_AD12/ **GPIO38**/ IRQ09	General Purpose I/O	D11	I/O	BVDD	—
IFC_AD13/ **GPIO39**/ IRQ07	General Purpose I/O	D15	I/O	BVDD	—
IFC_AD14/ **GPIO40**/ IRQ06	General Purpose I/O	E14	I/O	BVDD	—
IFC_AD15/ **GPIO41**/ TIMER02	General Purpose I/O	C13	I/O	BVDD	—
UART_CTS_B00/ SIM_PD/ DSP_TMS/ **GPIO42**/ IRQ04	General Purpose I/O	D8	I/O	OVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
UART_CTS_B01/ SIM_PD/ SRESET_B/ **GPIO44**/ IRQ05	General Purpose I/O	E8	I/O	OVDD	—
ANT3_DO00/ TDM_TCK/ **GPIO46**	General Purpose I/O	AE24	I/O	X2VDD	—
ANT3_DO01/ TDM_TFS/ **GPIO47**	General Purpose I/O	AD22	I/O	X2VDD	—
ANT3_DO02/ TDM_RXD/ **GPIO48**	General Purpose I/O	AE23	I/O	X2VDD	—
ANT3_DO03/ TDM_TXD/ **GPIO49**	General Purpose I/O	AE22	I/O	X2VDD	—
ANT3_DO04/ TDM_RCK/ **GPIO50**/ IRQ00	General Purpose I/O	AC22	I/O	X2VDD	—
ANT3_DO05/ TDM_RFS/ **GPIO51**/ IRQ01	General Purpose I/O	AB21	I/O	X2VDD	—
ANT3_DO06/ TRIG_IN/ **GPIO52**/ IRQ02	General Purpose I/O	AC23	I/O	X2VDD	—
ANT3_DO07/ SRESET_B/ **GPIO53**/ IRQ03	General Purpose I/O	AD25	I/O	X2VDD	—
ANT3_DO08/ MCP_B/ **GPIO54**	General Purpose I/O	AA21	I/O	X2VDD	—
ANT3_DO09/ CKSTP_IN_B/ **GPIO55**	General Purpose I/O	AD23	I/O	X2VDD	—
ANT3_DO10/ CKSTP_OUT_B/ **GPIO56**	General Purpose I/O	AC25	I/O	X2VDD	—
ANT3_DO11/ IRQ_OUT_B/ **GPIO57**	General Purpose I/O	AC24	I/O	X2VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO09/ USB_CLK/ **GPIO59**	General Purpose I/O	L23	I/O	X2VDD	—
ANT2_DIO10/ USB_NXT/ **GPIO60**	General Purpose I/O	M23	I/O	X2VDD	—
ANT2_DIO11/ TIMER08/ **GPIO61**	General Purpose I/O	L22	I/O	X2VDD	—
USB_D06/ UART_CTS_B02/ **GPIO62**	General Purpose I/O	AB10	I/O	CVDD	—
USB_D05/ UART_RTS_B02/ **GPIO63**	General Purpose I/O	AE6	I/O	CVDD	—
USB_CLK/ UART_SIN02/ **GPIO69**/ IRQ11/ TIMER03	General Purpose I/O	AD7	I/O	CVDD	—
USB_D07/ UART_SOUT02/ **GPIO70**	General Purpose I/O	AE8	I/O	CVDD	—
USB_D02/ IIC2_SDA/ **GPIO71**	General Purpose I/O	AC8	I/O	CVDD	—
USB_D01/ IIC2_SCL/ **GPIO72**	General Purpose I/O	AD9	I/O	CVDD	—
SDHC_DATA01/ SIM_SVEN/ TDM_RCK/ **GPIO77**	General Purpose I/O	D20	I/O	BVDD	—
SDHC_DATA02/ TDM_TXD/ **GPIO78**	General Purpose I/O	B20	I/O	BVDD	—
SDHC_DATA03/ TDM_RXD/ **GPIO79**/ IRQ10	General Purpose I/O	C20	I/O	BVDD	—
ANT1_RX_FRAME/ MAX3_LOCK/ **GPIO80**	General Purpose I/O	A24	I/O	X1VDD	—
ANT1_DIO00/ SPI3_MOSI/ ANT2_DO00/ **GPIO81**	General Purpose I/O	E24	I/O	X1VDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO01/ SPI3_MISO/ ANT2_DO01/ **GPIO82**	General Purpose I/O	E25	I/O	X1VDD	—
ANT1_DIO02/ SPI3_CLK/ ANT2_DO02/ **GPIO83**	General Purpose I/O	F22	I/O	X1VDD	—
ANT1_DIO03/ SPI3_CS0_B/ ANT2_DO03/ **GPIO84**	General Purpose I/O	E23	I/O	X1VDD	—
ANT1_DIO04/ SPI4_MOSI/ ANT2_DO04/ **GPIO85**	General Purpose I/O	E22	I/O	X1VDD	—
ANT1_DIO05/ SPI4_MISO/ ANT2_DO05/ **GPIO86**	General Purpose I/O	D25	I/O	X1VDD	—
ANT1_DIO06/ SPI4_CLK/ ANT2_DO06/ **GPIO87**/ IRQ10	General Purpose I/O	D23	I/O	X1VDD	—
ANT1_DIO07/ SPI4_CS0_B/ ANT2_DO07/ **GPIO88**/ IRQ11	General Purpose I/O	E21	I/O	X1VDD	—
ANT2_RX_CLK/ **GPIO91**	General Purpose I/O	J3	I/O	X2VDD	—
ANT1_RX_CLK/ TIMER05/ TSEC_1588_TRIG_IN2/ **GPIO95**	General Purpose I/O	B23	I/O	X1VDD	—
GPO					
IFC_ADDR16/ **GPO08**	General Purpose Output	C14	O	BVDD	—
IFC_ADDR17/ **GPO09**	General Purpose Output	A14	O	BVDD	—
IFC_ADDR18/ **GPO10**	General Purpose Output	B15	O	BVDD	—
IFC_ADDR19/ **GPO11**	General Purpose Output	A18	O	BVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_ADDR20/ **GPO12**	General Purpose Output	A15	O	BVDD	—
IFC_ADDR21/ **GPO13**	General Purpose Output	A13	O	BVDD	—
IFC_ADDR22/ **GPO14**	General Purpose Output	C17	O	BVDD	—
IFC_ADDR23/ **GPO15**	General Purpose Output	C16	O	BVDD	—
IFC_ADDR24/ **GPO16**	General Purpose Output	A16	O	BVDD	—
IFC_ADDR25/ **GPO17**	General Purpose Output	B16	O	BVDD	—
IFC_ADDR26/ **GPO18**	General Purpose Output	D17	O	BVDD	—
ANT1_TX_FRAME/ **GPO20**	General Purpose Output	D21	O	X1VDD	—
UART_RTS_B00/ PWM2/ DSP_TCK/ **GPO43**	General Purpose Output	A6	O	OVDD	—
UART_RTS_B01/ PPS_LED/ **GPO45**	General Purpose Output	C6	O	OVDD	—
ANT3_AGC/ **GPO58**	General Purpose Output	V25	O	X2VDD	—
IFC_CS_B01/ **GPO64**	General Purpose Output	C19	O	BVDD	—
IFC_CS_B02/ **GPO65**	General Purpose Output	D18	O	BVDD	—
IFC_WP_B/ **GPO66**/ DSP_TDI	General Purpose Output	A20	O	BVDD	—
IFC_BCTL/ **GPO67**/ DSP_TDO	General Purpose Output	B18	O	BVDD	—
IFC_CLK00/ **GPO68**	General Purpose Output	C18	O	BVDD	—
USB_STP/ IRQ_OUT_B/ **GPO73**	General Purpose Output	AA8	O	CVDD	—
SPI1_CS1_B/ UART_SOUT03/ **GPO74**	General Purpose Output	AD4	O	CVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SPI1_CS2_B/ CKSTP_OUT_B/ **GPO75**	General Purpose Output	AE5	O	CVDD	—
SPI1_CS3_B/ ANT_TCXO_PWM/ **GPO76**	General Purpose Output	AD5	O	CVDD	—
ANT2_AGC/ **GPO89**	General Purpose Output	M21	O	X2VDD	—
ANT2_TX_CLK/ **GPO90**	General Purpose Output	M25	O	X2VDD	—
ANT2_ENABLE/ USB_STP/ **GPO92**	General Purpose Output	P24	O	X2VDD	—
SPI2_CS2_B/ **GPO93**	General Purpose Output	V24	O	X2VDD	—
SPI2_CS3_B/ **GPO94**	General Purpose Output	T21	O	X2VDD	—
Analog					
MVREF	DDR Reference Voltage	M8	I	GVDD/2	—
TEMP_ANODE	Temperature Diode Anode	AE9	—	Internal Diode	8
TEMP_CATHODE	Temperature Diode Cathode	AE12	—	Internal Diode	8
SENSEVDD	VDD Sensing Pin—MAPLE	H17	—	—	13
SENSEVDDC	VDD Sensing Pin	AB5	—	—	13
SENSEVSS	GND Sensing Pin	AA6	—	—	13
Reset Configuration					
EC_MDC/**cfg_dsp_pll[0]**	DSP Subsystem PLL Configurations	AE18	I	LVDD	20
IFC_ADDR16/ GPO08/**cfg_dsp_pll[1]**	DSP Subsystem PLL Configurations	C14	I	BVDD	20
IFC_ADDR17/ GPO09/**cfg_dsp_pll[2]**	DSP Subsystem PLL Configurations	A14	I	BVDD	20
IFC_ADDR18/ GPO10/**cfg_dsp_pll[3]**	DSP Subsystem PLL Configurations	B15	I	BVDD	20
TSEC1_TXD00/**cfg_rom_loc[0]**	Boot ROM Location	AE11	I	LVDD	20
TSEC1_TXD01/**cfg_rom_loc[1]**	Boot ROM Location	AC10	I	LVDD	20
TSEC1_TXD02/**cfg_rom_loc[2]**	Boot ROM Location	AC12	I	LVDD	20
TSEC1_TXD03/**cfg_rom_loc[3]**	Boot ROM Location	AE15	I	LVDD	20
IFC_AD00/**cfg_sys_pll[0]**	CCB Clock PLL Ratio	B10	I	BVDD	21
IFC_AD01/**cfg_sys_pll[1]**	CCB Clock PLL Ratio	C11	I	BVDD	21
IFC_AD02/**cfg_sys_pll[2]**	CCB Clock PLL Ratio	D12	I	BVDD	21
IFC_AD03/**cfg_core_pll[0]**	e500 Core PLL Ratio	C12	I	BVDD	21

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_AD04/**cfg_core_pll[1]**	e500 Core PLL Ratio	A11	I	BVDD	21
IFC_AD05/**cfg_core_pll[2]**	e500 Core PLL Ratio	B12	I	BVDD	21
IFC_AD06/**cfg_core_speed**	Core Speed	B13	I	BVDD	20
IFC_AD07/**cfg_ddr_pll[0]**	DDR Complex Clock PLL Ratio	D14	I	BVDD	21
IFC_ADDR22/ GPO14/**cfg_ddr_pll[1]**	DDR Complex Clock PLL Ratio	C17	I	BVDD	21
IFC_ADDR19/ GPO11/**cfg_boot_seq[0]**	Boot Sequencer Configuration	A18	I	BVDD	20
TSEC_1588_PULSE_OUT1/ PPS_OUT/**cfg_boot_seq[1]**	Boot Sequencer Configuration	AC19	I	LVDD	20
IFC_OE_B/**cfg_cpu_boot**	CPU Boot Configuration	E16	I	BVDD	20
IFC_ADDR24/ GPO16/**cfg_ddr_speed[0]**	DDR Speed	A16	I	BVDD	20
UART_SOUT00/ **cfg_ddr_speed[1]**	DDR Speed	F5	I	OVDD	20
IFC_AVD/**cfg_dram_type**	DDR DRAM Type	E17	I	BVDD	20
IFC_WE_B/**cfg_ifc_adm_mode**	IFC Address Shift Mode Configuration	A19	I	BVDD	20
ANT3_AGC/ GPO58/**cfg_ifc_flash_mode**	IFC Flash Mode Configuration	V25	I	X2VDD	20
SPI2_MOSI/**cfg_ifc_ecc[0]**	IFC ECC Enable Configuration	R21	I	X2VDD	20
UART_SOUT01/**cfg_ifc_ecc[1]**	IFC ECC Enable Configuration	E5	I	OVDD	20
IFC_ADDR23/ GPO15/**cfg_ifc_pb[0]**	IFC Pages Per Block	C16	I	BVDD	20
IFC_ADDR25/ GPO17/**cfg_ifc_pb[1]**	IFC Pages Per Block	B16	I	BVDD	20
IFC_ADDR26/ GPO18/**cfg_ifc_pb[2]**	IFC Pages Per Block	D17	I	BVDD	20
IFC_ADDR20/ GPO12/**cfg_plat_speed**	Platform Speed	A15	I	BVDD	20
IFC_ADDR21/ GPO13/**cfg_sys_speed**	System Speed	A13	I	BVDD	20
ANT2_AGC/ GPO89/ **cfg_ddr_half_full_mode**	Power Architecture DDR Mode	M21	I	X2VDD	20
IFC_CLE/**cfg_tsec1_prctl**	eTSEC1 Protocol	C15	I	BVDD	20
Power Supply					
AVDD_PLAT	Platform PLL Supply	V9	—	AVDD_PLAT	—
AVDD_CORE	Core PLL Supply	V10	—	AVDD_CORE	—
AVDD_DDR	DDR PLL Supply	H8	—	AVDD_DDR	—
AVDD_DSP	DSP PLL Supply	N18	—	AVDD_DSP	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
AVDD_RF	RF PLL Supply	M17	—	AVDD_RF	—
POVDD1	Secure Fuse Programming Overdrive	N8	—	POVDD1	—
POVDD2	Central Fuse Programming Overdrive—Power Architecture	L8	—	—	7
POVDD3	Central Fuse Programming Overdrive—DSP	AA10	—	—	7
FA_VDD	POSt VDD	U9	—	—	6
VDDC	Core/Platform Supply	T10	—	VDDC	—
VDDC	Core/Platform Supply	J9	—	VDDC	—
VDDC	Core/Platform Supply	J11	—	VDDC	—
VDDC	Core/Platform Supply	J13	—	VDDC	—
VDDC	Core/Platform Supply	J15	—	VDDC	—
VDDC	Core/Platform Supply	K10	—	VDDC	—
VDDC	Core/Platform Supply	K12	—	VDDC	—
VDDC	Core/Platform Supply	L9	—	VDDC	—
VDDC	Core/Platform Supply	L11	—	VDDC	—
VDDC	Core/Platform Supply	L13	—	VDDC	—
VDDC	Core/Platform Supply	M10	—	VDDC	—
VDDC	Core/Platform Supply	M12	—	VDDC	—
VDDC	Core/Platform Supply	N9	—	VDDC	—
VDDC	Core/Platform Supply	N11	—	VDDC	—
VDDC	Core/Platform Supply	N13	—	VDDC	—
VDDC	Core/Platform Supply	P10	—	VDDC	—
VDDC	Core/Platform Supply	P12	—	VDDC	—
VDDC	Core/Platform Supply	P14	—	VDDC	—
VDDC	Core/Platform Supply	P16	—	VDDC	—
VDDC	Core/Platform Supply	R9	—	VDDC	—
VDDC	Core/Platform Supply	R11	—	VDDC	—
VDDC	Core/Platform Supply	R13	—	VDDC	—
VDDC	Core/Platform Supply	R15	—	VDDC	—
VDDC	Core/Platform Supply	R17	—	VDDC	—
VDDC	Core/Platform Supply	T12	—	VDDC	—
VDDC	Core/Platform Supply	T14	—	VDDC	—
VDDC	Core/Platform Supply	T16	—	VDDC	—
VDDC	Core/Platform Supply	U11	—	VDDC	—
VDDC	Core/Platform Supply	U13	—	VDDC	—
VDDC	Core/Platform Supply	U15	—	VDDC	—
VDDC	Core/Platform Supply	U17	—	VDDC	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VDD	MAPLE Supply	J17	—	VDD	—
VDD	MAPLE Supply	K14	—	VDD	—
VDD	MAPLE Supply	K16	—	VDD	—
VDD	MAPLE Supply	L15	—	VDD	—
VDD	MAPLE Supply	L17	—	VDD	—
VDD	MAPLE Supply	M14	—	VDD	—
VDD	MAPLE Supply	M16	—	VDD	—
VDD	MAPLE Supply	N15	—	VDD	—
VDD	MAPLE Supply	N17	—	VDD	—
GVDD	DDR Supply	H5	—	GVDD	—
GVDD	DDR Supply	P8	—	GVDD	—
GVDD	DDR Supply	R8	—	GVDD	—
GVDD	DDR Supply	T8	—	GVDD	—
GVDD	DDR Supply	U8	—	GVDD	—
GVDD	DDR Supply	V8	—	GVDD	—
GVDD	DDR Supply	J8	—	GVDD	—
GVDD	DDR Supply	K8	—	GVDD	—
GVDD	DDR Supply	L5	—	GVDD	—
GVDD	DDR Supply	P5	—	GVDD	—
GVDD	DDR Supply	U5	—	GVDD	—
GVDD	DDR Supply	Y5	—	GVDD	—
LVDD	Ethernet Supply	V12	—	LVDD	—
LVDD	Ethernet Supply	V14	—	LVDD	—
LVDD	Ethernet Supply	V15	—	LVDD	—
LVDD	Ethernet Supply	V16	—	LVDD	—
LVDD	Ethernet Supply	V17	—	LVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	E12	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	E15	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	E18	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	H12	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	H13	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	H14	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	H15	—	BVDD	—
BVDD	IFC, eSDHC, USIM, TDM Supply	H16	—	BVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	V11	—	CVDD	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	V13	—	CVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	AA7	—	CVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	AA9	—	CVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	AB14	—	CVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	AA17	—	CVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	AC7	—	CVDD	—
CVDD	USB, eSPI, DUART, UART, I2C, USIM, PWM Supply	AC11	—	CVDD	—
OVDD	DUART1, System, I2C, PWM, JTAG Supply	B4	—	OVDD	—
OVDD	DUART1, System, I2C, PWM, JTAG Supply	E6	—	OVDD	—
OVDD	DUART1, System, I2C, PWM, JTAG Supply	E9	—	OVDD	—
OVDD	DUART1, System, I2C, PWM, JTAG Supply	H9	—	OVDD	—
OVDD	DUART1, System, I2C, PWM, JTAG Supply	H10	—	OVDD	—
X1VDD	eSPI, RF Supply	A23	—	X1VDD	—
X1VDD	eSPI, RF Supply	D22	—	X1VDD	—
X1VDD	eSPI, RF Supply	H18	—	X1VDD	—
X1VDD	eSPI, RF Supply	J18	—	X1VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	P18	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	R18	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	T18	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	U18	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	V18	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	V23	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	AB22	—	X2VDD	—
X2VDD	eSPI, USB, TDM, RF Supply	AE21	—	X2VDD	—
RVDD	RF Supply	H23	—	RVDD	—
RVDD	RF Supply	K18	—	RVDD	—
RVDD	RF Supply	L18	—	RVDD	—
RVDD	RF Supply	M18	—	RVDD	—
Ground					
VSS	Platform and Core Ground	A25	—	—	—
VSS	Platform and Core Ground	B3	—	—	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	B8	—	—	—
VSS	Platform and Core Ground	B11	—	—	—
VSS	Platform and Core Ground	B14	—	—	—
VSS	Platform and Core Ground	B17	—	—	—
VSS	Platform and Core Ground	B19	—	—	—
VSS	Platform and Core Ground	C21	—	—	—
VSS	Platform and Core Ground	C24	—	—	—
VSS	Platform and Core Ground	D2	—	—	—
VSS	Platform and Core Ground	D7	—	—	—
VSS	Platform and Core Ground	D10	—	—	—
VSS	Platform and Core Ground	D13	—	—	—
VSS	Platform and Core Ground	D16	—	—	—
VSS	Platform and Core Ground	E4	—	—	—
VSS	Platform and Core Ground	F23	—	—	—
VSS	Platform and Core Ground	G2	—	—	—
VSS	Platform and Core Ground	H22	—	—	—
VSS	Platform and Core Ground	J4	—	—	—
VSS	Platform and Core Ground	J10	—	—	—
VSS	Platform and Core Ground	J12	—	—	—
VSS	Platform and Core Ground	J14	—	—	—
VSS	Platform and Core Ground	J16	—	—	—
VSS	Platform and Core Ground	K15	—	—	—
VSS	Platform and Core Ground	K17	—	—	—
VSS	Platform and Core Ground	K22	—	—	—
VSS	Platform and Core Ground	K2	—	—	—
VSS	Platform and Core Ground	K9	—	—	—
VSS	Platform and Core Ground	K11	—	—	—
VSS	Platform and Core Ground	K13	—	—	—
VSS	Platform and Core Ground	L10	—	—	—
VSS	Platform and Core Ground	L12	—	—	—
VSS	Platform and Core Ground	L14	—	—	—
VSS	Platform and Core Ground	L16	—	—	—
VSS	Platform and Core Ground	M4	—	—	—
VSS	Platform and Core Ground	M9	—	—	—
VSS	Platform and Core Ground	M11	—	—	—
VSS	Platform and Core Ground	M13	—	—	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	M15	—	—	—
VSS	Platform and Core Ground	M24	—	—	—
VSS	Platform and Core Ground	N2	—	—	—
VSS	Platform and Core Ground	N10	—	—	—
VSS	Platform and Core Ground	N12	—	—	—
VSS	Platform and Core Ground	N14	—	—	—
VSS	Platform and Core Ground	N16	—	—	—
VSS	Platform and Core Ground	N22	—	—	—
VSS	Platform and Core Ground	P9	—	—	—
VSS	Platform and Core Ground	P11	—	—	—
VSS	Platform and Core Ground	P13	—	—	—
VSS	Platform and Core Ground	P15	—	—	—
VSS	Platform and Core Ground	P17	—	—	—
VSS	Platform and Core Ground	R25	—	—	—
VSS	Platform and Core Ground	R24	—	—	—
VSS	Platform and Core Ground	R16	—	—	—
VSS	Platform and Core Ground	R14	—	—	—
VSS	Platform and Core Ground	R4	—	—	—
VSS	Platform and Core Ground	R10	—	—	—
VSS	Platform and Core Ground	R12	—	—	—
VSS	Platform and Core Ground	T2	—	—	—
VSS	Platform and Core Ground	T9	—	—	—
VSS	Platform and Core Ground	T11	—	—	—
VSS	Platform and Core Ground	T13	—	—	—
VSS	Platform and Core Ground	T15	—	—	—
VSS	Platform and Core Ground	T17	—	—	—
VSS	Platform and Core Ground	T22	—	—	—
VSS	Platform and Core Ground	U14	—	—	—
VSS	Platform and Core Ground	U16	—	—	—
VSS	Platform and Core Ground	U10	—	—	—
VSS	Platform and Core ground	U12	—	—	—
VSS	Platform and Core Ground	V4	—	—	—
VSS	Platform and Core Ground	W22	—	—	—
VSS	Platform and Core Ground	W2	—	—	—
VSS	Platform and Core Ground	AA24	—	—	—
VSS	Platform and Core Ground	AA20	—	—	—

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	AA11	—	—	—
VSS	Platform and Core Ground	AB2	—	—	—
VSS	Platform and Core Ground	AB8	—	—	—
VSS	Platform and Core Ground	AB13	—	—	—
VSS	Platform and Core Ground	AB16	—	—	—
VSS	Platform and Core Ground	AB19	—	—	—
VSS	Platform and Core Ground	AB20	—	—	—
VSS	Platform and Core Ground	AC4	—	—	—
VSS	Platform and Core Ground	AC21	—	—	—
VSS	Platform and Core Ground	AD2	—	—	—
VSS	Platform and Core Ground	AD10	—	—	—
VSS	Platform and Core Ground	AD12	—	—	—
VSS	Platform and Core Ground	AD15	—	—	—
VSS	Platform and Core Ground	AD18	—	—	—
VSS	Platform and Core Ground	AD21	—	—	—
VSS	Platform and Core Ground	AD24	—	—	—
VSS	Platform and Core Ground	AE25	—	—	—
VSS	Platform and Core Ground	AE1	—	—	—
VSS	Platform and Core Ground	AE4	—	—	—
No Connect					
NC	No connect	AB11	—	—	12
NC	No connect	AE10	—	—	12
NC	No connect	AD19	—	—	12
NC	No connect	AD20	—	—	12
NC	No connect	AC20	—	—	12
NC	No connect	AE14	—	—	12

Table 1. BSC9131 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
NC	No connect	AE20	—	—	12
NC	No connect	K23	—	—	12

1 This is a test signal for factory use only and must be pulled up (with 100 Ω –1 kΩ) to OVDD for normal operation.

2 This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed.

3 This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

4 This pin must NOT be pulled down during power-on reset.

5 This pin is an open-drain signal.Recommend that a pull-up resistor (1 kΩ to 4.7 kΩ) be placed on this pin to the respective power supply.

6 This pin should be pulled down to VSS with 10 kΩ.

7 POV_{DD2} and POV_{DD3} are always tied to GND. See section Section 2.2, “Power Sequencing,” for more details.

8 This pin may be connected to a temperature diode monitoring device such as the Analog Devices, ADT7461A™ or similar. If a temperature diode monitoring device will not be connected, these pins may be connected to test point or left as a no connect.

9 Pin should be pulled high or low depending on the JTAG topology selected. Refer to Section 3.9, “JTAG Configuration Signals.”

10 This pin should be tied to GND/VSS when MAPLE is powered down, otherwise it should be tied to OVDD. Also with MAPLE module off, AIC (RF interfaces) and SPI2 modules are disabled.

11 .It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ pull-down resistor. However, if thesignal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull-up or active driver is needed.

12 Do not connect.These pins should be left floating.

13 These pins are connected to the same global power and ground (VDD, VDDC and GND) nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function.

14 Recommend that a weak pull-up resistor (4.7 kΩ to 20 kΩ) be placed on this pin to the respective power supply.

15 Recommend that a weak pull-down resistor (4.7 kΩ) be placed on this pin.

16 Recommend that a weak pull-up resistor (10 to 100 kΩ) be placed on this pin to the respective power supply.

17 MDIC00 is grounded through an 36.5 Ω precision 1% resistor and MDIC01 is connected to GVDD through an 36.5 Ω precision 1% resistor. These pins are used for automatic calibration of the DDR3/DDR3L IOs.

18 Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin.

19 When TEST_SEL_B is low the SPI2 I/F is disable.

20 Reset configuration default value is 1due to weak internal pull-up.

21 Reset configuration value doesn’t have default.

22 Recommend that a weak pull-up resistor (4.7 kΩ to 20 kΩ) be placed on this pin to the respective power supply if it connected to an external device.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Note
Platform supply voltage	V_{DDC}	–0.3 to 1.05	V	—
MAPLE-B2F supply voltage	V_{DD}	–0.3 to 1.05	V	—
PLL supply voltage	AV_{DD_CORE} AV_{DD_DDR} AV_{DD_PLAT} AV_{DD_DSP} AV_{DD_RF}	–0.3 to 1.05	V	2
Fuse programming supply	POV_{DD1}	–0.3 to 1.65	V	—
DDR3/DDR3L DRAM I/O voltage	GV_{DD}	–0.3 to 1.65 –0.3 to 1.45	V	—
Three-speed Ethernet, Ethernet management (eTSEC) and 1588, USB	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
IFC, eSDHC, USIM, TDM	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	3
DUART1, SYSCLK, system control and power management, I^2C1, PWM2, clocking, I/O voltage select, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
USB, eSPI1, DUART2, I^2C2, USIM, PWM1	CV_{DD}	–0.3 to 3.63 –0.3 to 1.98	V	3, 4
eSPI3, eSPI4, RF parallel interface	$X1V_{DD}$	–0.3 to 3.63 –0.3 to 1.98	V	—
eSPI2, USB, TDM, RF parallel interface	$X2V_{DD}$	–0.3 to 3.63 –0.3 to 1.98	V	—
RF serial MaxPHY interface	RV_{DD}	–0.3 to 1.65	V	—

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR3/DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	5, 10
	DDR3/DDR3L DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2 + 0.3)	V	10
	Ethernet, USB signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	6, 10
	IFC, eSDHC, USIM, TDM signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	—	7, 10
	DUART1, SYSCLK, system control and power management, I^2C1, PWM2, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	8, 10
	USB, eSPI1, DUART2, I^2C2, USIM, PWM1	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 10
	eSPI3, eSPI4, RF parallel interface	$X1V_{IN}$	–0.3 to ($X1V_{DD}$ + 0.3)	V	9, 10
	eSPI2, USB, TDM, RF parallel interface	$X2V_{IN}$	–0.3 to ($X2V_{DD}$ + 0.3)	V	9, 10
	RF serial MaxPHY interface	RV_{IN}	–0.3 to (RV_{DD} + 0.3)	V	10
Storage temperature range		T_{STG}	–55 to 150	°C	—

Note:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. AV_{DD} is measured at the input to the filter and not at the pin of the device.
3. USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.
4. Caution: CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Caution: LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. Caution: $X[1\text{-}2]V_{IN}$ must not exceed $X[1\text{-}2]V_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. $(C,X,B,G,L,O,R)V_{DD}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Note
Platform supply voltage	V_{DDC}	1 + 50 mV / – 30mV	V	1
MAPLE-B2F supply voltage	V_{DD}	1 + 50 mV / – 30mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
PLL supply voltage		AV_{DD_CORE} AV_{DD_DDR} AV_{DD_PLAT} AV_{DD_DSP} AV_{DD_RF}	1 + 50 mV / – 30mV	V	1
Fuse supply voltage		POV_{DD1}	1.5 V ± 75 mV	V	1
DDR3 DRAM I/O voltage		GV_{DD}	1.5 V ± 75 mV	—	—
DDR3L DRAM I/O voltage		GV_{DD}	1.35 V +100mV/ –67mV	—	—
Three-speed Ethernet, Ethernet management (eTSEC) and 1588, USB		LV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
DUART1, SYSCLK, system control and power management, I^2C1, PWM2, clocking, I/O voltage select, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
IFC, eSDHC, USIM, TDM		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	2
USB, eSPI1, DUART2, I^2C2, USIM, PWM1		CV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	2
eSPI3, eSPI4, RF parallel interface		$X1V_{DD}$	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
eSPI2, USB, TDM, RF parallel interface		$X2V_{DD}$	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
RF serial MaxPHY Interface		RV_{DD}	1.5 V ± 75 mV	V	—
Input voltage	DDR3/DDR3L DRAM	MV_{IN}	GND to GV_{DD}	V	—
	DDR3/DDR3L DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Ethernet, USB	LV_{IN}	GND to LV_{DD}	V	—
	IFC, eSDHC, TDM signals	BV_{IN}	GND to BV_{DD}	V	—
	DUART1, SYSCLK, system control and power management, eSPI, I^2C1, USIM, PWM2, clocking, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	—
	USB, eSPI, eSDHC, DUART2, I^2C2, USIM, PWM1	CV_{IN}	GND to CV_{DD}	V	—
	eSPI3, eSPI4, RF parallel interface	$X1V_{IN}$	GND to $X1V_{DD}$	V	—
	eSPI2, USB, TDM, RF parallel interface	$X2V_{IN}$	GND to $X2V_{DD}$	V	—
	RF serial MaxPHY interface	RV_{IN}	GND to RV_{DD}	V	—
Maximum input capacitance		C_{INMAX}	10	pF	3

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
Operating Temperature range	Standard	T_A/T_J	T_A = 0 (min) to T_J = 105 (max)	°C	—
	Extended	T_A/T_J	T_A = –40 (min) to T_J = 105 (max)	°C	—
	Secure boot fuse programming	T_A/T_J	T_A = 0 (min) to T_J = 70 (max)	°C	1

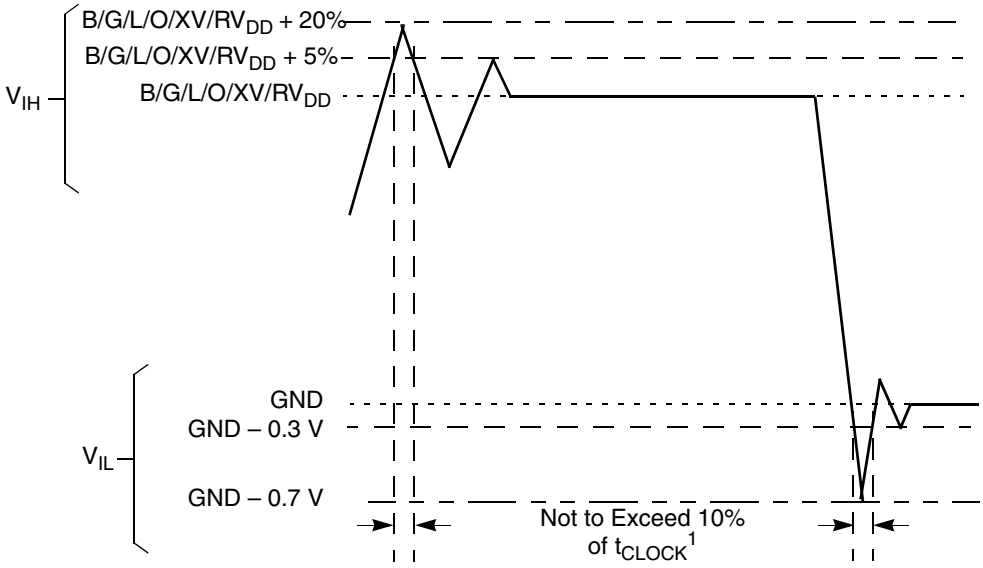
Note:

1 **Caution:** POV_{DD1} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD1} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Sequencing."

2 USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.

3 Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.

This figure shows the undershoot and overshoot voltages at the interfaces.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references TSEC*n*_GTX_CLK125.
   For IFC, t_{CLOCK} references IFC_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/X1V_{DD}/X2V_{DD}/RV_{DD}$

The core voltage must always be provided at nominal 1 V (see Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR3 SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage	Note
IFC, GPIO[0:7], eSDHC, TDM	47 ± 7	BV_{DD} = 3.3/2.5/1.8 V	—
DDR3 (programmable)	16 32 (half strength mode)	GV_{DD} = 1.5 V DDR3 GV_{DD} = 1.35 V DDR3L	1
eTSEC, USB	47 ± 7	LV_{DD} = 3.3/2.5 V	—
DUART1, system control, I^2C1, USIM, PWM2, JTAG	47 ± 7	OV_{DD} = 3.3 V	2
USB, eSPI1, DUART2, I^2C2, USIM, PWM1	47 ± 7	CV_{DD} = 3.3/1.8 V	2
eSPI3, eSPI4, RF parallel interface	LVCMOS	$X1V_{DD}$ = 3.3/1.8 V	—
eSPI2, USB, TDM, RF parallel interface	—	$X2V_{DD}$ = 3.3/1.8 V	—
RF serial MaxPHY interface, DDR3 I/O	20 (full strength mode) 40 (half strength mode)	RV_{DD} = 1.5 V	—

Note:

1. The drive strength of the DDR3 interface in half-strength mode is at T_j = 125°C and at GV_{DD} (min).
2. USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. VDD, VDDC, AVDD (all PLL supplies)
2. LVDD, BVDD, CVDD, OVDD, X1VDD, X2VDD, GVDD
3. For secure boot fuse programming: After deassertion of HRESET_B, drive POV_{DD1} = 1.5 V after a required minimum delay per Table 5. After fuse programming is completed, it is required to return POV_{DD1} = GND before the system is power cycled (HRESET_B assertion) or powered down (V_{DDC} ramp down) per the required timing specified in Table 5. See Section 3.11, "Security Fuse Processor," for additional details.

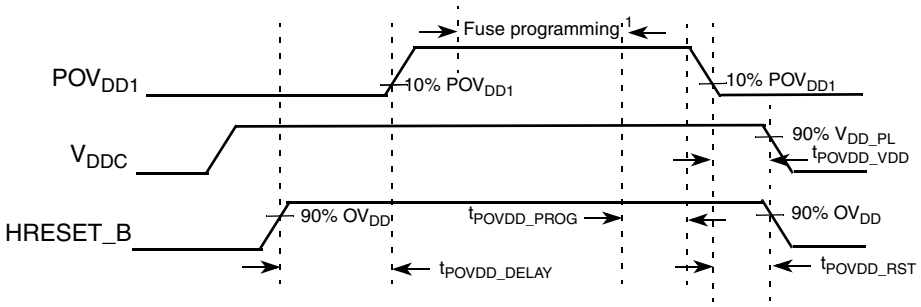
WARNING

Only 100,000 POR cycles are permitted per lifetime of a device. Only one secure boot fuse programming event is permitted per lifetime of a device.

No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND.

POV_{DD2} and POV_{DD3} are always tied to GND.

This figure provides the POV_{DD1} timing diagram.



NOTE: POVDD must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD1} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD1}.

Table 5. POV_{DD1} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	1500	—	t_{SYSCLK}	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the deassertion of HRESET_B to driving POV_{DD1} ramp up. Delay measured from HRESET_B deassertion at 90% OV_{DD} to 10% POV_{DD1} ramp up.
2. Delay required from fuse programming finished to POV_{DD1} ramp down start. Fuse programming must complete while POV_{DD1} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND. After fuse programming is completed, it is required to return POV_{DD1} = GND.
3. Delay required from POV_{DD1} ramp down complete to V_{DDC} ramp down start. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before V_{DDC} is at 90% V_{DDC}.
4. Delay required from POV_{DD1} ramp down complete to HRESET_B assertion. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before HRESET_B assertion reaches 90% OV_{DD}.
5. Only one secure boot fuse programming event is permitted per lifetime of a device.

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, the sequencing for GV_{DD} is not required.

2.3 Power-Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

2.4 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. Table 6 provides the RESET initialization AC timing specifications.

Table 6. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Note
Required assertion time of HRESET_B	600	—	µs	1, 2, 5
Minimum assertion time of TRESET_B simultaneous to HRESET_B assertion	25	—	ns	3
Minimum assertion time for SRESET_B	3	—	t_{SYSCLK}	4
PLL input setup time with stable SYSCLK before HRESET_B negation	25	—	µs	—
Input setup time for POR configurations (other than PLL configuration) with respect to negation of HRESET_B	4	—	t_{SYSCLK}	4
Input hold time for all POR configurations (including PLL configuration) with respect to negation of HRESET_B	2	—	t_{SYSCLK}	4
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of HRESET_B	—	8	t_{SYSCLK}	4

Note:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. TRST is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in Section 3.9.1, “Termination of Unused Signals.”
4. SYSCLK is the primary clock input.
5. Reset initialization should start only after all power supplies are stable.

This table provides the PLL lock times.

Table 7. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	µs	—

2.5 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. Table 8 provides the power supply ramp rate specifications.

Table 8. Power Supply Ramp Rate

Parameter	Min	Max	Unit
Required ramp rate	—	36000	V/s
Required ramp time	—	50	ms

Table 8. Power Supply Ramp Rate (continued)

Parameter	Min	Max	Unit

Note:
1. Ramp rate is specified as a linear ramp from 10 to 90% of the nominal voltage of the specific voltage supply.
2. All MCKE signals must remain low during the power up sequence.

2.6 Power Characteristics

This table shows the power dissipations of the V_{DDC} and V_{DD} supplies for various operating DSP and core complex bus clock (CCB_clk) frequencies versus the core and DDR clock frequencies.

Table 9. Core Power Dissipation

Power Mode	PA Core Frequency (MHz)	DSP Core Frequency (MHz)	CCB Frequency (MHz)	PA DDR Frequency (MHz)	V_{DDC} Core (V)	V_{DD} MAPLE (V)	Junction Temp (°C)	V_{DDC} +V_{DD} Power (W)	Note
Typical	1000	1000	500	800	1.0	1.0	65	3.4	1, 2
Thermal							105	5.0	1, 3, 5
Maximum								5.9	1, 4, 5
Typical	800	800	400	800	1.0	1.0	65	3.0	1, 2
Thermal							105	4.4	1, 3, 5
Maximum								5.2	1, 4, 5

Note:
1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured while running a typical use case, using the *nominal* process and *recommended* core and platform (V_{DDC}) and MAPLE (V_{DD}) voltages at 65 °C junction temperature (see Table 3).
3. Thermal power is the power measured while running a 70% (cores) and 50% (platform) utilization case, using the *worst case* process and *recommended* core and platform (V_{DDC}) and MAPLE (V_{DD}) voltages at maximum operating junction temperature (see Table 3).
4. Maximum power is the maximum power measured while running a maximum power pattern, using the *worst case* process and *recommended* core and platform (V_{DDC}) and MAPLE (V_{DD}) voltages at maximum operating junction temperature (see Table 3).
5. An estimated I/O power while running a typical use case, using the *nominal* process and *recommended* voltages of 1 W (see Table 3).

Table 10. I/O Power

PS#	Primary pin name	Pin width	Voltage domain	Recommended value	Current max	Typical current (A)	Max (A)	Note
I/O	OVDD	37	General I/O supply	3.3V		0.178	0.266	—
	BVDD	46	Local Bus and GPIO I/O supply	1.8V/ 2.5V/ 3.3V		0.097	0.148	3
	LVDD	32	TSEC I/O supply	3.3V/ 2.5V		0.051	0.076	3
	CVDD	19	ULPI/SPI/UART/SIM I/O supply	3.3V/ 1.8V		0.030	0.045	3
	GVDD		DDR I/O supply	1.5V/ 1.35V		0.710	0.950	1, 2, 3
	X1VDD		ANT1I/O supply	3.3V/ 1.8V		0.098	0.140	3
	X2VDD		ANT2, ANT3 I/O supply	3.3V/ 1.8V		0.098	0.140	3

Table 10. I/O Power (continued)

PS#	Primary pin name	Pin width	Voltage domain	Recommended value	Current max	Typical current (A)	Max (A)	Note
Analog	AVDD_CORE		Core PLL supply	1.0 V		0.005	0.015	—
	AVDD_PLAT		Platform PLL supply					—
	AVDD_DDR		DDR PLL supply					—

Note:

1 For DDR typical, it is 40% DIMM utilization.

2 For DDR max, it is 75% DIMM utilization.

3 For I/O with different possible voltages, the currents listed above are for the higher voltage.

2.7 Input Clocks

This section provides information about the system clock specifications, spread spectrum sources, real time clock specifications, eTSEC gigabit reference clock specifications, TDM clock specifications, and other input sources.

2.7.1 System Clock and DDR Clock Specifications

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) 3.3 V DC specifications.

Table 11. SYSCLK/DDRCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) AC timing specifications.

Table 12. SYSCLK/DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	66	—	100	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DDRCLK frequency	f_{DDRCLK}	66	—	166	MHz	1
DDRCLK cycle time	t_{DDRCLK}	6.0	—	15.15	ns	—
SYSCLK/DDRCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK/DDRCLK slew rate	—	1	—	4	V/ns	3

Table 12. SYSCLK/DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK/DDRCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK/DDRCLK jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.2 DSP Clock (DSPCLKIN) Specifications

This table provides the DSP clock (DSPCLKIN) 3.3 V DC specifications.

Table 13. DSPCLKIN DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the DSP clock (DSPCLKIN) AC timing specifications.

Table 14. DSPCLKIN AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
DSPCLKIN frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
DSPCLKIN cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DSPCLKIN duty cycle	t_{KHK}/ t_{SYSCLK}	40	—	60	%	2
DSPCLKIN slew rate	—	1	—	4	V/ns	3
DSPCLKIN peak period jitter	—	—	—	±150	ps	—
DSPCLKIN jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Table 14. DSPCLKIN AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note

Note:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DSPCLKIN frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.3 Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet this device's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the device is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 15. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

Parameter	Min	Max	Unit	Note
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 95.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device

CAUTION

The processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

2.7.4 Real Time Clock Specifications

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.7.5 eTSEC Gigabit Reference Clock Specifications

Table 16 lists the eTSEC gigabit reference clock DC electrical characteristics.

Table 16. eTSEC Gigabit Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	±40	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

Table 17 provides the eTSEC gigabit reference clocks (TSEC*n*_GTX_CLK125) AC timing specifications.

Table 17. TSEC*n*_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
TSEC*n*_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
TSEC*n*_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	—	—	0.75	ns	1
TSEC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	—	53	%	2
TSEC*n*_GTX_CLK125 jitter	—	—	—	±150	ps	2

Note:
1. Rise and fall times for TSEC*n*_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 .
2. TSEC*n*_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The TSEC*n*_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.11.1.2, “RMII and RGMII AC Timing Specifications,” for the duty cycle for 10Base-T and 100Base-T reference clock.

2.7.6 RF Parallel Interface Clock Specifications

The following table lists the RF parallel interface clock DC electrical characteristics.

Table 18. RF Parallel Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	C	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following table lists the RF parallel interface clock AC electrical characteristics.

Table 19. RF Parallel Reference Clock AC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
ANT_REF_CLK frequency	$f_{ANT\_REF\_CLK}$	—	19.2	—	MHz	—
ANT_REF_CLK cycle time	$t_{ANT\_REF\_CLK}$	—	52	—	ns	—
ANT_REF_CLK duty cycle	$t_{KHK}/t_{ANT\_REF\_CLK}$	48	50	52	%	—
ANT_REF_CLK slew rate	—	1	—	4	V/ns	1
ANT_REF_CLK peak period jitter	—	—	—	±100	ps	—
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.

2.7.7 RF Serial (MaxPHY) Interface Clock Specifications

Table 20 lists the RF serial (MaxPHY) interface clock DC electrical characteristics.

Table 20. RF Serial (MaxPHY) Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	C	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

Table 21 lists the RF serial (MaxPHY) interface clock AC electrical characteristics.

Table 21. RF Serial (MaxPHY) Reference Clock AC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
MAX_REF_CLK frequency	$f_{MAX\_PHY\_REF\_CLK}$	19.2	—	19.6608	MHz	—
MAX_REF_CLK cycle time	$t_{MAX\_PHY\_REF\_CLK}$	50.86	—	52	ns	—
MAX_REF_CLK duty cycle	$t_{KHK}/t_{MAX\_PHY\_REF\_CLK}$	48	50	52	%	—
MAX_REF_CLK slew rate	—	1	—	4	V/ns	1
MAX_REF_CLK peak period jitter	—	—	—	±100	ps	—
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.

2.7.8 Other Input Clocks

A description of the overall clocking of this device is available in the *BSC9131QorIQ Qonverge Multicore Baseband Processor Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such asEthernet Management, eSDHC, and IFC, see the specific interface section.

2.8 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V and 1.35 V when interfacing to DDR3 or DDR3L SDRAM, respectively.

2.8.1 DDR3 and DDR3L SDRAM Interface DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 22. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.5 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF*n* may not exceed ±1% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 μA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 23. DDR3L SDRAM Interface DC Electrical Characteristics

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MVREF*n*	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MVREF*n* + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MVREF*n* – 0.090	V	5
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.3	mA	6, 7
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	6, 7
I/O leakage current	I_{OZ}	–50	50	μA	8

Table 23. DDR3L SDRAM Interface DC Electrical Characteristics (continued)

At recommended operating condition with GV_{DD} = 1.35 V[1]

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MVREF*n* is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver.Peak-to-peak noise on MVREFn may not exceed the MVREFn DC level by more than ±1% of GV_{DD} (i.e. ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MVREF*n* with a min value of MVREF*n* – 0.04 and a max value of MVREF*n* + 0.04. V_{TT} should track variations in the DC level of MVREF*n*.
4. The voltage regulator for MVREF*n* must be able to supply up to125 µA current.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. IOH and IOL are measured at GV_{DD} = 1.282 V
7. See the IBIS model for the complete output IV curve characteristics.
8. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the DDR controller interface capacitance for DDR3.

Table 24. DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, DQS_B	C_{IO}	6	8	pF	—
Delta input/output capacitance: DQ, DQS, DQS_B	C_{DIO}	—	0.5	pF	—

This table provides the current draw characteristics for MVREF*n*.

Table 25. Current Draw Characteristics for MVREF*n*

For recommended operating conditions, seeTable 3.

Parameter	Symbol	Min	Max	Unit	Note
Current draw for DDR3 SDRAM for MVREF*n*	I_{MVREFn}	—	700	µA	—
Current draw for DDR3L SDRAM for MVREF*n*	I_{MVREFn}	—	700	µA	—

2.8.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM, and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 26. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.175	V	—

Table 26. DDR3 SDRAM Interface Input AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	V_{IHAC}	MVREF*n* + 0.175	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 27. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{ILAC}	—	MVREF*n* – 0.160	V	—
AC input high voltage	V_{IHAC}	MVREF*n* + 0.160	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3/3L SDRAM.

Table 28. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
800 MHz data rate		–200	200		
667 MHz data rate		–240	240		
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}	—	—	ps	2
800 MHz data rate		–425	425		
667 MHz data rate		–510	510		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

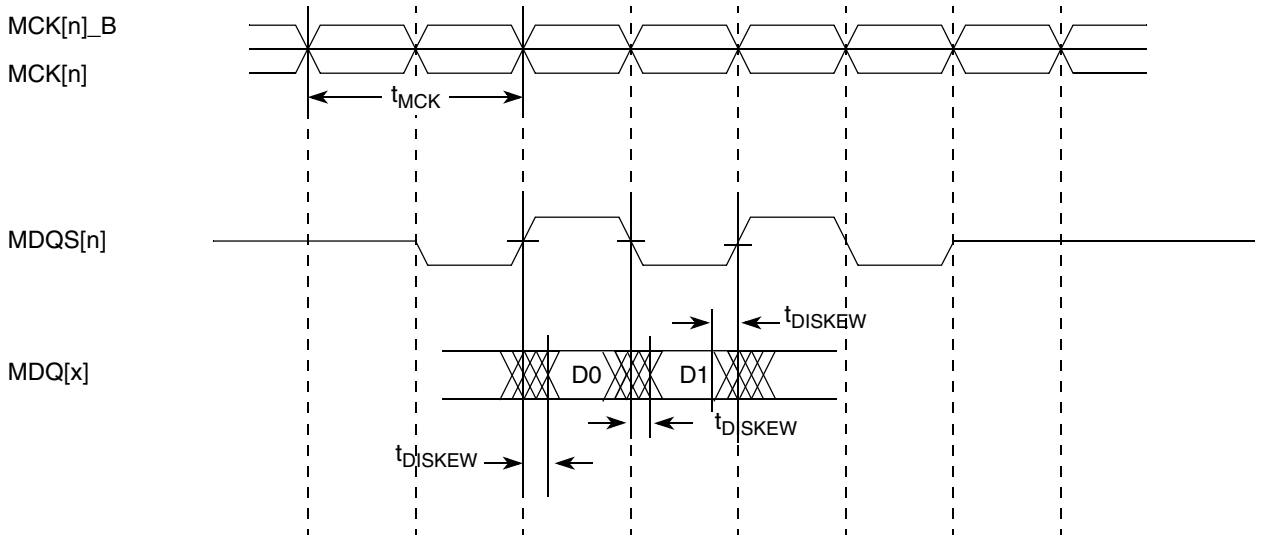


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

2.8.2.2 DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR3 and DDR3L SDRAM interface.

Table 29. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK[n] cycle time	t_{MCK}	2.5	3	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCS[n]_B output setup with respect to MCK	t_{DDKHCS}			ns	3
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCS[n]_B output hold with respect to MCK	t_{DDKHCX}			ns	3
800 MHz data rate		0.917	—		
667 MHz data rate		1.10	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
800 MHz data rate		–0.375	0.375		
667 MHz data rate		–0.6	0.6		

Table 29. DDR3 and DDR3L SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
800 MHz data rate		375	—		
667 MHz data rate		450	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 29, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

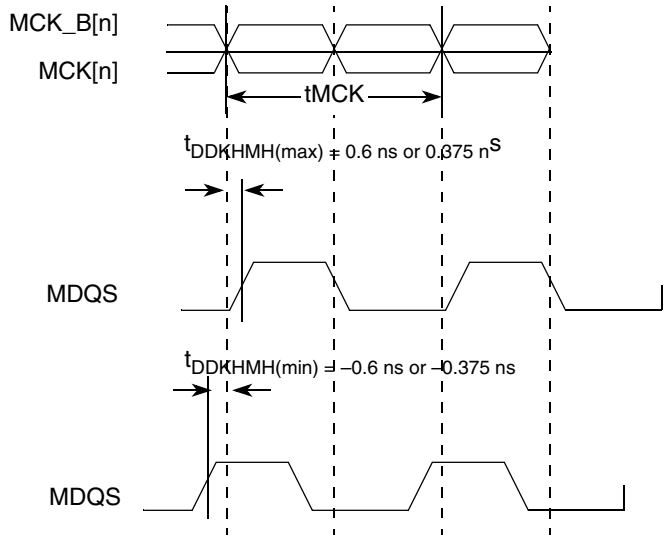


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

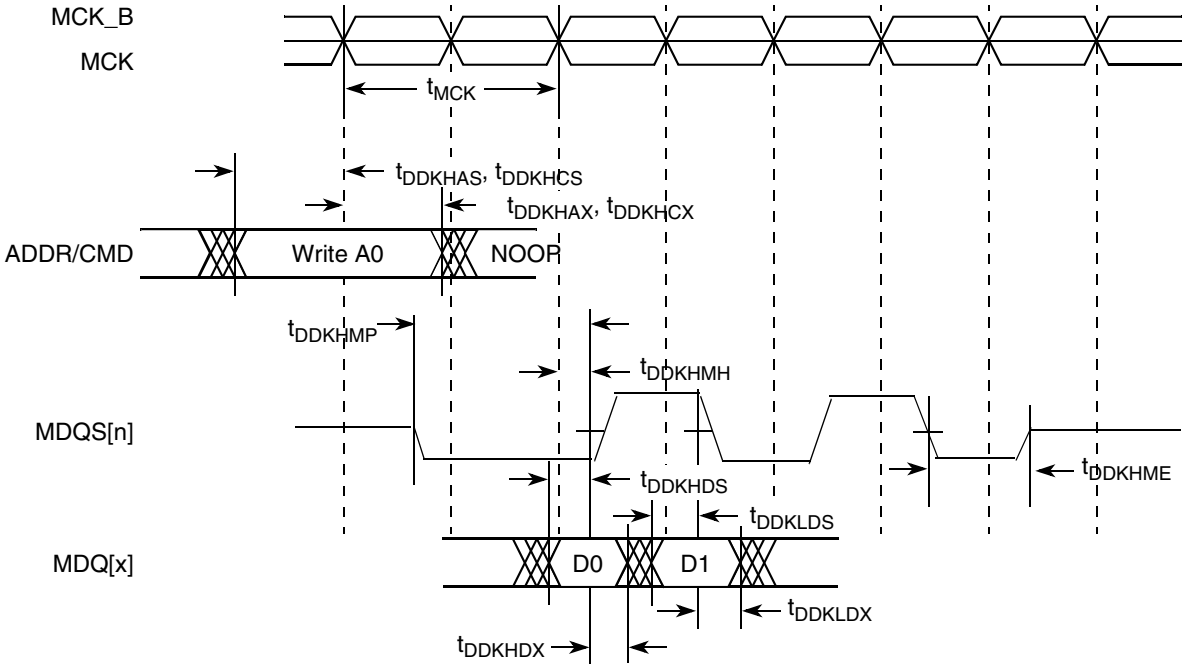


Figure 11. DDR3 and DDR3L Output Timing Diagram

This figure provides the AC test load for the DDR3 and DDR3Lcontroller bus.

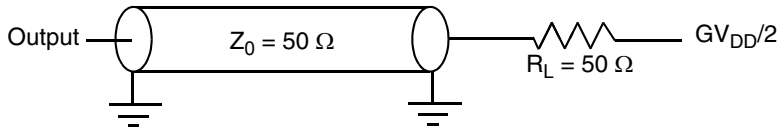


Figure 12. DDR3 and DDR3L Controller Bus AC Test Load

2.8.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

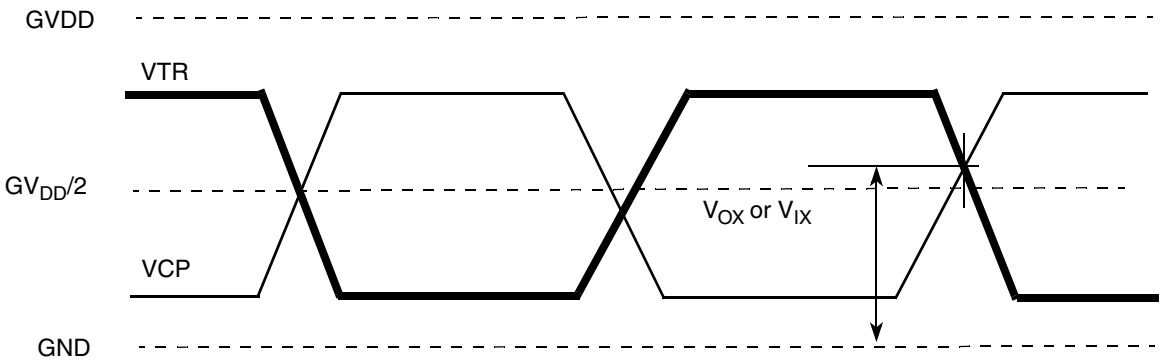


Figure 13. DDR3, and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as MCK_B or MDQS_B).

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 30. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.150$	$0.5 \times GV_{DD} + 0.150$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.115$	$0.5 \times GV_{DD} + 0.115$	V	1

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 31. DDR3L SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.135$	$0.5 \times GV_{DD} + 0.135$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.105$	$0.5 \times GV_{DD} + 0.105$	V	1

Note:
1. I/O drivers are calibrated before making measurements.

2.9 eSPI

This section describes the DC and AC electrical specifications for the SPI.

2.9.1 eSPI1 DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI1 on the device operating on a 3.3 V power supply.

Table 32. eSPI1 DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD})	I_{IN}	—	±10	μA	2
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 6.0 mA)	V_{OL}	—	0.5	V	—
Output low voltage (IOL = 3.2 mA)	V_{OL}	—	0.4	V	—

Note:

1 The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2 The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the eSPI1, eSPI2, eSPI3, and eSPI4 on the device operating on a 1.8 V power supply.

Table 33. eSPI DC Electrical Characteristics (CV_{DD}, $X2V_{DD}$, $X1V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD}/$X2V_{DD}$/$X1V_{DD}$)	I_{IN}	—	±40	μA	2, 3
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	1.35	—	V	—
Output low voltage (I_{OL} = 6.0 mA)	V_{OL}	—	0.4	V	—

Note:

1 The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2 The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

3 eSPI1 is powered on CV_{DD}, SPI2 is on $X2V_{DD}$, SPI3 and SPI4 are on $X1V_{DD}$ (see Table 3).

2.9.2 eSPI1 AC Timing Specifications

This table provides the eSPI1 input and output AC timing specifications.

Table 34. eSPI1 AC Timing Specifications

For recommended operating conditions, see Table 3.

Characteristic	Symbol[1]	Min	Max	Unit	Note
eSPI outputs—Master data (internal clock) hold time	t_{NIKHOX}	0.5 + ($t_{PLATFORM\_CLK}$/2)	—	ns	2
eSPI outputs—Master data (internal clock) delay	t_{NIKHOV}	—	6.0 + ($t_{PLATFORM\_CLK}$/2)	ns	2
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

This figure provides the AC test load for eSPI1.

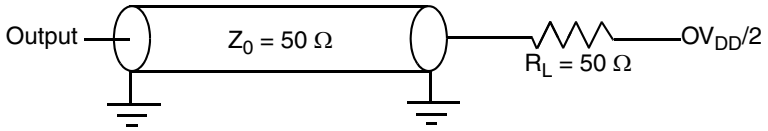


Figure 14. eSPI1 AC Test Load

This figure represents the AC timing from Table 34 in master mode (internal clock). Note that although the specifications are generally refer to the rising edge of the clock, Figure 14 also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI1.

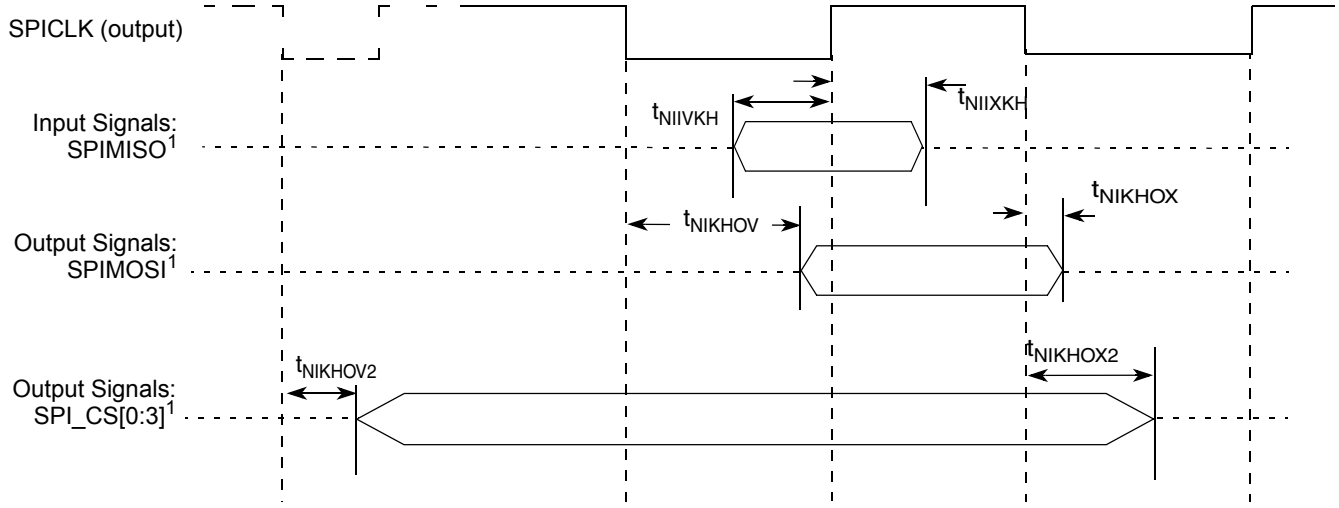


Figure 15. eSPI1 AC Timing in Master Mode (Internal Clock) Diagram

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interfaces.

2.10.1 DUART DC Electrical Characteristics

Table 35 and Table 37 provide the DC electrical characteristics for the two DUARTs on the device, which correspond to four UART interfaces. DUART1 is powered by OV_{DD}, while DUART2 is powered by the CV_{DD}.

This table provides the DC timing parameters for the DUART interface operating from a 3.3 V power supply.

Table 35. DUART DC Electrical Characteristics (OV_{DD}, CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN}/CV_{IN} = 0 V or OV_{IN}/CV_{IN} = OV_{DD}/CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD}/CV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD}/CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN}/CV_{IN} values found in Figure 3.
2. Note that the symbol OV_{IN}/CV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

This table provides the DC timing parameters for the DUART interface operating from a 1.8 V power supply.

Table 36. DUART DC Electrical Characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (CV_{IN} = 0 V or CV_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Figure 3.
2. Note that the symbol CV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

2.10.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 37. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Note:

1. CCB clock refers to the platform clock.
2. Actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet10/100/1000 controller and MII management.

2.11.1 RMII/RGMII Interface Electrical Specifications

This section provides AC and DC electrical characteristics of RMII/RGMII interface for eTSEC.

2.11.1.1 RMII and RGMII DC Electrical Characteristics

Table 38 presents the RGMII/RMII DC timing specifications.

Table 38. RGMII/RMII DC Electrical Characteristics (LV_{DD} = 3.3 V)

At recommended operating conditions with LV_{DD} = 3.3 V

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	—
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	50	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–50	—	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

Table 39 shows the RGMII/RMII DC electrical characteristics when operating from a 2.5 V supply.

Table 39. RGMII/RMII DC Electrical Characteristics (LV_{DD} = 2.5 V)

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	—	V	1
Input low voltage	V_{IL}	—	0.70	V	1
Input high current (V_{IN} = LV_{DD})	I_{IH}	—	50	μA	2
Input low current (V_{IN} = GND)	I_{IL}	–50	—	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 3.

2.11.1.2 RMII and RGMII AC Timing Specifications

Table 40 presents the RMII transmit AC timing specifications.

Table 40. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMT}	—	20.0	—	ns
TSEC*n*_TX_CLK duty cycle	t_{RMTH}	35	—	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	5.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	5.0	ns

Table 40. RMII Transmit AC Timing Specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
TSEC*n*_TX_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Figure 16 shows the RMII transmit AC timing diagram.

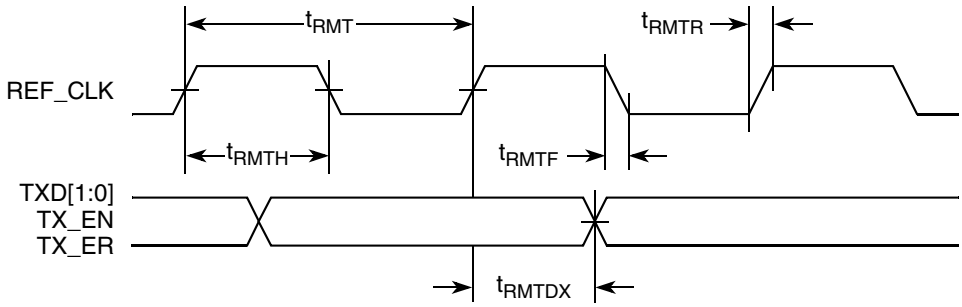


Figure 16. RMII Transmit AC Timing Diagram

Table 41 lists the RMII receive AC timing specifications.

Table 41. RMII Receive AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMR}	—	20.0	—	ns
TSEC*n*_TX_CLK duty cycle	t_{RMRH}	35	—	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMRR}	1.0	—	5.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMRF}	1.0	—	5.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to TSEC*n*_TX_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to TSEC*n*_TX_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Figure 17 provides the AC test load for eTSEC.

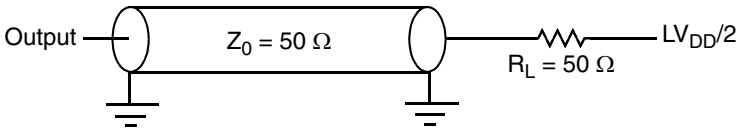


Figure 17. eTSEC AC Test Load

Figure 18 shows the RMII receive AC timing diagram.

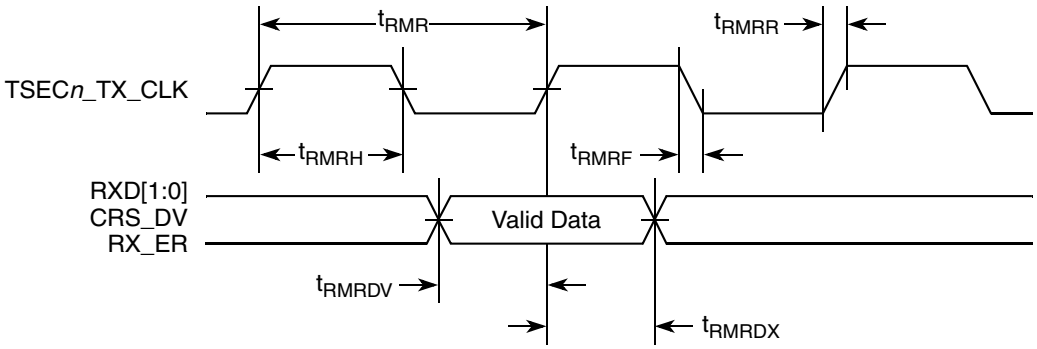


Figure 18. RMII Receive AC Timing Diagram

Table 42 presents the RGMII AC timing specifications.

Table 42. RGMII AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Note:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

Figure 19 shows the RGMII AC timing and multiplexing diagrams.

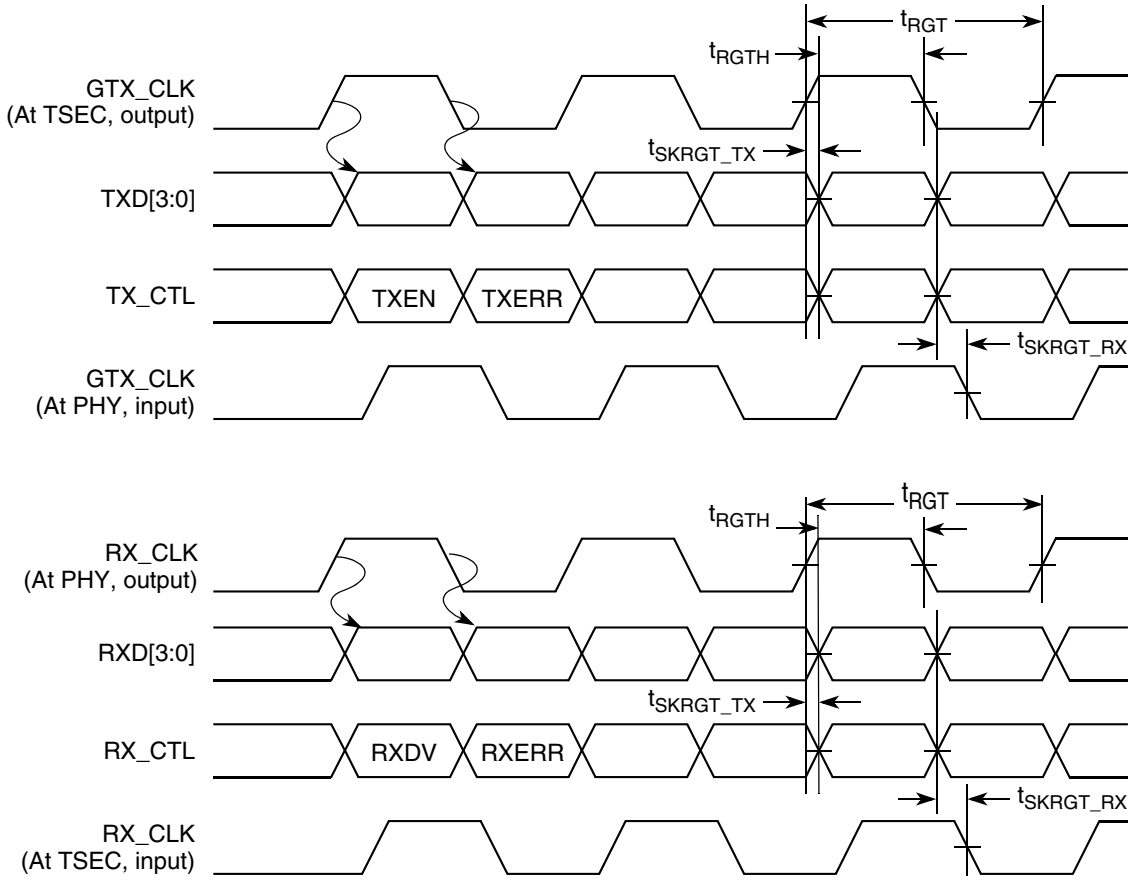


Figure 19. RGMII AC Timing and Multiplexing Diagram

2.11.2 MII Management

2.11.2.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V and 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in Table 43 and Table 44.

Table 43. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.4	V	—

Table 43. MII Management DC Electrical Characteristics (continued)

At recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

Table 44. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	10	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.11.2.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 45. MII Management AC Timing Specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Table 45. MII Management AC Timing Specifications (continued)

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

This figure shows the MII management interface timing diagram.

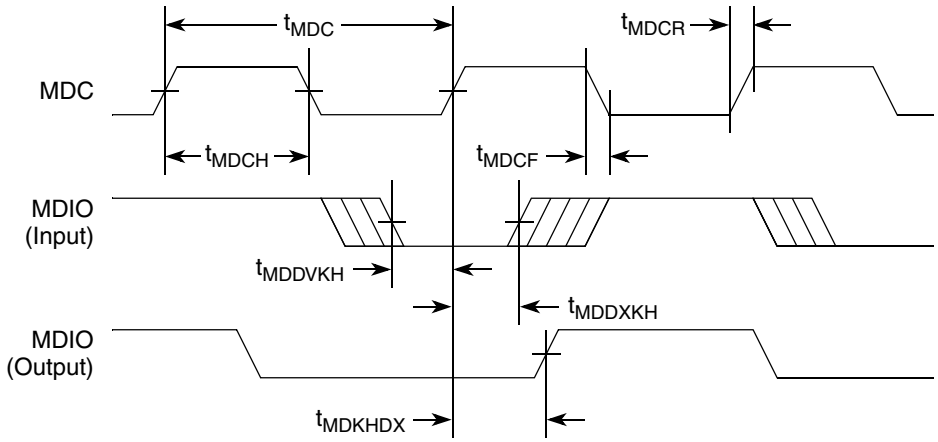


Figure 20. MII Management Interface Timing Diagram

2.11.3 eTSEC IEEE Std 1588 Electrical Specifications

2.11.3.1 eTSEC IEEE Std 1588 DC Specifications

This table shows IEEE Std 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 46. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1

Table 46. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

This table shows the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 47. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions with LV_{DD} = 2.5 V

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.70	V	—
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Note:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 2 and Table 3.

2.11.3.2 eTSEC IEEE Std 1588 AC Specifications

This table provides the IEEE Std 1588 AC timing specifications.

Table 48. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
TSEC_1588_CLK clock period	$t_{T1588CLK}$	5	—	T_{RX_CLK}*7	ns	1, 3
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}$ /$t_{T1588CLK}$	40	50	60	%	—
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$ /$t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	2*$t_{T1588CLK\_MAX}$	—	—	ns	2

Table 48. eTSEC IEEE 1588 AC Timing Specifications (continued)

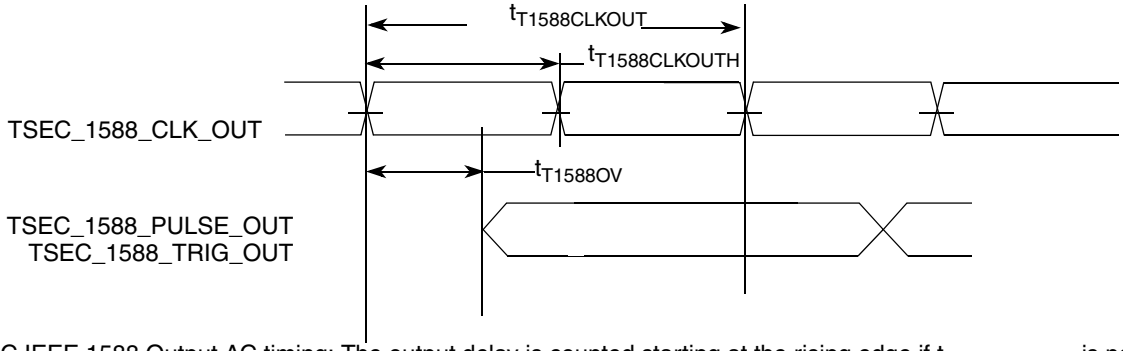
For recommended operating conditions, see Table 3

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ is 2800, 280, and 56 ns respectively.

Figure 21 shows the data and command output AC timing diagram.



[1] eTSEC IEEE 1588 Output AC timing: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 21. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

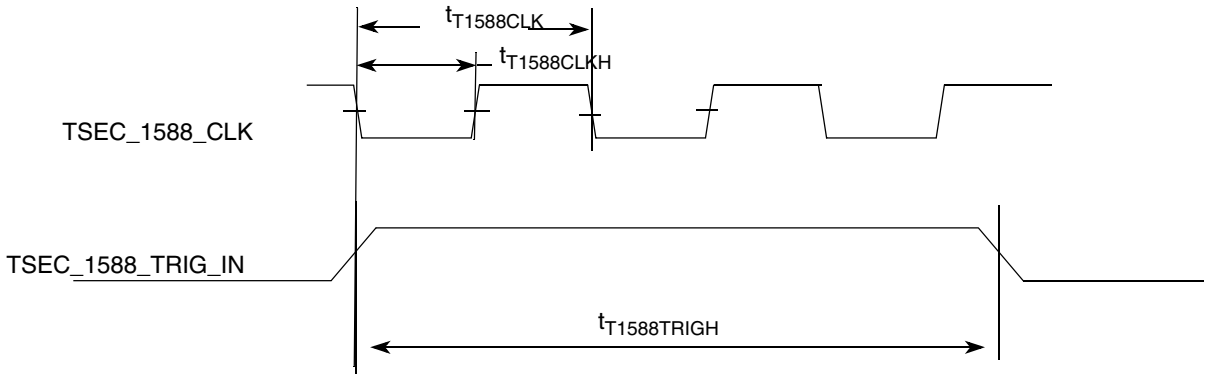


Figure 22. eTSEC IEEE 1588 Input AC Timing

2.12 USB

This section provides the AC and DC electrical specifications for the USB interface.

2.12.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the ULPI interface when operating at 3.3 V.

Table 49. USB DC Electrical Characteristics ($CV_{DD}/LV_{DD}/X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($CV_{IN}/LV_{IN}/X2V_{IN}$ = 0 V or $CV_{IN}/LV_{IN}/X2V_{IN}$ = $CV_{DD}/LV_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/LV_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage ($CV_{DD}/LV_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/LV_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol CV_{IN}, LV_{IN}, and $X2V_{IN}$ represent the input voltage of the power supplies. See Table 3.

Table 51 provides the DC electrical characteristics for the ULPI interface when operating at 2.5 V.

Table 50. USB DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. Note that the symbol LV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the ULPI interface when operating at 1.8 V.

Table 51. USB DC Electrical Characteristics ($CV_{DD}/X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($CV_{IN}/X2V_{IN}$ = 0 V or $CV_{IN}/X2V_{IN}$ = $CV_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($CV_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Table 51. USB DC Electrical Characteristics ($CV_{DD}/X2V_{DD}$ = 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.12.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 52. USB General Timing Parameters (ULPI Mode)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of the USB clock to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 23 and Figure 24 provide the USB AC test load and signals, respectively.

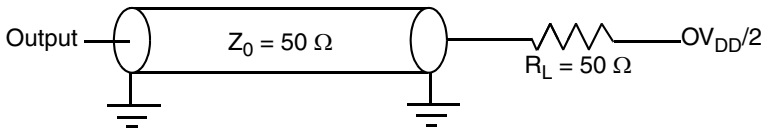


Figure 23. USB AC Test Load

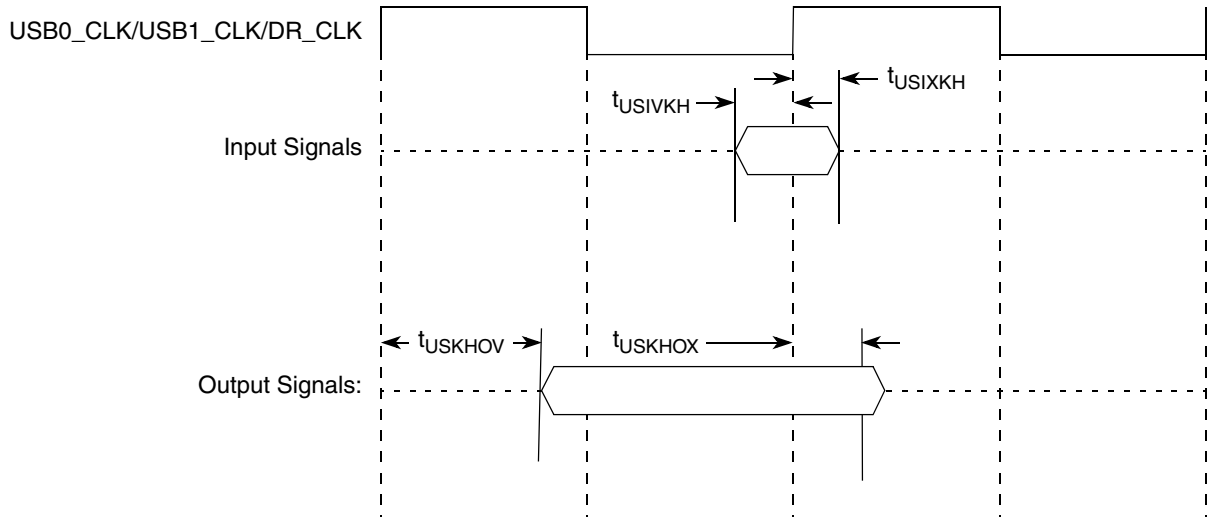


Figure 24. USB Signals

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 53. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	Steady state	$f_{USB\_CLK\_IN}$	59.97	60	60.03	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.05	0	0.05	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	200	ps

2.13 Integrated Flash Controller (IFC)

This section describes the DC and AC electrical specifications for the integrated flash controller.

2.13.1 IFC DC Electrical Characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 3.3 V.

Table 54. Integrated Flash Controller DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OL}	—	0.4	V	—

Table 54. Integrated Flash Controller DC Electrical Characteristics (3.3 V) (continued)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 2.5 V.

Table 55. Integrated Flash Controller DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the integrated flash controller when operating at BV_{DD} = 1.8 V.

Table 56. Integrated Flash Controller DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.13.2 IFC AC Timing Specifications

This section describes the AC timing specifications for the integrated flash controller.

2.13.2.1 Test Condition

This figure provides the AC test load for the integrated flash controller.

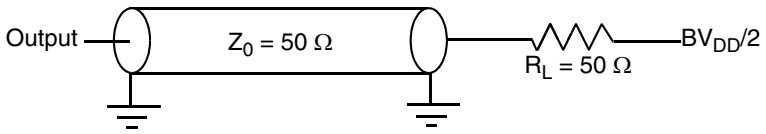


Figure 25. Integrated Flash Controller AC Test Load

2.13.2.2 IFC AC Timing Specifications

All output signal timings are relative to the falling edge of any IFC_CLK. The external circuit must use the rising edge of the IFC_CLKs to latch the data.

All input timings are relative to the rising edge of IFC_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

Table 57. IFC Timing Specifications (BV_{DD} = 3.3 V, 2.5 V, and 1.8 V)

For recommended operating conditions, see Table 3

Parameter	Symbol[1]	Min	Max	Unit	Note
IFC_CLK cycle time	t_{IBK}	10	—	ns	—
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	—
Input setup	t_{IBIVKH}	4	—	ns	—
Input hold	t_{IBIXKH}	1	—	ns	—
Output delay	t_{IBKLOV}	—	1.5	ns	—
Output hold	t_{IBKLOX}	–2	—	ns	5, 6

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of IFC_CLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different IFC_CLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{IBONOT} is a measurement of the maximum time between the negation of ALE and any change in AD when FTIM0_CSn[TEAHC] = 0.
5. Here the negative sign means output transit happens earlier than the falling edge of IFC_CLK.
6. Here a convention has been followed in which the more negative/less-positive the number, the smaller the number would be. For example –2 is smaller then –1 and –1 is smaller then 0. So if the min value of this parameter is shown as –2 ns than the for any part parameter's measure will never go to –3ns though it can go to –1 ns.

This figure shows the AC timing diagram.

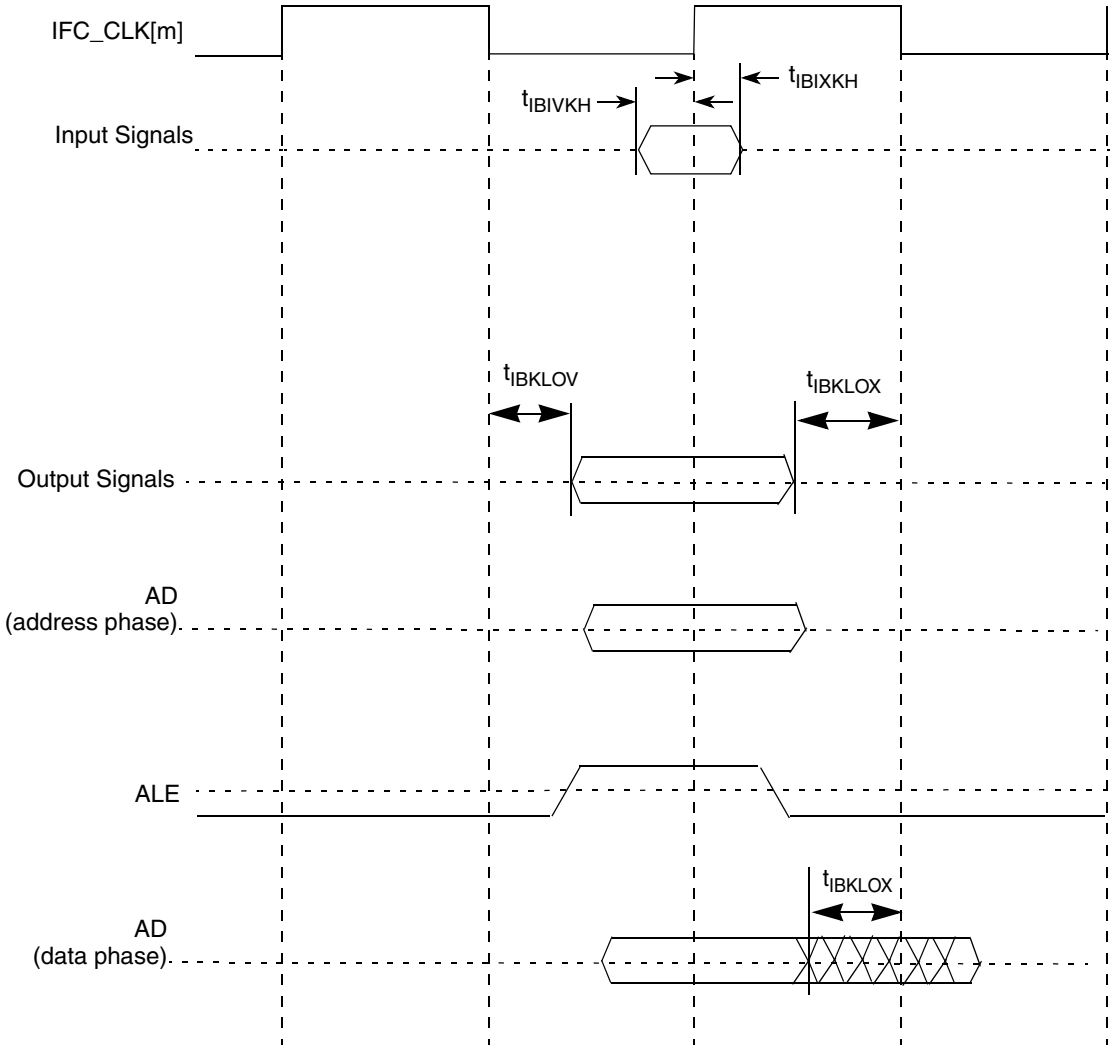
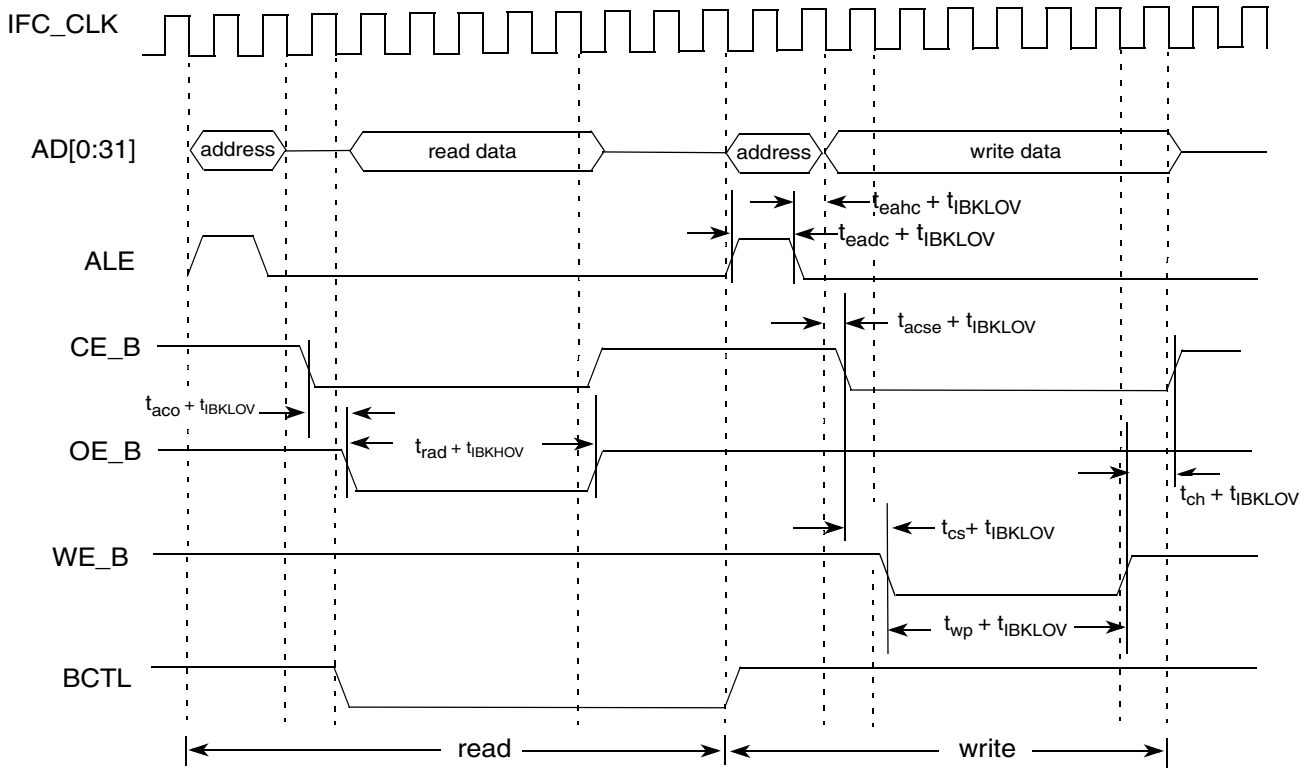


Figure 26. Integrated Flash Controller Signals

Figure 26 applies to all the controllers that IFC supports.

For input signals, the AC timing data is used directly for all controllers. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.



1 t_{aco}, t_{rad}, t_{eahc}, t_{eadc}, t_{acse}, t_{cs}, t_{ch}, t_{wp} are programmable. See the *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

2 For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

Figure 27. GPCM Output Timing Diagram

2.14 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.14.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 58. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × BV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × BV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at BV_{DD} min	0.75 × BV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at BV_{DD} min	—	0.125 × BV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	BV_{DD} - 0.2	—	V	2

Table 58. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with BV_{DD} = 3.3 V or 1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Figure 3.
2. Open drain mode for MMC cards only.

2.14.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in Figure 29.

Table 59. eSDHC AC Timing Specifications

At recommended operating conditions with BV_{DD} = 3.3 or 1.8 V

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode	f_{SFSCK}	 0 0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SFSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SFSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx	$t_{SFSIVKH}$	2.5	—	ns	3, 4
Input hold times: SD_CMD, SD_DATx	$t_{SFSIXKH}$	2.5	—	ns	3, 4
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SFSKHOV}$	—	3	ns	4
Output delay time: SD_CLK to SD_CMD, SD_DATx hold time	$t_{SFSKHOX}$	–3	—	ns	4

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1.5 ns.
4. CCARD ≤10 pF, (1 card), and CL = CBUS + CHOST + CCARD ≤ 40 pF

This figure provides the eSDHC clock input timing diagram.

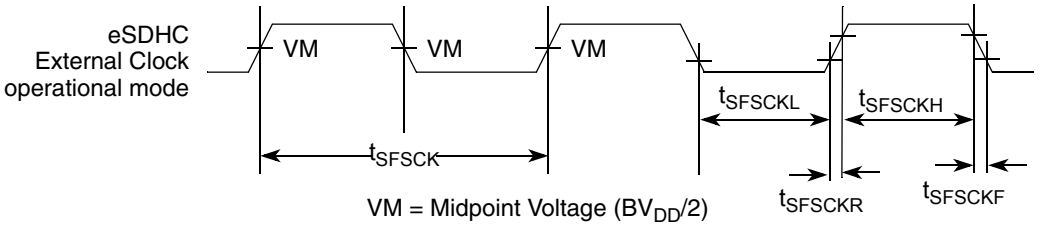


Figure 28. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

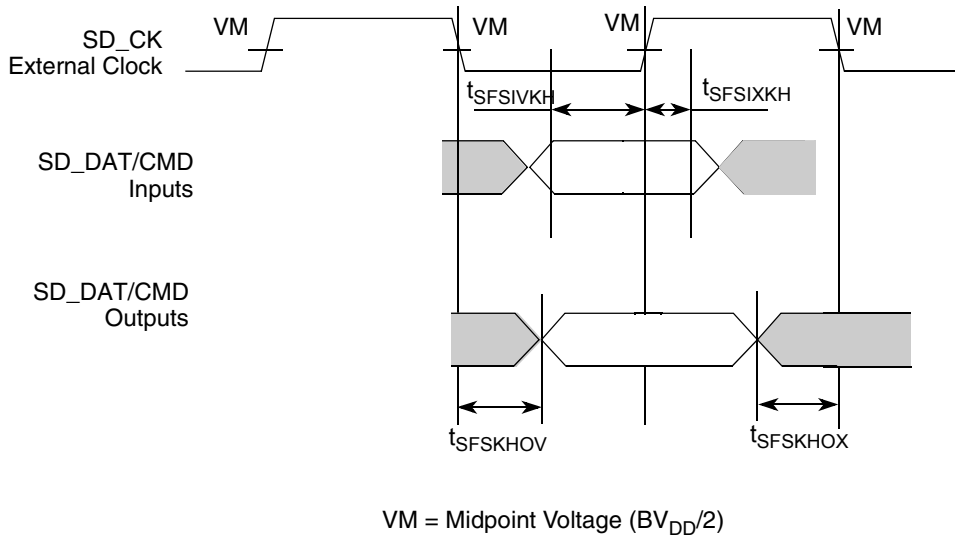


Figure 29. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.15 Programmable Interrupt Controller (PIC) Specifications

This section describes the DC and AC electrical specifications for the PIC.

2.15.1 PIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the PIC interface when operating at $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = 3.3 V.

Table 60. PIC DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN} = CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

Table 60. PIC DC Electrical Characteristics (3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

This table provides the DC electrical characteristics for the PIC interface when operating at $LV_{DD}/OV_{DD}/BV_{DD}/CV_{DD}$ = 2.5 V.

Table 61. PIC DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

This table provides the DC electrical characteristics for the PIC interface when operating at $LV_{DD}/OV_{DD}/BV_{DD}/CV_{DD}$ = 1.8 V.

Table 62. PIC DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = 0V or $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ = $CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—

Table 62. PIC DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.15.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

Table 63. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.16 JTAG

This section describes the AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface. This section applies to both the Power Architecture and DSP JTAG ports. The BSC9131 has multiple JTAG topology; see Section 3.9, "JTAG Configuration Signals," for details.

2.16.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

Table 64. JTAG DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.1	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3
2. Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.16.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 65. JTAG AC Timing Specifications

For recommended operating conditions see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	2	ns	—
TRST_B assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	10	—	ns	—
Output valid times	t_{JTKLDV}	4	10	ns	3
Output hold times	t_{JTKLDX}	30	—	ns	3

Table 65. JTAG AC Timing Specifications (continued)

For recommended operating conditions see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
JTAG external clock to output high impedance	t_{JTKLDZ}	4	10	ns	—

Note:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

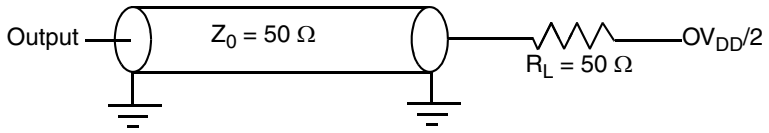


Figure 30. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

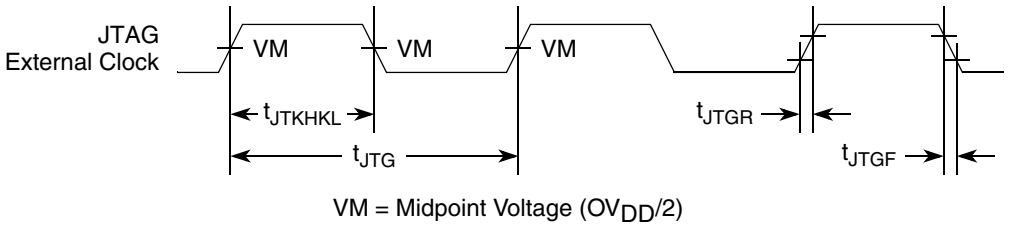


Figure 31. JTAG Clock Input Timing Diagram

This figure provides the TRST_B timing diagram.

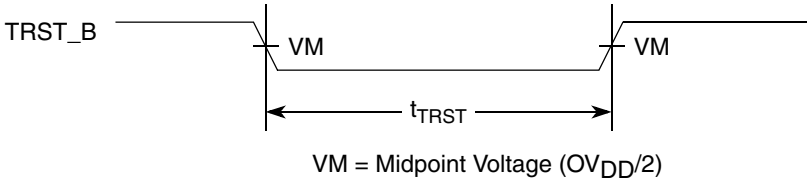


Figure 32. TRST_B Timing Diagram

This figure provides the boundary-scan timing diagram.

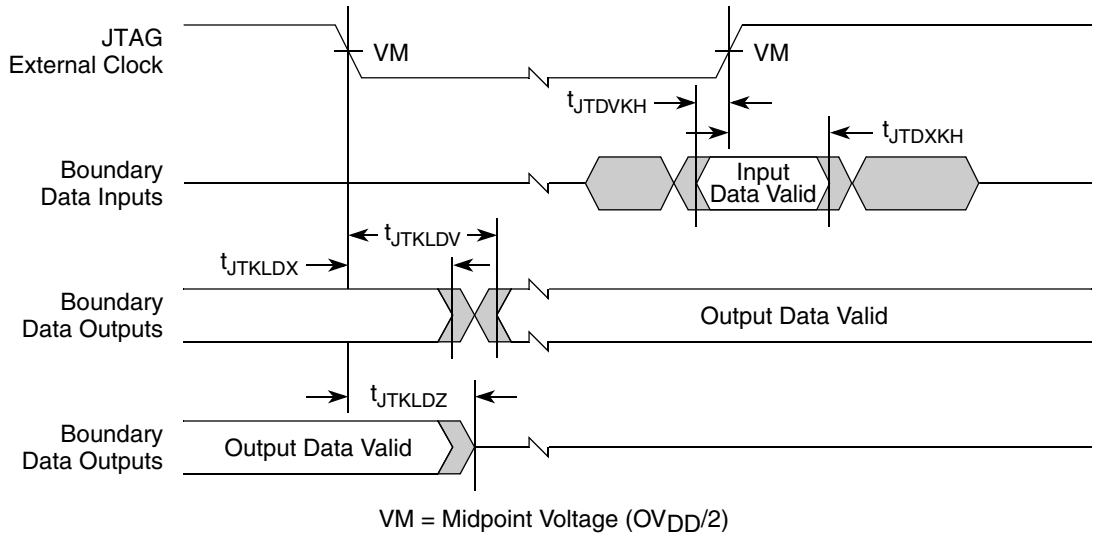


Figure 33. Boundary-Scan Timing Diagram

2.17 I²C

This section describes the DC and AC electrical characteristics for the two I²C interfaces. The input voltage for I²C1 is provided by a OV_{DD} (3.3 V) power supply, while the input voltage for I²C2 is provided by a CV_{DD} (3.3 V/1.8 V) power supply.

2.17.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating from a 3.3 power supply.

Table 66. I²C DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–10	10	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

This table provides the DC timing parameters for the I^2C interface operating from a 1.8 V power supply.

Table 67. I^2C DC Electrical Characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (CV_{IN} = 0 V or CV_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = mn, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Figure 3.
2. Note that the symbol CV_{IN} represents the input voltage of the supply. It is referenced in Figure 3.

2.17.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 68. I^2C AC Electrical Specifications

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 66)

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Table 68. I²C AC Electrical Specifications (continued)

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 66)

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

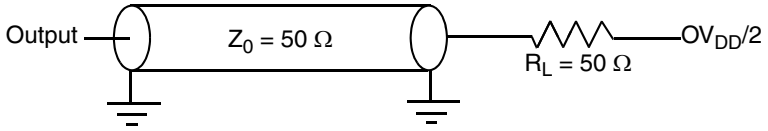


Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

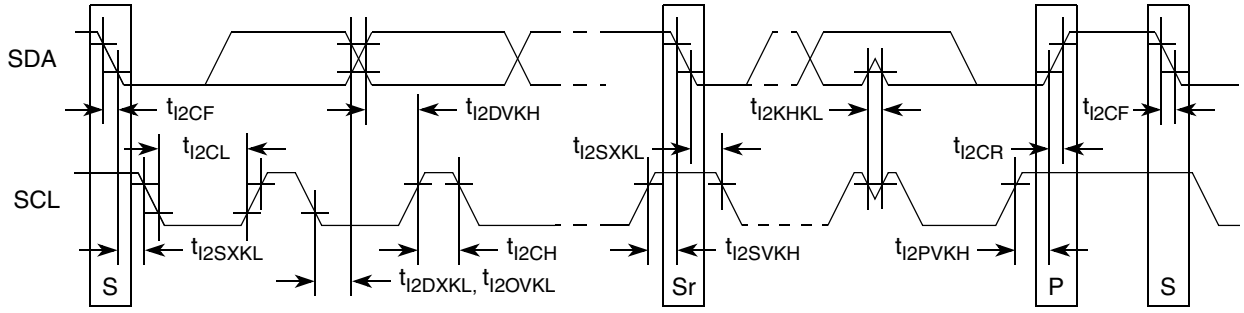


Figure 35. I²C Bus AC Timing Diagram

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface when operating from 3.3-V supply.

Table 69. GPIO DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 2.5-V supply.

Table 70. GPIO DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = 2 mA)	V_{OH}	1.7	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.7	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the GPIO interface when operating from 1.8-V supply.

Table 71. GPIO DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.2	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Table 71. GPIO DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

2.18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 72. GPIO Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Unit	Note
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

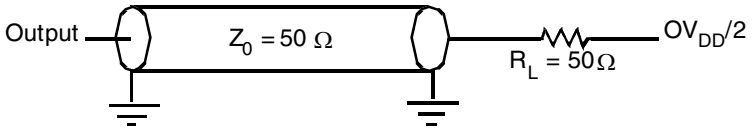


Figure 36. GPIO AC Test Load

2.19 TDM

This section describes the DC and AC electrical specifications for the TDM.

2.19.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics for the TDM interface when operating at 3.3 V.

Table 73. TDM DC Electrical Characteristics ($BV_{DD}/X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	–0.3	0.8	V	1
Input current ($BV_{IN}/X2V_{IN}$ = 0 V or $BV_{IN}/X2V_{IN}$ = $BV_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($BV_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage ($BV_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Table 73. TDM DC Electrical Characteristics (BV_{DD}/$X2V_{DD}$ = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Min	Max	Unit	Note

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN}/$X2V_{IN}$ respective values found in Table 3
2. Note that the symbol BV_{IN}/$X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

Table 74 provides the DC electrical characteristics for the TDM interface when operating at 2.5 V.

Table 74. TDM DC Electrical Characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in Table 3.

This table provides the DC electrical characteristics for the TDM interface when operating at 1.8 V.

Table 75. TDM DC Electrical Characteristics (BV_{DD}/$X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (BV_{IN}/$X2V_{IN}$ = 0 V or BV_{IN}/$X2V_{IN}$ = BV_{DD}/$X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD}/$X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD}/$X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN}/$X2V_{IN}$ respective values found in Table 3
2. Note that the symbol BV_{IN}/$X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3

2.19.2 TDM AC Electrical Characteristics

This table provides the input and output AC timing specifications for the TDM interface.

Table 76. TDM AC Timing Specifications for 62.5 MHz[1]

Parameter	Symbol[2]	Min	Max	Unit	Note
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns	3

Table 76. TDM AC Timing Specifications for 62.5 MHz[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Note
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns	3
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns	3
TDM all input setup time	t_{DMIVKH}	3.6	—	ns	4, 5
TDMxRD input hold time	$t_{DMRDIXKH}$	1.9	—	ns	4, 8
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns	5
TDMxTCK high to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns	7
TDMxTCK high to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns	7, 9
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns	7
TDMxTCK high to TDMxTD output high impedance	t_{DM_OUTHI}	—	9.8	ns	7
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns	6
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns	6

Note: Output values are based on 30 pF capacitive load.

Note: Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. t_{DMxTCK} and t_{DMxRCK} are shown using the rising edge.

1. All values are based on a maximum TDM interface frequency of 62.5 MHz.
2. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the output internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Relevant for all pins that function as TDM RX/TX clock—pins may be TDM_RCK and TDM_TCK, pending TDM port configuration.
4. Relevant for all pins that function as TDM receive data—pins may be TDM_RCK, TDM_RSN, TDM_RDT, TDM_TDT, pending TDM port configuration.
5. Relevant for all pins that function as TDM input frame sync (TX/RX)—pins may be TDM_TSN, TDM_RSN, pending TDM port configuration.
6. Relevant for all pins that function as TDM output frame sync (TX/RX)—pins may be TDM_TSN, TDM_RSN, pending TDM port configuration.
7. Relevant for all pins that function as TDM transmit data—pins may be TDM_RCK, TDM_RSN, TDM_RDT, TDM_TDT, pending TDM port configuration.
8. Applies to any TDM pin that functions as Rx data (including TDMxTD and others).
9. Represents the time from the positive clock edge to the valid data on the Tx data like; it applies to any TDM pin that functions as Tx data (including TDMxRD and others).

This figure shows the TDM receive signal timing.

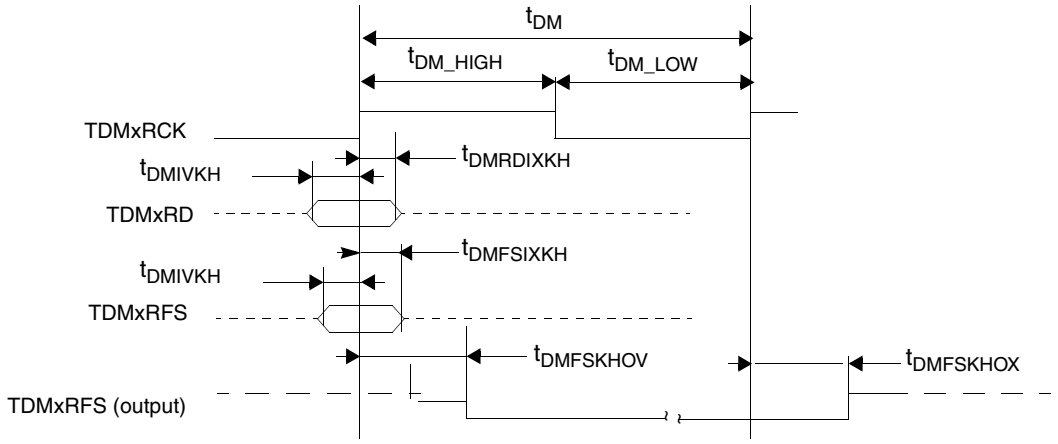


Figure 37. TDM Receive Signals

This figure shows the TDM transmit signal timing.

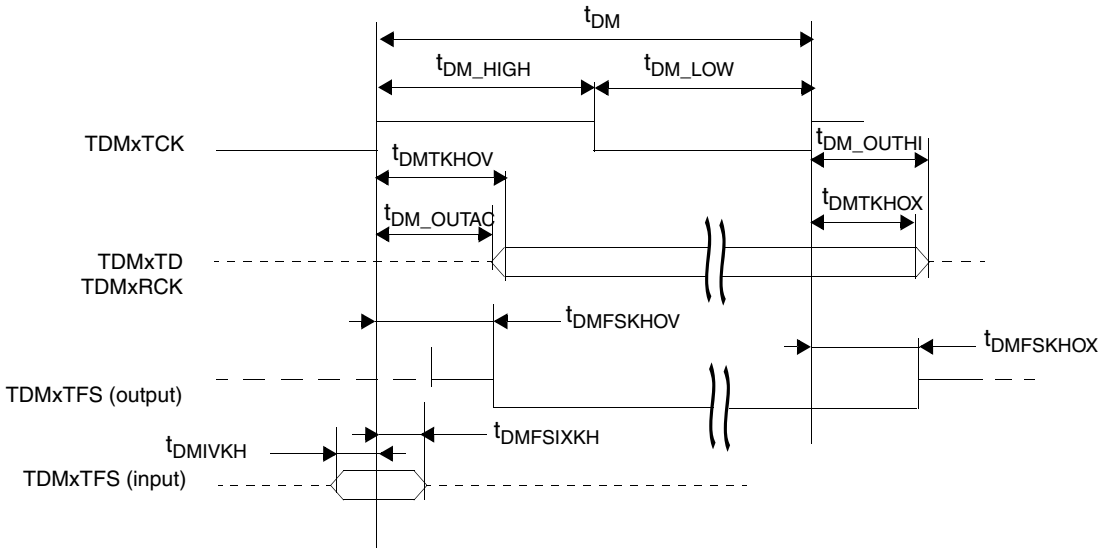


Figure 38. TDM Transmit Signals

This figure provides the AC test load for the TDM.

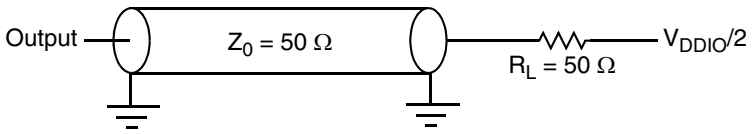


Figure 39. TDM AC Test Load

2.20 Radio Frequency (RF) Interface

2.20.1 RF Parallel Interface

There are two RF interfaces—parallel and MaxPHY serial interfaces.

2.20.1.1 RF Parallel Interface DC Electrical Characteristics (eSPI2)

2.20.1.1.1 RF Parallel Interface DC Data Path

Table 77 provides the DC electrical characteristics for the RF parallel interface when operating at 3.3 V.

Table 77. RF Parallel Interface DC Electrical Characteristics ($X1V_{DD}$, $X2V_{DD}$ = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current ($X1V_{IN}/X2V_{IN}$ = 0 V or $X1V_{IN}/X2V_{IN}$ = $X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $X1V_{IN}/X2V_{IN}$ represent the input voltage of the power supplies. It is referenced in Table 3.

Table 78 provides the DC electrical characteristics for the RF interface when operating at 1.8 V.

Table 78. RF Parallel Interface DC Electrical Characteristics ($X1V_{DD}$, $X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current ($X1V_{IN}/X2V_{IN}$ = 0 V or $X1V_{IN}/X2V_{IN}$ = $X1V_{DD}/X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

2.20.1.1.2 RF Parallel Interface DC Control Plane

See Table 33 in Section 2.9.1, "eSPI1 DC Electrical Characteristics," for the DC specs for eSPI2, powered by $X2V_{DD}$ = 1.8 V.

2.20.1.2 RF Parallel Interface AC Electrical Characteristics (eSPI2)

2.20.1.2.1 RF Parallel AC Data Interface

Table 79 provides the timing specifications for the RF parallel interface.

Table 79. RF Parallel Interface Timing Specification (3.3 V, 1.8 V)[1,2]

Parameter	Symbol	Min	Max	Unit	Note
Data_clk (MCLK) clock period	t_{PDCP}	16.276 (61.44)	—	ns (MHz)	—
Data_clk (MCLK) and fb_clk (FCLK) pulse width	t_{PDMP}	45% of t_{PDCP}	—	—	—
Delay between MCLK and FCLK at the external RFIC including trace delay	t_{PDCD}	—	7.32	ns	—
MCLK input to FCLK output delay at the BSC9131 BBIC	t_{PDMFD}	—	6.32	ns	—
Control/Data output valid time wrt FCLK during Tx from the BSC9131 BBIC	t_{PDOV}	—	6.0	ns	—
Control/Data hold from FCLK during Tx from the BSC9131 BBIC	t_{PDOX}	1.37	—	ns	3
Control/Data setup wrt MCLK	t_{PDIV}	2.5	—	ns	—
Control/Data hold wrt MCLK	t_{PDIX}	0.4	—	ns	—

Note:

1 The max trace delay of MCLK from the external RFIC to the BSC9131 BBIC and FCK/TXNRX/ENABLE from BBIC to RFIC = 1 ns each.

2 The max allowable trace skew between MCLK/FCLK and the respective data/control is 70 ps.

3 1.37 ns includes 70 ps trace skew.

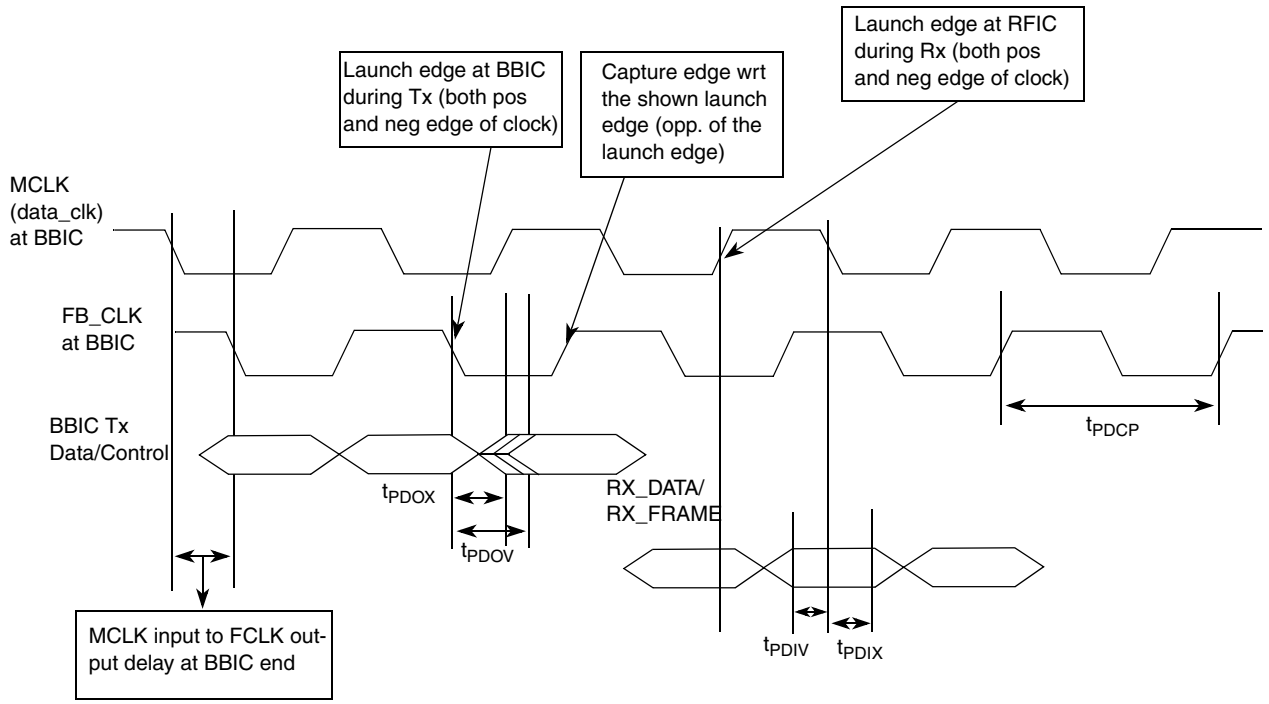


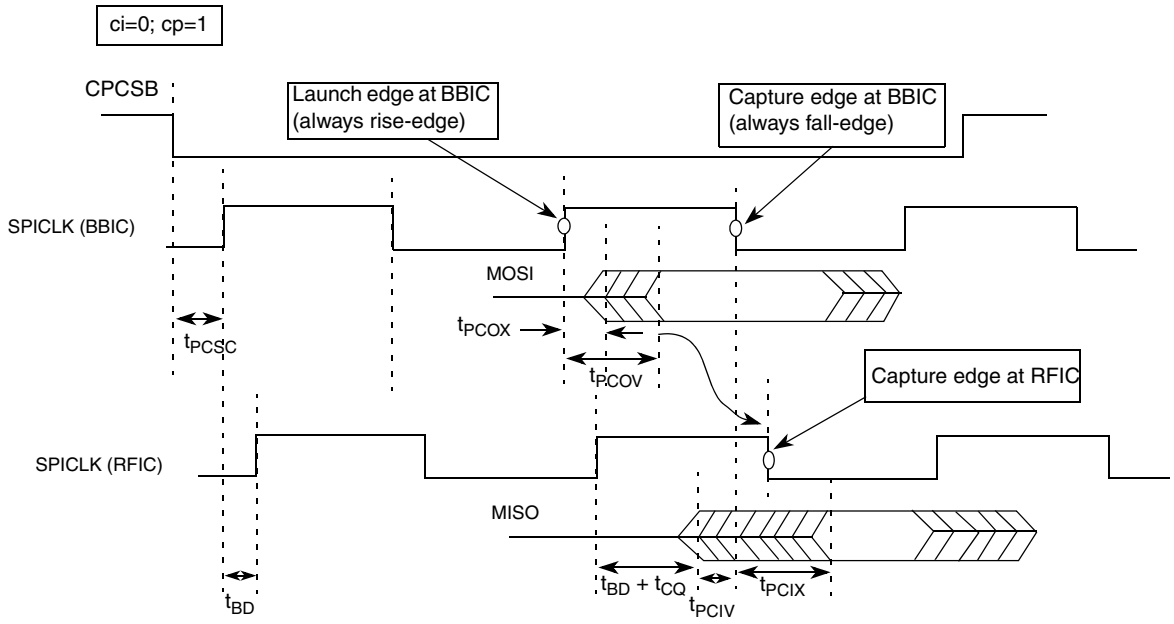
Figure 40. RF Parallel Interface AC Timing Diagram

2.20.1.2.2 RF Parallel Interface AC Control Plane

Table 80. RF Parallel Control Plane Interface AC Timing Specification

Parameter	Symbol	Min	Max	Unit
Control plane clock period	t_{PCCP}	33.3 (30)	—	ns (MHz)
Clock min pulse width	t_{PCMP}	16.6	—	ns
PCB trace delay between the BSC9131 BBIC master and the external RFIC slave	t_{PCBD}	—	1	ns
Setup time from CPCSB assertion to first rising edge of SPICLK	t_{PCSC}	6.1	—	ns
Hold time from last SPICLK falling edge to CPCSB deassertion	t_{PCHC}	9.9	—	ns
MOSI data output setup time against SPICLK	t_{PCOV}	—	15.4	ns
MOSI data ouptut hold time against SPICLK	t_{PCOX}	–16.4	—	ns
MISO data input setup time against SPICLK	t_{PCIV}	7.9	—	ns
MISO data input hold time against SPICLK	t_{PCIX}	21.9	—	ns

Note: RF parallel control plane is SPI2; RF serial control plane is SPI3 and SPI4.



t_{BD}: Board delay from the BSC9131 BBIC to the external RFIC or back
t_{CQ}: Delay in RFIC from input of SPICLK to output valid data
Max permissible board skew: 100 ps
Proposed frequency of SPICLK: 30 MHz

Data timing at RF parallel interface:
Input data setup requirement: 1 ns
Input data hold requirement: 0 ns
t_{CQ}: 4.5 ns–6.5 ns (6.5 ns is critical, which defines the max frequency)

Figure 41. RF Parallel Control Plane Interface AC Timing Diagram

2.20.2 RF Serial (MaxPHY) Interface

2.20.2.1 RF Serial (MaxPHY) Interface DC Electrical Characteristics (eSPI3, eSPI4)

2.20.2.1.1 RF Serial (MaxPHY) Interface DC Data Path

Table 81. RF Serial Interface DC Electrical Characteristics

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Differential input logic high	V_{IHdiff}	0.200	—	V	1, 2
Differential input logic low	V_{ILdiff}	—	–0.200	V	1, 2
Differential input high AC	$V_{IHdiff(AC)}$	0.350	—	V	2
Differential input low AC	$V_{ILdiff(AC)}$	—	–0.350	V	2

Note:
1. Used to define a differential signal slew rate.
2. These values are not defined. However, each signal must be within the respective limites for inputs as well as the limitations for overshoot and undershoot (see Table 82 for specifications).

Table 82 provides the AC overshoot/undershoot specifications; see Figure 42 for the areas referenced.

Table 82. AC Overshoot/Undershoot Specification for Clock and Data

Parameter	Maxim 153.6 MHz
Maximum peak amplitude allowed for overshoot area	0.4
Maximum peak amplitude allowed for undershoot area	0.4
Maximum overshoot area above RVDD	0.25
Maximum overshoot area below GND	0.25

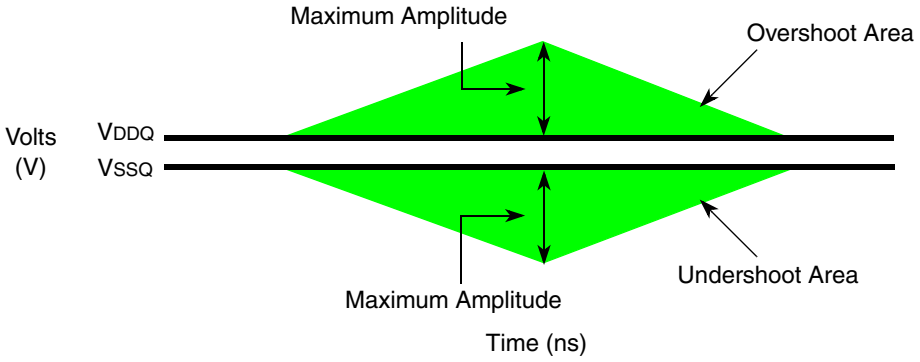


Figure 42. RF Serial Interface AC Overshoot/Undershoot Diagram

2.20.2.1.2 RF Serial (MaxPHY) Interface DC Control Plane

See Table 33 in Section 2.9.1, "eSPI1 DC Electrical Characteristics," for the DC specs for eSPI3 and eSPI4, powered by $X1V_{DD}$ = 1.8 V.

2.20.2.2 RF Serial (MaxPHY) Interface AC Electrical Characteristics (eSPI3, eSPI4)

2.20.2.2.1 RF Serial (MaxPHY) AC Data Interface

Table 83 provides the timing specifications for the RF parallel interface.

Table 83. RF Serial Interface Timing Specification

Parameter	Symbol	Min	Max	Unit	Note
TXCLK max period (frequency)	t_{SDCP}	6.51 (153.6)	—	ns (MHz)	1
Setup time to falling edge of TXCLK	t_{SDOV}	—	3.08	ns	2
Hold time to falling edge of TXCLK	t_{SDOX}	–3.05	—	ns	2

Note:

1 The maximum trace skew between TXLCK and data is estimated <50 ps.

2 Assuming 50 ps worst trace skew.

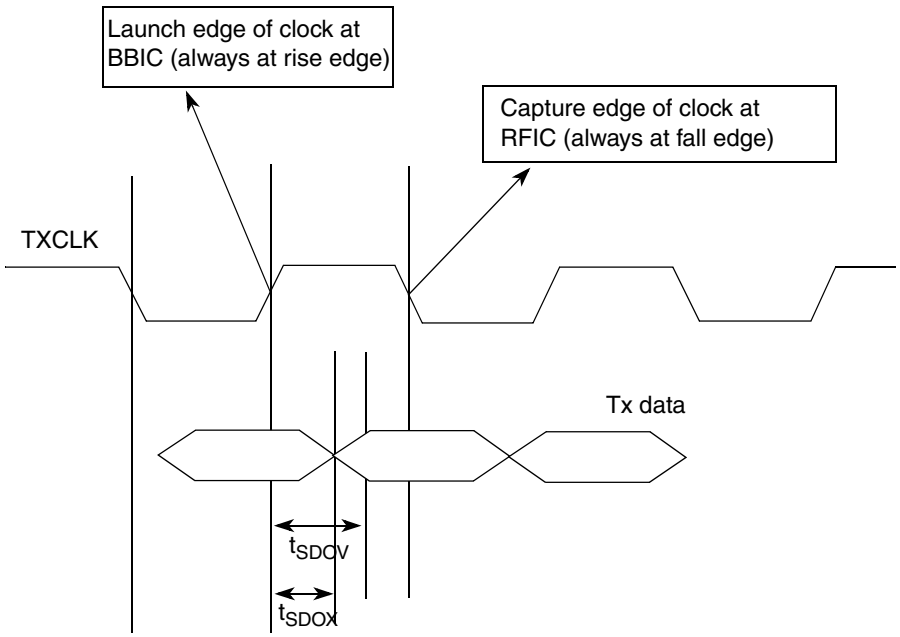


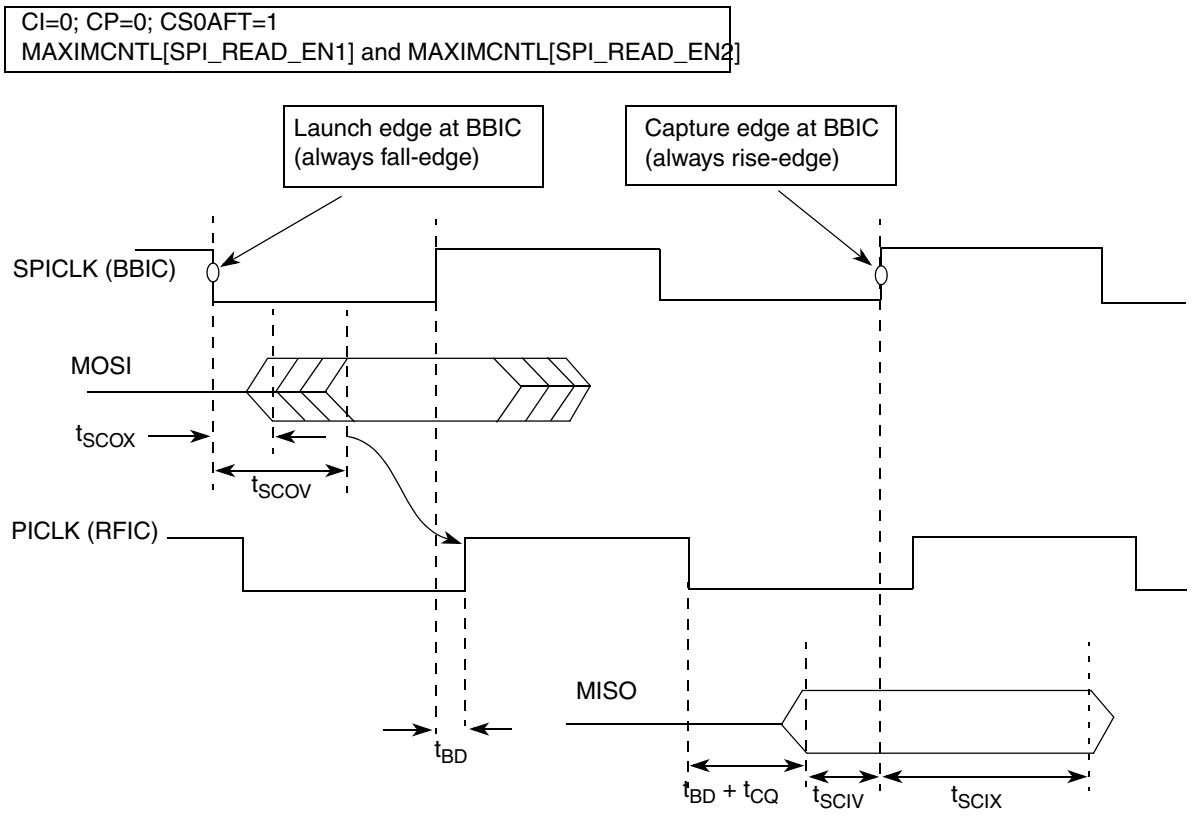
Figure 43. RF Serial Interface AC Timing Diagram

2.20.2.2.2 RF Serial (MaxPHY) Interface AC Control Plane

Table 84. RF Serial Control Plane Interface AC Timing Specification

Parameter	Symbol	Min	Max	Unit	Note
Control plane clock period (frequency)	t_{SCCP}	50 (20)	—	ns (MHz)	—
Clock min pulse width	t_{SCMP}	20	—	ns	—
PCB trace delay between the BSC9131 BBIC master and the external RFIC slave	t_{SCBP}	—	1	ns	—
Setup time from CS assertion to first SPICLK rising edge	t_{SCSC}	5	—	ns	—
Hold time from last SPICLK falling edge to CS deassertion	t_{SCHC}	5	—	ns	—
MOSI data output setup time against SPICLK	t_{SCOV}	—	10.4	ns	1
MOSI data ouptut hold time against SPICLK	t_{SCOX}	–10.4	—	ns	—
MISO data input setup time against SPICLK	t_{SCIV}	10.4	—	ns	2
MISO data input hold time against SPICLK	t_{SCIX}	31	—	ns	—

Note:
1 Wrt 30 MHz SPICLK
2 Wrt 25 MHz SPICLK



t_{BD}: Board delay from either side
t_{CQ}: Data delay wrt to clock at the external RFIC
Proposed max frequency: 25 MHz
Max board skey permissible: 100 ps

Data timing at RF serial interface:
Input data setup requirement: 6 ns
Input data hold requirement: 6 ns
t_{CQ}: 12.5 ns

Figure 44. RF Serial Control Plane Interface AC Timing Diagram

2.20.2.2.3 RF Serial (MaxPHY) Jitter and Skew Specfications

Table 85. RF Serial (MaxPHY) Jitter and Skew Specifications

Parameter	Symbol	Max	Unit	Comments
Rx Path				
Jitter introduced in Rx path (peak-to-peak)	t_{SDIJ}	705	ps	Where D_J = 345 ps, R_J = 360 ps p-p
Skew introduced between I and Q in Rx path	t_{SDIIQS}	118	ps	—
Skew introduced between differential I & Q pair in Rx path	t_{SDIDS}	149	ps	—
Tx Path				
Jitter introduced in Tx path (peak-to-peak)	t_{SDOJ}	725	ps	—
Skew introduced between I and Q in Tx path	t_{SDOIQS}	117	ps	—
Skew introduced between differential I & Q pair in Tx path	t_{SDODS}	73	ps	—

2.20.3 Pulse-Width Modulator (PWM)

There are two pulse-width modulators (PWM). Both PWMs are connected at two different pins. The output of PWM is pulse-width modulated signal (PWMO) available at external output pin.

2.20.3.1 PWM Timing

Figure 45 shows the timing diagram of PWM.

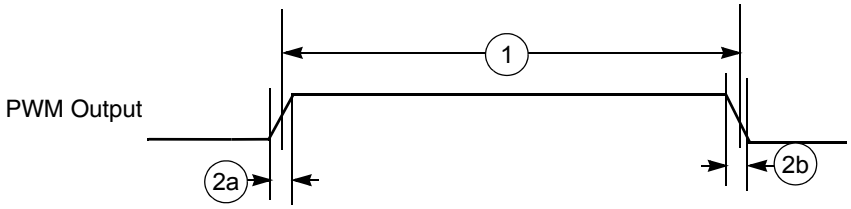


Figure 45. PWM Timing Diagram

Table 86 lists the PWM output timing characteristics.

Table 86. PWM Output Timing Parameter

Ref No.	Parameter	Minimum	Maximum	Unit
1	Output pulse width	$(1/f_{platform\_clk})$	—	ns
2a	Output rise time	TBD	TBD	ns
2b	Output fall time	TBD	TBD	ns

2.21 Universal Subscriber Identity Module (USIM)

The USIM module interface consist of a total of five pins. Only “Internal One Wire” interface mode is supported. In this mode, the Rx input of the USIM IP is connected to the TX output of the USIM, which is internal to the device. Only one bidirectional signal (Rx/Tx) is routed to the device pin, which is connected to the external SIM card.

The interface is meant to be used with synchronous SIM cards. This means that the SIM module provides a clock for the SIM card to use. The frequency of this clock is normally 372 times the data rate on the Rx/Tx pins; however, the SIM module can work with CLK equal to 16 times the data rate on Rx/Tx pins.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card will be used by the SIM card to recover the clock from the data much like a standard UART. All five pins of SIM module are asynchronous to each other.

There are no required timing relationships between the pads in normal mode, The SIM card is initiated by the interface device, whereupon the SIM card will send a response with an Answer to Reset. Although the SIM interface has no specific requirement, the ISO-7816 specifies reset and power down sequences. For detailed information, see ISO-7816.

The USIM interface pins are available at two locations. At one location, it is multiplexed with eSDHC and TDM functionality and is powered by the BVDD power supply (3.3V/2.5V/1.8V). At the other location, it is multiplexed with eSPI and UART functionality and is powered by CVDD power supply (3.3V/1.8V).

2.21.1 USIM DC Electrical Characteristics

This table provides the DC electrical characteristics for the USIM interface.

Table 87. USIM Interface DC Electrical Characteristics

At recommended operating conditions with BV_{DD} = 3.3 V/2.5 V/1.8 V.

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Input high voltage	V_{IH}	—	0.625 × BV_{DD}	—	V	1
Input low voltage	V_{IL}	—	—	0.25 × BV_{DD}	V	1
Output high voltage	V_{OH}	I_{OH} = –100 uA at BV_{DD}min	0.75 × BV_{DD}	—	V	—
Output low voltage	V_{OL}	I_{OL} = 100uA at CV_{DD}min	—	0.125 × BV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 uA	BV_{DD} - 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	0.3	V	2
Input/output leakage current	I_{IN}/I_{OZ}	—	–10	10	uA	—

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max BV_{IN} values found in Figure 3.
2. Open drain mode for SIM cards only.

2.21.2 USIM General Timing Requirements

The timing requirements for the USIM are found in Table 88.

Table 88. USIM Timing Specification, High Drive Strength

Parameter	Symbol	Min	Max	Unit	Note
USIM clock frequency (SIM_CLK)	S_{freq}	0.01	25	MHz	1
USIM clock rise time (SIM_CLK)	S_{rise}	—	0.09 × (1/S_{freq})	ns	2
USIM clock fall time (SIM_CLK)	S_{fall}	—	0.09* × 1/S_{freq})	ns	2
USIM input transition time (SIM_TRXD, SIM_PD)	S_{trans}	10	25	ns	—
USIM I/O rise time / fall time (SIM_TRXD)	Tr/Tf	—	1	µs	3
USIM RST rise time / fall time (SIM_RST)	Tr/Tf	—	1	µs	4

Note:

1 50% duty cycle clock
2 With C = 50 pF
3 With CIN = 30 pF, COUT = 30 pF
4 With C_{IN} = 30 pF

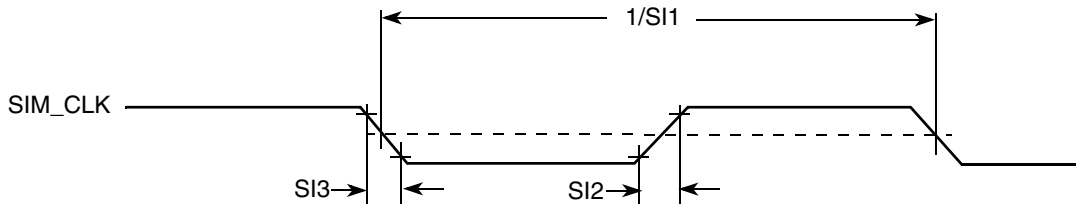


Figure 46. USIM Clock Timing Diagram

2.21.3 USIM External Pull Up/Pull Down Resistor Requirements

External off-chip pull up resistor of 20 KΩ is required on the SIM_TRXD pin.

External off-chip pull down resistors are required on the SIM_PD, SIM_SVEN, SIM_RST pins.

2.21.4 USIM Reset Sequence

2.21.4.1 SIM Cards With Internal Reset

The sequence of reset for this kind of SIM cards is as follows (see Figure 47):

- After power up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, Rx must be high.
- The card must send a response on Rx acknowledging the reset between 400 and 40000 clock cycles after T0.

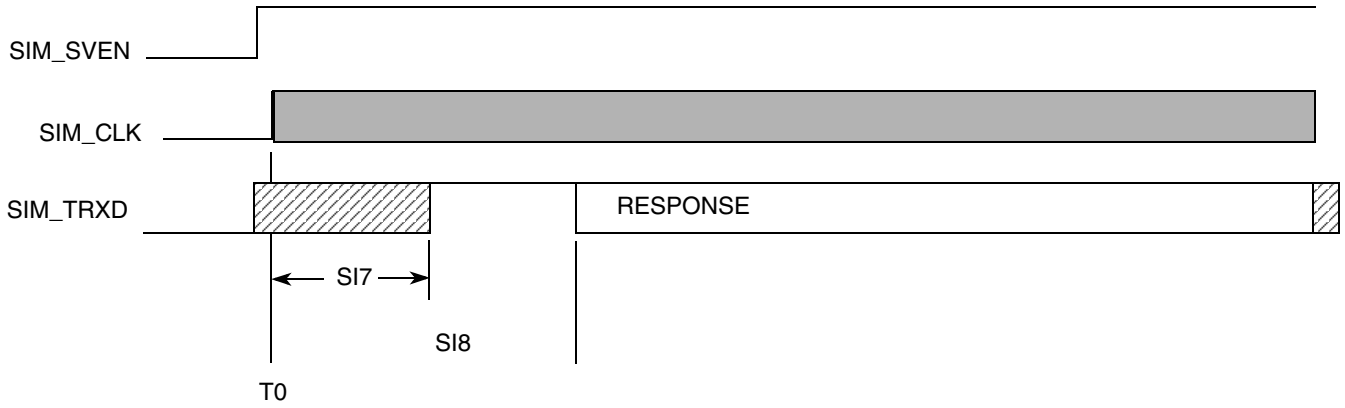


Figure 47. Internal-Reset Card Reset Sequence

Table 89. Parameters of Reset Sequence For Card With Internal Reset

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM clock to SIM TX data H	$S_{clk2dat}$	—	200	SIM_CLK clock cycle
SI8	SIM clock to SIM get ATR data	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle

2.21.4.2 SIM Cards With Active-Low Reset

The sequence of reset for this kind of card is as follows (see Figure 48):

- After powering up, the clock signal is enabled on SIM_CLK (time T0).
- After 200 clock cycles, SIM_TRXD must be high.
- SIM_RST must remain Low for at least 40000 clock cycles after T0 (no response is to be received on Rx during those 40000 clock cycles).
- SIM_RST is set High (time T1).
- SIM_RST must remain High for at least 40000 clock cycles after T1 and a response must be received on SIM_TRXD between 400 and 40000 clock cycles after T1.

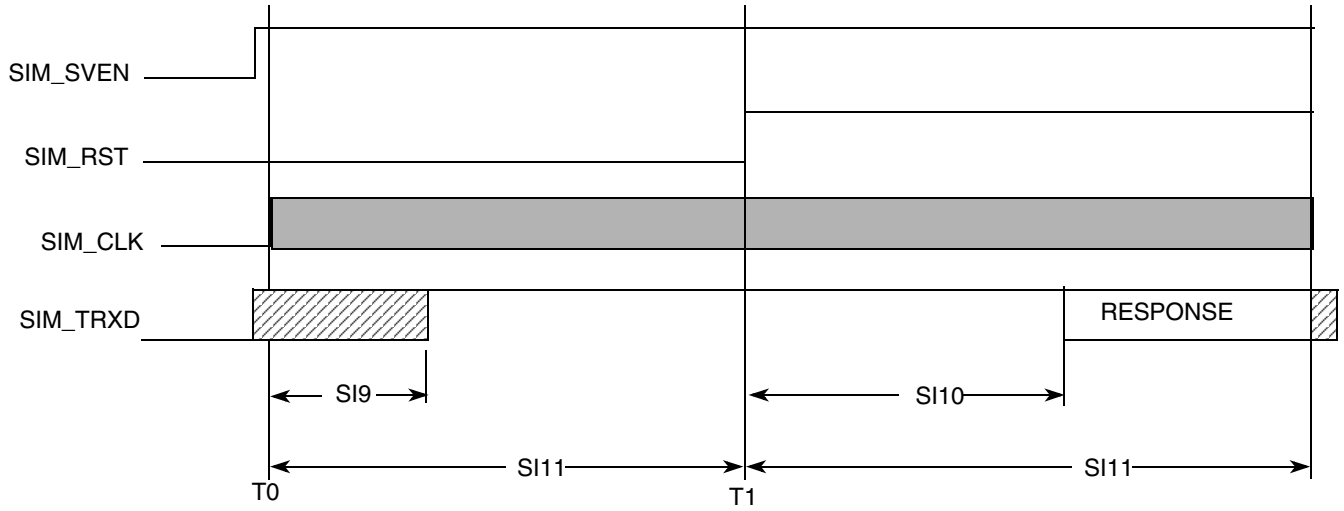


Figure 48. Active-Low Reset Card Reset Sequence

Table 90. Parameters of Reset Sequence For Active-Low Reset Card

ID	Parameter	Symbol	Min	Max	Unit
SI9	SIM clock to SIM TX data H	$S_{clk2dat}$	—	200	SIM_CLK clock cycle
SI10	SIM reset rising to SIM TX data low	$S_{clk2atr}$	400	40000	SIM_CLK clock cycle
SI11	SIM clock to SIM reset signals	$S_{clk2rst}$	40000	—	SIM_CLK clock cycle

2.21.4.3 USIM Power Down Sequence

Power down sequence for SIM interface is as follows:

- SIM_PD port detects the removal of the SIM card
- SIM_RST goes low
- SIM_CLK goes low
- SIM_TRXD goes low
- SIM_SVEN goes low

Each of these steps is done in one CKIL period (typically 32 KHz). Power down is initiated by detection of a SIM card removal or is launched by the processor. See Figure 49 and Table 91 for the timing requirements for this sequence, with F_{CKIL} = CKIL frequency value.

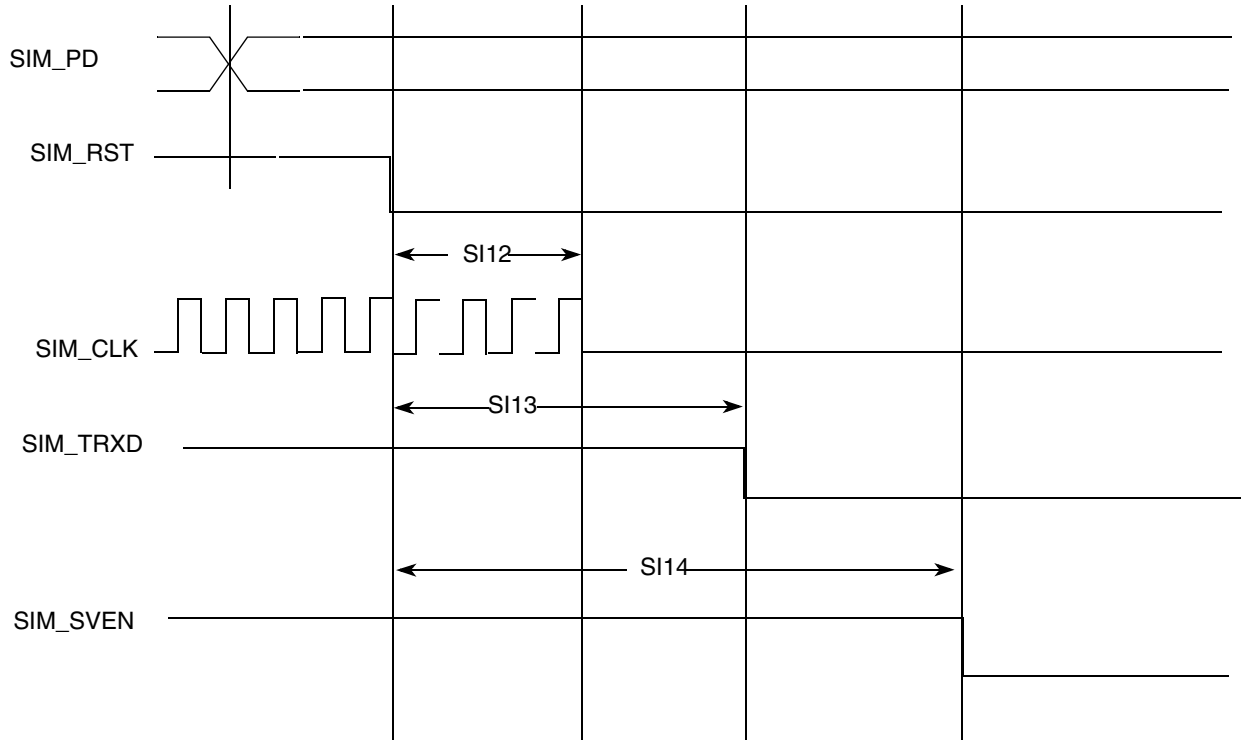


Figure 49. SmartCard Interface Power Down AC Timing

Table 91. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI12	USIM reset to USIM clock stop	$S_{rst2clk}$	0.9 × 1/Fckil	1.1 × $1/F_{CKIL}$	ns
SI13	USIM reset to USIM Tx data low	$S_{rst2dat}$	1.8 × 1/Fckil	2.2 × $1/F_{CKIL}$	ns
SI14	USIM reset to USIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Fckil	3.3 × $1/F_{CKIL}$	ns
SI15	USIM presence detect to USIM reset low	S_{pd2rst}	0.9 × 1/Fckil	1.1 × $1/F_{CKIL}$	ns

2.22 Timers and Timers_32b AC Timing Specifications

This table lists the timer input AC timing specifications.

Table 92. Timers Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Minimum	Unit	Note
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Note:

1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure shows the AC test load for the timers.

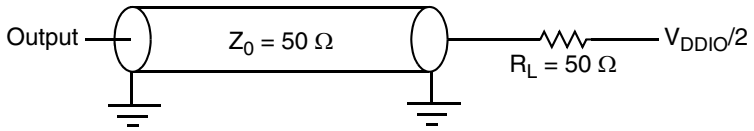


Figure 50. Timer AC Test Load

3 Hardware Design Considerations

This section discusses the hardware design considerations.

3.1 Power Architecture System Clocking

This section describes the PLL configuration for the Power Architecture side of the device. Note that the platform clock is identical to the internal core complex bus (CCB) clock.

This device includes 3 PLLs, as follows:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, “Power Architecture Platform to SYSCLK PLL Ratio.”
- The e500 core PLL generates the core clock from the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 3.1.3, “e500 Core to Platform Clock PLL Ratio.”
- The DDR PLL generates the clocking for the DDR SDRAM controller. The frequency ratio between DDR clock and platform clock is selected using the DDR PLL ratio configuration bits as described in section Section 3.1.4, “Power Architecture DDR/DDRCLK PLL Ratio.”
- The MAPLE eTVPE clock is sourced from the DDR PLL and has a maximum frequency of 800 MHz.

3.1.1 Power Architecture Clock Ranges

Table 93 provides the clocking specifications for the processor core and platform.

Table 93. Power Architecture Processor Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Note
	Min	Max		
e500 core processor frequency	400	1000	MHz	1, 2, 3
Platform CCB bus clock frequency	267	500	MHz	1, 4, 5

Table 93. Power Architecture Processor Clocking Specifications (continued)

Characteristic	Maximum Processor Core Frequency		Unit	Note
	Min	Max		

Note:

1. **Caution:** The Power Architecture platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio," and Section 3.1.3, "e500 Core to Platform Clock PLL Ratio" and Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio," for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform clock frequency of 267 MHz.
3. The reset config signal cfg_core_speed must be pulled low if the core frequency is 500 MHz or below.
4. These values are preliminary and subject to change.
5. The reset config signal cfg_plat_speed must be pulled low if the CCB bus frequency is lower than 320 MHz.

The DDR memory controller can run in asynchronous mode.

Table 94 provides the clocking specifications for the memory bus.

Table 94. Power Architecture Memory Bus Clocking Specifications

Characteristic	Min	Max	Unit	Note
Memory bus clock frequency	320	400	MHz	1, 2, 3

Note:

1. **Caution:** The platform clock to SYSCLK ratio and e500 core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Section 3.1.2, "Power Architecture Platform to SYSCLK PLL Ratio," and Section 3.1.3, "e500 Core to Platform Clock PLL Ratio," and Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio," for ratio settings.
2. The memory bus clock refers to the memory controllers' Dn_MCK[0:5] and Dn_MCK[0:5]_B output clocks, running at half of the DDR data rate.
3. In asynchronous mode, the memory bus clock speed is dictated by its own PLL. See Section 3.1.4, "Power Architecture DDR/DDRCLK PLL Ratio." The memory bus clock speed must be less than or equal to the platform clock rate, which in turn must be less than the DDR data rate.

As a general guideline, the following procedures can be used for selecting the DDR data rate or platform frequency:

1. Start with the processor core frequency selection.
2. Once the processor core frequency is determined, select the platform frequency from the options listed in Table 96 and Table 100.
3. Check the platform to SYSCLK ratio to verify a valid ratio can be chosen from Table 98.
4. Please note that the DDR data rate must be greater than the platform frequency. In other words, running DDR data rate lower than the platform frequency is not supported.
5. Verify all clock ratios to ensure that there is no violation to any clock and/or ratio specification.

3.1.2 Power Architecture Platform to SYSCLK PLL Ratio

The clock that drives the internal CCB bus is called the platform clock. The frequency of the platform clock is set using the following reset signals, as shown in Table 95:

- SYSCLK input signal

- Binary value on IFC_AD[0:2] at power up

These signals must be pulled to the desired values.

In asynchronous mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 95. Power Architecture Platform/SYSCLK Clock Ratios

Binary Value of IFC_AD[0:2] Signals	Platform: SYSCLK Ratio
000	4:1
001	5:1
010	6:1
All Others	Reserved

3.1.3 e500 Core to Platform Clock PLL Ratio

The clock ratio between the e500 core and the platform clock is determined by the binary value of IFC_AD[3:5] signals at power up. Table 96 describes the supported ratios. There are no default values for these PLL ratios; these signals must be pulled to the desired values. Note that IFC_AD[6] must be pulled low if the core frequency is 500 MHz or below.

Table 96. e500 Core to Platform Clock Ratios

Binary Value of IFC_AD[3:5]Signals	e500 Core: Platform Ratio
010	1:1
011	1.5:1
100	2:1
101	2.5:1
110	3:1
All Others	Reserved

3.1.4 Power Architecture DDR/DDRCLK PLL Ratio

Table 97 describes the clock ratio between the DDR memory controller complex and the DDR PLL reference clock, DDRCLK, which is not the memory bus clock. The DDR memory controller complex clock frequency is equal to the DDR data rate.

The DDR PLL rate to DDRCLK ratios listed in Table 97 reflects the DDR data rate to DDRCLK ratio, since the DDR PLL rate in asynchronous mode means the DDR data rate resulting from DDR PLL output. This ratio is determined by the binary value of the IFC_AD[7].

Table 97. Power Architecture DDR Clock Ratio

Binary Value of {IFC_AD[7], IFC_ADDR[22]} Signal	DDR:DDRCLK Ratio
00	8:1
01	10:1
10	12:1
11	Reserved

3.1.5 Power Architecture SYSCLK and Platform Frequency Options

Table 98 shows the expected frequency options for SYSCLK and platform frequencies.

Table 98. Power Architecture SYSCLK and Platform Frequency Options

Platform:SYSCLK	SYSCLK Frequency (MHz)		
	66.66	80	100
	Platform Frequency (MHz)[1]		
4:1	267	320	400
5:1	333	400	500
6:1	400	480	600

1) Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).

3.2 DSP System Clocking

This section describes the PLL configuration for the DSP side of the device. Note that the platform clock is identical to the internal core complex bus (CCB) clock.

This device has the following PLL:

- One SC3850 core PLL

3.2.1 DSP Clock Ranges

Table 99 provides the clocking specifications for the SC3850 processor core.

Table 99. DSP Processor Clocking Specifications

DSP Core	Minimum Frequency	Maximum Frequency	Unit
SC3850 core	800	1000	MHz

3.2.2 DSPCLKIN and SC3850 Core Frequency Options

Table 100 shows the expected frequency options for DSPCLKIN and SC3850 core frequencies.

Table 100. Options for SC3850 Core Clocking

PLL_T2 MF	DSPCLKIN Frequency (MHz)			
	66.66	80	100	133
	SC3850 Core Frequency (MHz)			
1	66.66	80	100	133
8	533	640	800	1066
10	667	800	1000	—
12	800	960	—	—
15	1000	—	—	—

3.3 Supply Power Default Setting

This device is capable of supporting multiple power supply levels on its I/O supply. Table 101 through Table 105 shows the encoding used to select the voltage level for each I/O supply. When setting the VSEL signals, "1" is selected through a pull-up resistor to OVDD (as seen in Table 1).

Table 101. Default Voltage Level for BV_{DD}

BVDD_VSEL[0:1]	I/O Voltage Level
00	3.3 V
01	2.5 V
10	1.8 V
11	Reserved

Table 102. Default Voltage Level for CV_{DD}

CVDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 103. Default Voltage Level for $X1V_{DD}$

X1VDD_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 104. Default Voltage Level for $X2V_{DD}$

XVDD2_VSEL	I/O Voltage Level
0	3.3 V
1	1.8 V

Table 105. Default Voltage Level for LV_{DD}

LVDD_VSEL	I/O Voltage Level
0	3.3 V
1	2.5 V

3.4 PLL Power Supply Design

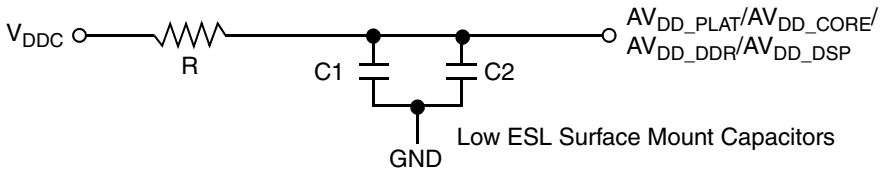
Each of the PLLs listed above is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE, AVDD_DDR, AVDD_DSP, and AVDD_RF respectively). The AV_{DD} level should always be equivalent to V_{DDC}, and these voltages must be derived directly from V_{DDC} through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 51, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 624 ball FCPBGA the footprint, without the inductance of vias.

Figure 51 shows the core PLL (AV_{DD_CORE}) power supply filter circuit.



Notes:

R = 5Ω ± 5%

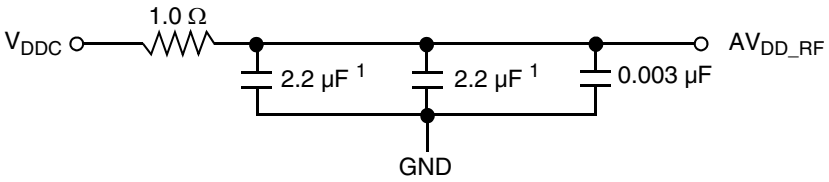
C1 = 10μF ± 10%, 603, X5R with ESL ≤ 0.5 nH

C2 = 1.0μF ± 10%, 402 X5R with ESL ≤ 0.5 nH

This circuit applies for system PLL, core PLL, DDR PPLL, and DSP PLL.

Figure 51. PLL Power Supply Filter Circuit

The AVDD_RF signal provides power for the RF PLL. This PLL generates clock for communication with the MaxPHY RF interface controller. This supply should be after low pass filter from board. Filter components, a resistor and three capacitors are required on this supply. The resistor should be connected between platform 1 V and AVDD_RF. Platform 1 V should be directly tapped from a 1 V regulator using a star connection. Place capacitors in parallel on AVDD_RF pin, physically close to chip. See Figure 52.



1. An 0805 sized capacitor is recommended for system initial bring-up

Figure 52. RF PLL Power Supply Filter Circuit

3.5 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, BVDD, CVDD, OVDD, GVDD, LVDD, RVDD, X1VDD, and X2VDD pin of the device. These decoupling capacitors should receive their power from separate VDD, BVDD, OVDD, GVDD, LVDD, RVDD, X1VDD, X2VDD, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0201 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors on open drain type pins including I^2C pins (1 kΩ is recommended) and MPIC interrupt pins (2–10 kΩ is recommended).

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 54. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior, and spurious assertion gives unpredictable results.

3.7 Output Buffer DC Impedance

The drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 53). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

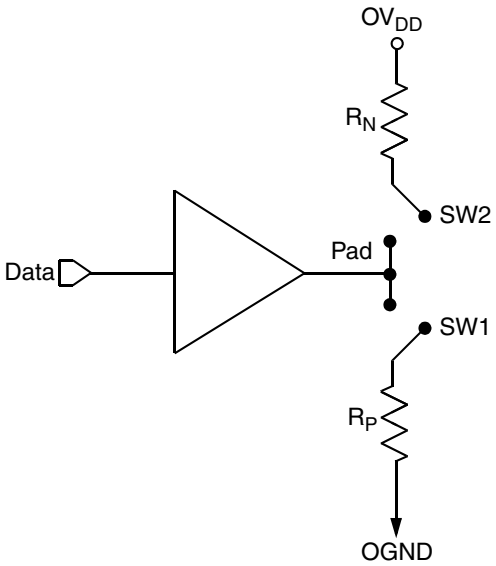


Figure 53. Driver Impedance Measurement

Table 106 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DDC}, nominal OV_{DD}, 90°C.

Table 106. Impedance Characteristics

Impedance	IFC, Ethernet, DUART, Control, Configuration, Power Management	DDR DRAM	Symbol	Unit
R_N	43 Target	20 Target	Z_0	W
R_P	43 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 2.

3.8 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET_B is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET_B is asserted, is latched when HRESET_B deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET_B (and for platform/system clocks after HRESET_B deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

3.9 JTAG Configuration Signals

There are two JTAG ports:

- Power Architecture JTAG (TDI, TDO, TMS, TCK, and TRST_B)
- DSP JTAG (DSP_TDI, DSP_ TDO, DSP_TMS, DSP_TCK, and DSP_TRST_B)

Note that the DSP JTAG is available as a muxed option on I/O pins.

The Power Architecture JTAG is the primary JTAG interface of the chip. DSP JTAG is defined as optional debug interface. As seen in Table 107, the JTAG topology is selectable by static value driven on two pins—CFG_0_JTAG_MODE and CFG_1_JTAG_MODE.

Table 107. JTAG Topology

{CFG_0_JTAG_MODE, CFG_1_JTAG_MODE}	Uses Power Architecture Debug Header	Uses DSP Debug Header	JTAG Topology
00	Yes	No	Access Power Architecture domain and DSP domain using Power Architecture JTAG port
01	Yes	No	Access DSP domain using Power Architecture JTAG port
10	Yes	No	Access Power Architecture domain using Power Architecture JTAG port

Table 107. JTAG Topology (continued)

{CFG_0_JTAG_MODE, CFG_1_JTAG_MODE}	Uses Power Architecture Debug Header	Uses DSP Debug Header	JTAG Topology
11	Yes	Yes	Access Power Architecture domain using Power Architecture JTAG and DSP domain using DSP JTAG

Note: For boundary SCAN, set {CFG_0_JTAG_MODE, CFG_1_JTAG_MODE} = 10.

The TRST/DSP_TRST signal is optional in the IEEE 1149.1 specification, but is provided on the device. The device requires TRST/DSP_TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert TRST/DSP_TRST during the power-on reset flow. Simply tying TRST/DSP_TRST to HRESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of the processor allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The arrangement shown in Figure 54 and Figure 55 allows the COP/ONCE port to independently assert HRESET_B or TRST, while ensuring that the target can drive HRESET_B as well.

The COP interface has a standard header for connection to the target system. The 16-pin PA COP connector is shown in Figure 54.

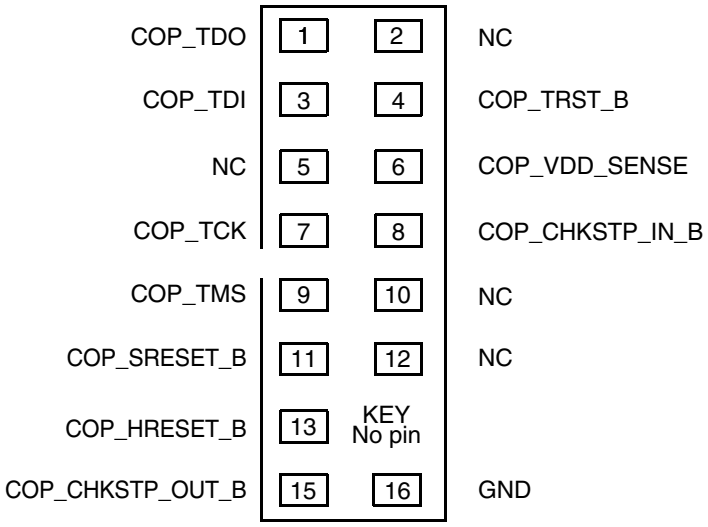


Figure 54. COP Connector Physical Pinout

The ONCE interface also has a standard header for connection to the target system. The 14-pin DSP ONCE connector is shown in Figure 55.

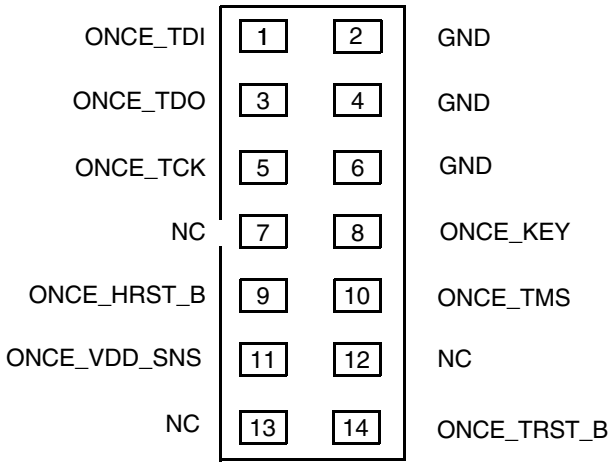


Figure 55. ONCE Connector Physical Pinout

3.9.1 Termination of Unused Signals

If the Power Architecture JTAG or DSP JTAG interface and COP/ONCE header is not used, Freescale recommends the following connections:

- TRST_B should be tied to HRESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (HRESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 54. If this is not possible, the isolation resistor allows future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.
- TCK should be pulled down to GND through a 1 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device. See AN4405, “BSC9131 QorIQ Qonverge Multicore Baseband Processor Design Checklist,” for more information.
- No connection is required for TDI, TDO, or TMS.

NOTE

In the case where the DSP JTAG is also used (as described in Table 107), DSP_TRST and DSP_TCK need to be handled in the same way as TRST and TCK are, as mentioned above.

3.10 Thermal

This section describes the thermal specifications.

3.10.1 Thermal Characteristics

Table 108 provides the package thermal characteristics.

Table 108. Package Thermal Resistance Characteristics

Characteristic	JEDEC Board	Symbol	Lid	Unit
Junction-to-Ambient Natural Convection	Single layer board (1s)	$R_{\theta JA}$	32–33	°C/W
Junction-to-Ambient Natural Convection	Four layer board (2s2p)	$R_{\theta JA}$	23–24	°C/W
Junction-to-Ambient (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	24–25	°C/W

Table 108. Package Thermal Resistance Characteristics (continued)

Characteristic	JEDEC Board	Symbol	Lid	Unit
Junction-to-Ambient (at 200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	18–19	°C/W
Junction-to-Board	—	$R_{\theta JB}$	12–13	°C/W
Junction-to-Case Top	—	$R_{\theta JCtop}$	<0.1	°C/W

Note:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

3.10.2 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

3.11 Security Fuse Processor

This device implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD1} pin per Section 2.2, "Power Sequencing." POV_{DD1} should only be powered for the duration of the fuse programming cycle, with a per device limit of one fuse programming cycle. All other times POV_{DD1} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD1} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD1} to GND.

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters

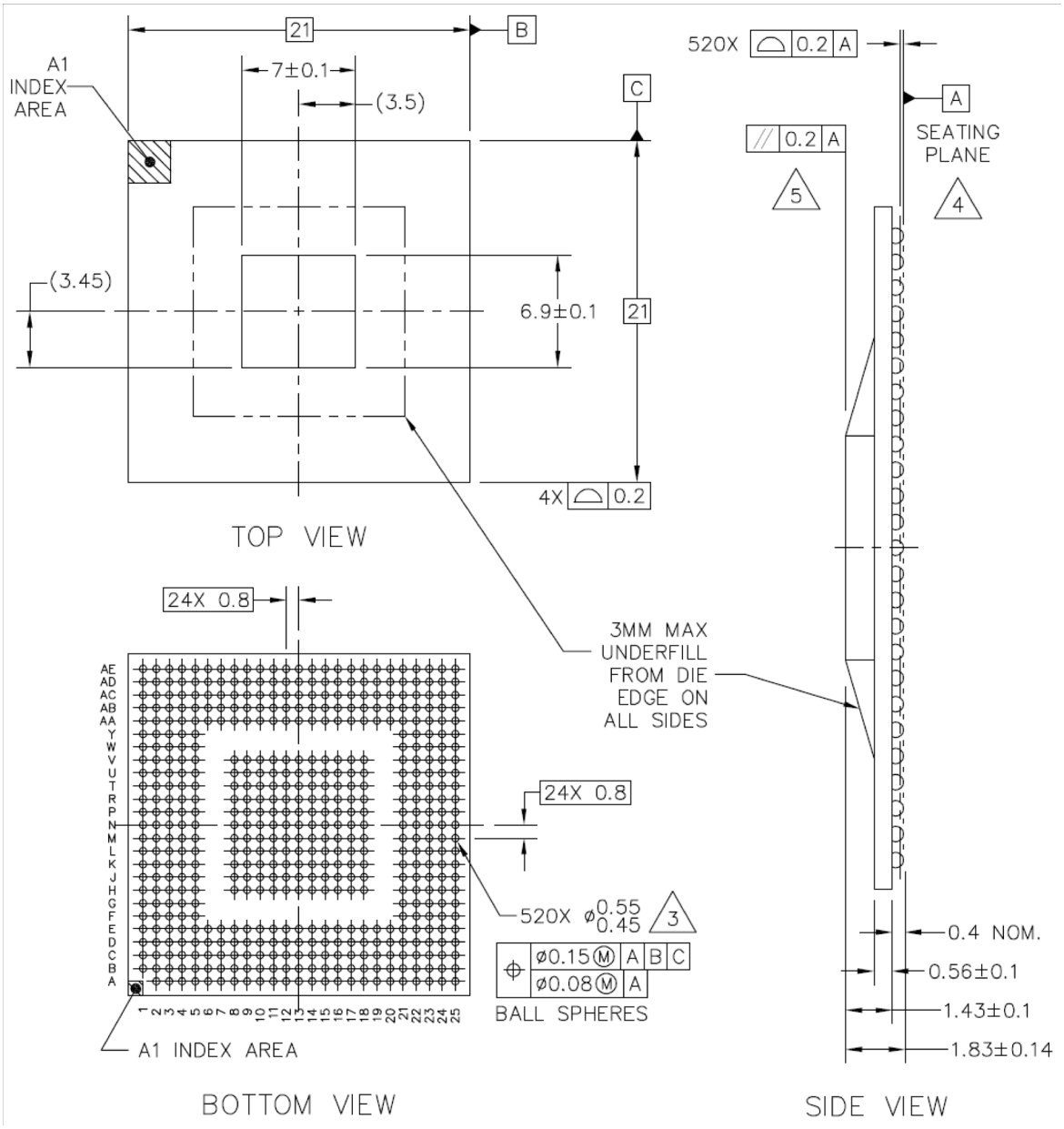
The package parameters are provided in the following list. The package type is plastic ball grid array (FC-PBGA).

Package outline	21 mm × 21 mm
Interconnects	520
Die Size	7.0 mm × 6.9 mm
Pitch	0.8 mm

Module height (typical)	1.83 mm
Ball diameter (typical)	0.4 mm

4.2 Mechanical Dimensions of the FC-PBGA

Figure 56 shows the package and bottom surface nomenclature.



Notes:
1. All dimentions are in milimeters.
2. Dimensions and tolerancing per ASME Y14.5-1994.
3. Maximum ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Figure 56. BSC9131 Mechanical Dimensions and Package Diagram

5 Ordering Information

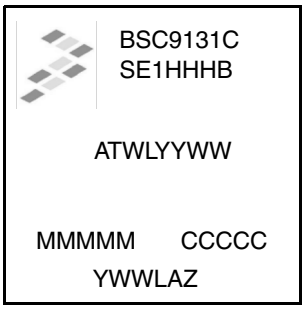
The table below provides the Freescale part numbering nomenclature for the BSC9131. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Each part number also contains a revision code which refers to the die mask revision number.

Table 109. Part numbering nomenclature

	n	*x*	*t*	*e*	*n*	*c*	*d*	*f*	*r*
Product code	**Part Identifier**	**Qual Status**	**Temp Range**	**Encryp-tion**	**Package Type**	**CPU Freq**	**DDR Speed**	**DSP Freq**	**Die Revision**
BSC	9131	C = Commercial Tier N = Industrial Tier	S, L = Std temp (0–105°C) X, J = Ext temp (-40–105°C)	E = SEC Present N = No SEC Present	1 = FC-PBGA Pb-free 7 = FC-PBGA Pb-free bumps and package	H = 800 MHz K = 1000 MHz	H = 800 MHz	H = 800 MHz K = 1000 MHz	B = Rev 1.1

5.1 Part Marking

Parts are marked as the example shown in this figure.



FCPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.
BSC9131CSE1HHHB is the orderable part number. See Table 109 for details.

Figure 57. Part Marking for FCPBGA Device

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part. Some documents may require a non-disclosure agreement. Contact your local FAE for assistance.

- *BSC9131 QorIQ Qonverge Multicore Baseband Processor Reference Manual* (BSC9131RM)
- *e500 PowerPC Core Reference Manual* (E500CORERM)

7 Revision History

Table 110. Document Revision History

Rev	Date	Substantive Change(s)
1	08/2015	• In Table 1, “BSC9131 Pinout Listing:” — Added references to footnote #1 in the “SPI3 over RF Interface,” and “SPI4 over RF Interface,” listings. — Added references to footnote #10 to the “RF Interface 1,” “RF Interface 2,” “RF Interface3,” and the “RF Serial (MaxPHY) Interface,” listings. — Added references to footnote #4 for signals ANT3_DIO01–ANT3_DIO06 — Renamed list heading “Programmable Interrupt Controller over ANT1” to “Programmable Interrupt Controller over RF Interface 1.” — Renamed list heading “Programmable Interrupt Controller over ANT3” to “Programmable Interrupt Controller over RF Interface 3.” — Renamed list heading “DMA over ANT2” to “DMA over RF Interface 2.” — Changed footnote #7 wording (was, “This pin is used for fuse programming. Should be tied to VSS for normal operation [fuse read]. See section Section 2.2, "Power Sequencing," for more details.” Is now, “POVDD2 and POVDD3 are always tied to GND.See section Section 2.2, "Power Sequencing," for more details.”). • In Table 2, “Absolute Maximum Ratings,” removed POV_{DD2} and POV_{DD3} from Fuse programming supply charasteristic. • In Table 109, “Part numbering nomenclature,” updated package type to include “7 = FC-PBGA Pb-free Bumps and Package.”
0	03/2014	Initial public release.

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