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DEVICE SPECIFICATION for
DIGITAL DBS TUNER with LINK

MODEL NO. BS2F7VZ7395

FOR CUSTOMER'S APPROVAL

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DATE	REF. PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	CHECK & APPROVAL
20. Mar. 2007	P9 6-3 Interface figure	△1	Add the description of IC's marking.	Y. Ieshima A. Yokoyama H. Ogino M. Noboru
23. May. 2007	P12 8-2	△2	Postscript to title. Describe clearly the PLL setting condition; "at every tuning".	Y. Ieshima A. Yokoyama H. Ogino M. Noboru
20. Jun. 2007	P17 Dimension and mounting details	△3	Add a screw hole(no tap) between RF in and out. History of aleteration(6th of Lot.No) is changed from "A" to "B". Apply after July 2007.	Y. Ieshima A. Yoko M. Noboru

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[DESCRIPTION] This specification covers DBS tuner intended for use in Digital Broadcasting Satellites. This tuner incorporates "LINK" section that is composed of DVB standard QPSK demodulation circuit and FEC (Forward Error Correction) circuit. This tuner has 8-bit transport stream output.

[1] GENERAL SPECIFICATIONS

1-1	Receiving frequency range		950MHz to 2150MHz
1-2	Input level		-65dBm to -25dBm
1-3	Input structure		F type Female
1-4	Nominal input impedance		75 ohm
1-5	Channel selection system		PLL synthesizer(Clock 4.0MHz)
1-6	Step frequency		500kHz
1-7	I/Q output LPF cut off frequency(-3dB)		10MHz to 30MHz, variable (2MHz step)
1-8	Symbol rate		2Msps to 45Msps
1-9	Roll-off Factor		35% (root-raised cosine)
1-10	LINK IC		STV0288 (Clock: 4MHz, Address: D0 (HEX))
1-11	FEC	Inner decoder:	Viterbi soft decoder, Constraint length M=7 Punctured codes 1/2, 2/3, 3/4, 5/6, 7/8 Automatic or manual rate and Phase recognition deinterleaver Word synchro extraction Convolutive deinterleaver
		Outer decoder:	Reed-solomon decoder, for 16 parity bytes Block lengths 204byte Energy dispersal descrambler
1-12	Absolute maximum ratings	(B2)	-0.30 to +4.00V DC
		(B3)	-0.30 to +3.63V DC
		(B4)	-0.30 to +4.00V DC
		(VDD)	-0.25 to +2.75V DC
1-13	Operating voltage		
	LNB voltage	(B1A, B1B)	25V, 400mA max
	Supply voltage	(B2)	3.3V +/- 0.165V DC
		(B3)	3.3V +/- 0.165V DC
		(B4)	3.3V +/- 0.165V DC
		(VDD)	2.5V +/- 0.125V DC
1-14	Circuit block diagram		Fig.1
1-15	Connection diagram		Fig.2
1-16	Mass		35g
1-17	Storage condition		
		Temperature	15 deg.C to 35 deg.C
		Humidity	25 %RH to 75 %RH
		Period	6 months
1-18	Environmental characteristics		RoHS compliant

(RoHS refers to the "DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.")

1-19 Attention items:

1) This unit contains components that can be damaged by electro-static discharge. Before handling this unit, ground your hands, tools, working desks and equipment to protect the unit from Electronic Static Destroy.

2) Avoid following actions;

a)to store this unit in the place of the high temperature and humidity.

b)to expose this unit to corrosive gases.

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[2] MECHANICAL SPECIFICATION

2-1 Dimension and mounting details Fig.3

2-2 Strength of F-connector No severe transform or distortion at bending moment, 98N・cm. To be connected electrically.

2-3 Clamp Torque of F-connector No severe transform or distortion on the connection with F-connector at bending moment, 98N・cm. To be connected electrically.

[3] ENVIRONMENTAL SPECIFICATION

(ELECTRICAL FUNCTIONAL OPERATION GUARANTEE)

3-1. Operating	Temperature	0 to +60 deg. C
	Humidity	Less than 85%
3-2. Storage	Temperature	-20 to +85 deg. C
	Humidity	Less than 95%

[Point to notice] Water vapor pressure 6643Pa max, no condensation
Please be careful that sudden temperature changes may cause condensation during storage, and such condensation may cause corrosion.

[4] TESTING CONDITION

4-1. Supply voltage	(B2)	3.3V +/- 0.05V
	(B3)	3.3V +/- 0.05V
	(B4)	3.3V +/- 0.05V
	(VDD)	2.5V +/- 0.05V
4-2. Ambient temperature		25 deg. C +/- 5 deg. C
4-3. Ambient humidity		65% +/- 10%

[5]ELECTRICAL SPECIFICATION (Unless otherwise stated testing condition 4-1 to 4-3.)

No.	Item		Specification				Condition
			MIN.	TYP.	MAX.	UNIT	
5-1	RF input VSWR			2.0	2.5		950M to 2150MHz
5-2	Noise figure(at max. gain)			8	12	dB	950M to 2150MHz
5-3	Intermodulation rejection Desired signal Fo Undesired signal (2 signals) (Fo+29.5MHz, Fo+59MHz) or (Fo-29.5MHz, Fo-59MHz)		40	60		dB	Input level:-25dBm I/Q output level: 0.6V_{P-P}(1kohm load) BBLPF:Fc=20MHz
5-4	L.O. leak at input terminal			-68	-63	dBm	950M to 2150MHz
5-5	Eb/No for BER = 2e-4 @viterbi_out	PC= 1/2		3.7	4.5	dB	4<Fs<45[Msps] (Fs :symbol rate)
		PC= 2/3		4.2	5.0		
		PC= 3/4		4.7	5.5		
		PC= 5/6		5.3	6.0		
		PC= 7/8		5.7	6.4		
		PC= 1/2		4.8	5.5	dB	2<Fs＜4[Msps]
		PC= 2/3		5.0	6.0		
		PC= 3/4		5.5	6.5		
		PC= 5/6		6.2	7.0		
		PC= 7/8		6.8	7.4		
5-6	PLL lock up time (C1,C0)=(1,1)			10	50	ms	
5-7	PLL phase noise (C1,C0)=(1,1)			-78	-70	dBc/Hz	10kHz offset
				-85	-78	dBc/Hz	100kHz offset

5-8	PLL reference leak			-40	-30	dBc	500kHz
5-9	RF output VSWR			2.0	2.5		950M to 2150MHz measured at RF out
5-10	RF output gain		-5	0	+5	dB	
5-11	Current consumption	B2		90	135	mA	B2=3.3V
		B3		34	112	mA	B3=3.3V
		B4		25	40	mA	B4=3.3V
		VDD		61	180	mA	VDD=2.5V

[6] PLL FUNCTION DESCRIPTION

PLL and VCO are promptly set up without fail when the user correctly program the data with the prompt I²C access sequence as long as the following are also applied;

a) Follow the I²C standard specification
b) Leave RTS to 0

6-1. I²C-BUS DATA FORMATS

Table 1; Write data format (MSB is transmitted first)

MSB							LSB		
1	1	0	0	0	0(MA1)	0(MA0)	0	A	Byte1
0	BG1	BG0	N8	N7	N6	N5	N4	A	Byte2
N3	N2	N1	A5	A4	A3	A2	A1	A	Byte3
1	1(C1)	1(C0)	PD5	PD4	TM	0(RTS)	1(REF)	A	Byte4
BA2	BA1	BA0	PSC	PD3	PD2/TS2	DIV/TS1	PD0/TS0	A	Byte5

* A	; Acknowledge bit	
* N8 to N1	; Programmable division ratio control bits	(see Table 3)
* A5 to A1	; Swallow division ratio setting bits	(see Table 4)
* REF	; Reference division ratio setting bits	(see Table 5)
* PSC	; Prescaler division ratio setting bits	(see Table 6)
* MA1, MA0	; Address setting bits	(see Table 7)
* PD0	; PO control bit	(see Table 8)
* BA2, BA1, BA0	; Local oscillator select	(see Table 9)
* DIV	; Local oscillator divided ratio setting	(see Table 9)
* PD5 to PD2	; BB LPF cut-off frequency setting	(see Table 10)
* RTS	; Test mode control bit	(see Table 11)
* TS2, TS1, TS0	; Test mode setting bits (when RTS = '1')	(see Table 11)
* C1, C0	; Charge pump current setting bits	(see Table 12)
* BG1, BG0	; BB AMP gain setting bits	(see Table 13)
* TM	; VCO/LPF adjustment mode setting bits	(see section [8])

Write PLL register data to set one among the following I²C access sequence as #a) to h).
It is available to skip the bytes which does not require for renewal or change the sequence of the bytes to choose one of the following.

I²C start->1st byte->2nd byte->3rd byte->4th byte->5th byte

a) I²C start -> byte1 -> byte2 -> byte3 -> byte4 -> byte5 * byte1: I²C address byte
b) I²C start -> byte1 -> byte4 -> byte5 -> byte2 -> byte3 *
c) I²C start -> byte1 -> byte2 -> byte3 -> byte4 -> either I²C stop or (another) start
d) I²C start -> byte1 -> byte4 -> byte5 -> byte2 -> either I²C stop or (another) start
e) I²C start -> byte1 -> byte2 -> byte3 -> either I²C stop or (another) start
f) I²C start -> byte1 -> byte4 -> byte5 -> either I²C stop or (another) start
g) I²C start -> byte1 -> byte2 -> either I²C stop or (another) start
h) I²C start -> byte1 -> byte4 -> either I²C stop or (another) start

*: Either I²C stop or (another) start is available to follow after the 5th byte, but not mandatory

(Caution): During receiving signals, don't access I²C bus to satisfy the phase noise character specification.

(Note): PLL set up rules

The following conditions are required to program the I²C access sequence.
According to a required renewal data on each byte, one of the access sequence shown above as a) to h) should be chosen.

1) Write byte1 on the 1st byte after I²C start.
2) Write either byte2 or byte4 on the 2nd byte.
   When the MSB header is 0 on the 2nd byte, the 2nd byte is recognized as byte2.
   When the MSB header is 1 on the 2nd byte, the 2nd byte is recognized as byte4.
3) The following byte after byte2 or byte4 should be the sequent # of the last byte as;
   The byte3 should be followed after byte2.
   The byte5 should be followed after byte4.
4) The number of byte to write in one access sequence as from a start to a stop (or another start) state should be two bytes at least. Review #g) and #h).
   Maximum bytes are five as write all byte1 to byte5 data in one access sequence. Review #a) and #b)
5) The renewal of the register data is only available when it becomes an I²C stop or another start state after all the bytes to write in case of #c) to h).
   Only in the case when the renewal of the register data all from byte2 to byte5 in one access sequence as #a) and #b), a stop state or another start state is not mandatory required for data renewal.
6) The data already registered and not to write for renewal has kept as it is as the last state.
7) Every time when the power is on, write all the register data on byte2 to byte5 in one sequence for the purpose of the initial default set up to follow either #a) or #b). Because the initial values on byte2 to byte5 are not fixed before the initialization.

Table 2; Read data format

MSB							LSB		
1	1	0	0	0	MA1	MA0	1	A	Byte1
POR	FL	RD2	RD1	RD0	X	X	X	A	Byte2

* POR ; Power on reset indicator (see table 14)
* FL ; Phase lock detect flag (see table 15)
* RD2 – RD0 ; Reserved (These bit values change under the condition of ICs.)
* X ; don't care
* All data of byte2 will be "H", when "Power on reset" operates
* "Read mode" will change to "Write mode" after completing to output the byte2.

6-2. PROGRAMING

6-2-1 Programmable divider bits data

Please set P, N, A, R as follows.

$$fvco=[(P*N)+A]*fosc/R$$

fvco : Receiving frequency
P : Dividing factor of prescaler (16 or 32)
N : Programmable division ratio (5 to 255)
A : Swallow division ratio (0 to 31 and A < N)
fosc : Reference oscillation frequency (4 MHz)
R : Reference division ratio (see table 5)

6-2-2 Data setting

Table 3; Programmable division ratio control (Binary: 8 bits)

Dividing factor (N)	Bit data							
	N8	N7	N6	N5	N4	N3	N2	N1
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
・	・	・	・	・	・	・	・	・
255	1	1	1	1	1	1	1	1

Table 4; Swallow division ratio setting (Binary: 5 bits)

Dividing factor (A)	Bit data				
	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
・	・	・	・	・	・
31	1	1	1	1	1

* The using of 4 or smaller dividing factors is inhibited.
* The dividing factor is set by the data of N8 to N1 and A5 to A1 in byte2, 3 on I²C write data.

Table 5; Reference division ratio setting (Binary: 1 bit)

REF	Dividing factor (R)	Compare frequency	fvco(MHz)
0	4	1 MHz	1024 – 2150 MHz*
1	8	500 kHz	950 – 2150 MHz

Caution: Only use REF=1

*When the reference division ratio set to 4(REF = '0'), the fvco's minimum frequency must be higher than 1024 MHz (including 1024 MHz). If the frequency is lower than 1023 MHz, the condition mentioned in section 6-2-1 "A < N" is not satisfied.
But all receiving ranges can be covered with combination with PSC setting. (see Table 6)

Table 6; Prescaler division ratio setting (Binary: 1 bit)

PSC	Dividing factor (P)	fvco
0	32	950 - 2150 MHz
1	16	950 - 1375 MHz*

The dividing factor is set by the data of PSC in byte 5 on I²C write data.

*When the prescaler division ratio of the prescaler is set to 16(PSC = '1'), the fvco's maximum frequency must be lower than 1375 MHz (including 1375 MHz). This fvco's maximum frequency limitation is depended on the operation frequency of the internal programmable counter.
Refer to Table 9 about PSC detailed setting.

Table 7; Address selection (Binary: 2 bits)

Bit		ADR input voltage
MA1	MA0	
0	0	0V to 0.1*B2
0	1	open
1	0	0.4*B2 to 0.6*B2
1	1	0.9*B2 to B2

* The address of this tuner is C0(h).

Table 8; PO control (Binary: 1 bit)

Bit	Output of PO		
PD0	Normal	Power on reset	Power on
1	L	Hi-Z	Hi-Z
0	Hi-Z	Hi-Z	

Hi-Z : High impedance

Table 9; Local oscillator select

BAND	DIV	BA2	BA1	BA0	Local frequency (Receiving frquency)	Divider ratio
1	1	1	1	0	950MHz to 1065MHz	1/4
2	1	1	1	1	1065MHz to 1170MHz	1/4
3	0	0	0	1	1170MHz to 1300MHz	1/2
4	0	0	1	0	1300MHz to 1445MHz	1/2
5	0	0	1	1	1445MHz to 1607MHz	1/2
6	0	1	0	0	1607MHz to 1778MHz	1/2
7	0	1	0	1	1778MHz to 1942MHz	1/2
8	0	1	1	0	1942MHz to 2150MHz	1/2

Table10 ; Baseband LPF cut-off frequency setting

PD2	PD3	PD4	PD5	LPF cut-off Frequency
0	0	1	1	10 MHz
0	1	0	0	12 MHz
0	1	0	1	14 MHz
0	1	1	0	16 MHz
0	1	1	1	18 MHz
1	0	0	0	20 MHz
1	0	0	1	22 MHz
1	0	1	0	24 MHz
1	0	1	1	26 MHz
1	1	0	0	28 MHz
1	1	0	1	30 MHz

Table 11; Test mode setting

Register Bit				Test mode
RTS	TS2	TS1	TS0	
0	X	X	X	Normal operation
1	Don't use			Reserved (Test Mode)

X: don't care

* When RTS=1 on "I²C write data (table 1)", it changes to test mode.

Table 12; Charge pump output current selection

Bit		Charge pump output current [μA]		
C1	C0	min	typ	max
0	0	±78	±120	±150
0	1	±169	±260	±325
1	0	±360	±555	±694
1	1	±780	±1200	±1500

Table 13; Baseband AMP gain control (Depend on PLL register setting)

BG1	BG0	ATTENUATION (Typ.)
0	0/1	0
1	0	–2 dB
1	1	–4 dB

Table 14; POR bit polarity

	VCC3 > 2.2V	VCC3 < 2.2V
POR bit	L	H

Table 15; FL bit polarity

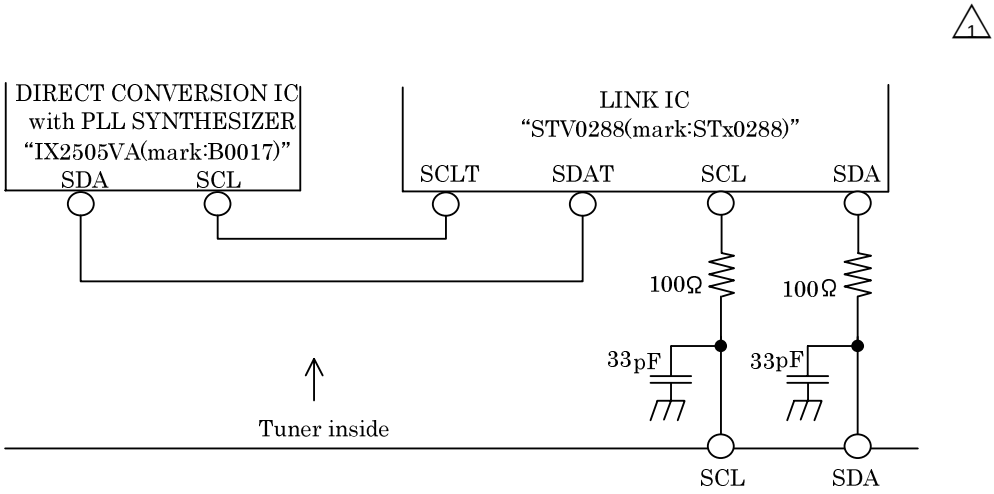
	lock	unlock
FL bit	H	L

* SDA has to be pulled up.

6-3. INTERFACE CIRCUITS

Table 16; Internal interface of I²C bus

Tuner pin No.	I²C port	Note
8	SDA	Refer to following figure
9	SCL	



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[7] CONFIGURATION REGISTERS

Table 17; STV0288's Test Register Value

address [H]	data [H] 27.5Msps	data [H] 5Msps
00	n/a	n/a
01	15	15
02	20	20
03	8E	8E
04	8E	8E
05	12	12
06	00	00
07	n/a	n/a
08	n/a	n/a
09	00	00
0A	04	04
0B	00	00
0C	00	00
0D	00	00
0E	C4	C4
0F	54	54
10	n/a	n/a
11	7A	7A
12	03	03
13	48	48
14	84	84
15	45	45
16	B7	B7
17	9C	9C
18	00	00
19	A6	A6
1A	88	88
1B	8F	8F
1C	F0	F0
1E	n/a	n/a
1F	n/a	n/a
20	0B	0B
21	54	54
22	00	00
23	00	00
24	n/a	n/a
25	n/a	n/a
26	n/a	n/a
27	n/a	n/a
28	46	0C
29	65	CC
2A	E0	B0
2B	FF	FF
2C	F7	F7
2D	n/a	n/a
2E	n/a	n/a
2F	n/a	n/a

address [H]	data [H] 27.5Msps	data [H] 5Msps
30	00	00
31	1E	1E
32	14	14
33	0F	0F
34	09	09
35	0C	0C
36	05	05
37	2F	2F
38	16	16
39	BD	BD
3A	00	00
3B	13	13
3C	11	11
3D	30	30
3E	n/a	n/a
3F	n/a	n/a
40	63	63
41	04	04
42	60	60
43	00	00
44	00	00
45	00	00
46	00	00
47	00	00
4A	00	00
4B	n/a	n/a
4C	n/a	n/a
50	10	10
51	38	38
52	21	21
53	A2	86
54	D9	56
55	23	06
56	8D	76
57	1B	05
58	54	54
59	86	86
5A	00	00
5B	9B	9B
5C	08	08
5D	7F	7F
5E	00	00
5F	FF	FF
60	n/a	n/a
61	n/a	n/a
62	n/a	n/a
63	n/a	n/a

address [H]	data [H] 27.5Msps	data [H] 5Msps
64	n/a	n/a
65	n/a	n/a
66	n/a	n/a
67	n/a	n/a
68	n/a	n/a
69	n/a	n/a
6A	n/a	n/a
6B	n/a	n/a
6C	n/a	n/a
70	00	00
71	00	00
72	00	00
74	00	00
75	00	00
76	00	00
81	00	00
82	3F	3F
83	3F	3F
84	00	00
85	00	00
88	00	00
89	00	00
8A	00	00
8B	00	00
8C	00	00
90	00	00
91	00	00
92	00	00
93	00	00
94	1C	1C
97	00	00
A0	48	48
A1	00	00
B0	B8	B8
B1	3A	3A
B2	10	10
B3	82	82
B4	80	80
B5	82	82
B6	82	82
B7	82	82
B8	20	20
B9	00	00
F0	00	00
F1	00	00
F2	C0	C0

<note>

(1) The data field with " n/a " stands for "read only register". No need to write, no malady with writing.

(2) Some register bit should be swiched "1" and "0", duaring the signal search.
Ex) I²C bus repeater [address:01/bit7] : OFF=0/ON=1

(3) symbol_frequency : SFRH,M,L[address:28,29,2A] = symbol_frequency / F_{M_CLK} [100MHz] x 2^{20}

(4) F_{M_CLK} : f_{pll} = fxtal x (PLL_DIV)/4 when PLL_SELRATIO = 1
f_{pll} = fxtal x (PLL_DIV)/6 when PLL_SELRATIO = 0
(# fxtal = 4MHz , PLL_SELRATIO[address:41,bit2])

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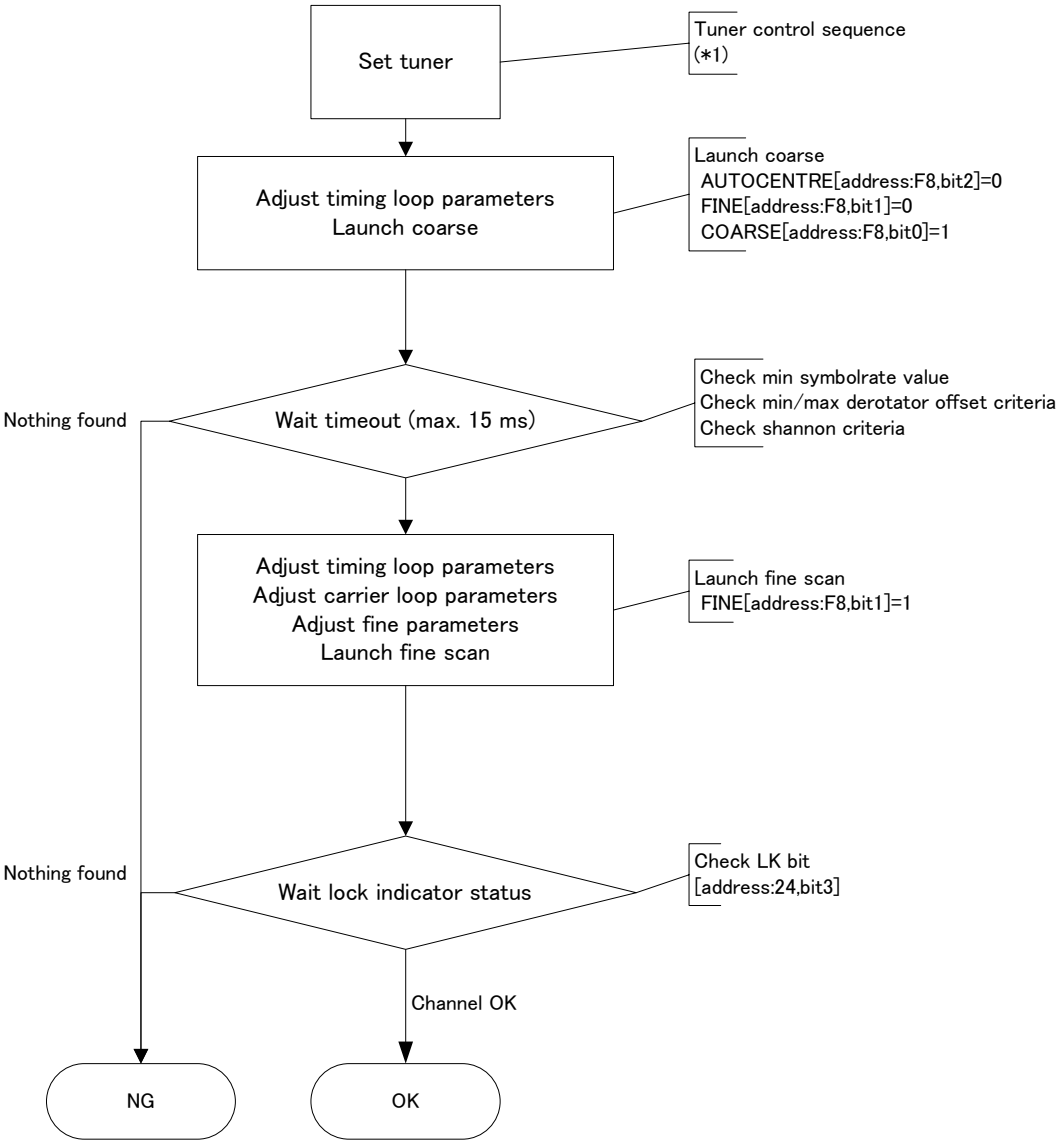
[8]TUNER CONTROL PROCEDURE
8-1 FLOW CHART



*1 Tuning details is shown in the next section.

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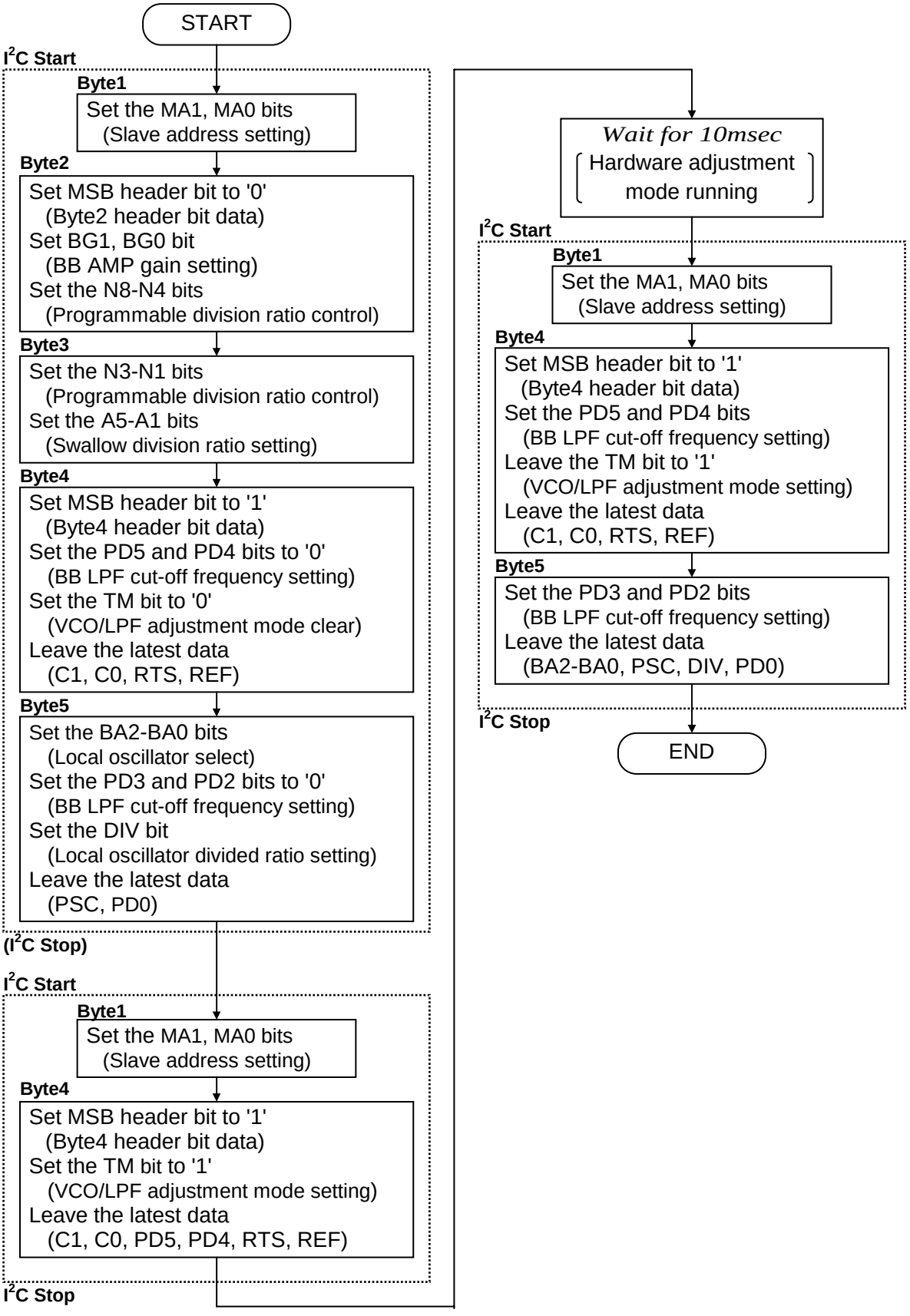
8-2 VCO and LPF ADJUSTMENT MODE SETTING SEQUENCE AFTER POWER ON and AT EVERY TUNING △2



[9] Reliability

9-1. High temperature high humidity load (40deg.C, 90% RH, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After cycling DUT in the constant chamber at 40deg.C/90-95% RH in on state, for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 19.
4) The contact resistance of F-connector must be less than 0.02 ohm. (*)

9-2. High temperature load (70deg.C, 40% RH, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant chamber at 70+/-2deg.C/40% RH for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 19.

9-3. Cold test (-25deg.C, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant temperature chamber at -25deg.C for 500h, leave the DUT at room temperature and humidity for 2h and then measure the values after test.
3) Must meet the specifications of Table 19.

9-4. Shock (686 m/s^2, 6 planes, 3 times)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the shock tester, apply shock of 686 m/s^2 three times to each of 6 planes and then measure the values.
3) Must meet the specifications of Table 19.
4) This test is to be conducted using a single tuner.

9-5. Vibration (10-55 Hz, 1.5 mm, in each of three mutually perpendicular directions, each 2 times)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the vibration tester, apply motion having an amplitude of 1.5 mm (constant), the frequency being varied uniformly between 10 and 55 Hz, to DUT, for 2h in each of three mutually perpendicular directions (X, Y and Z, total of 6h). After the test, measure the values.
3) Must meet the specifications of Table 19.
4) This test is to be conducted using a single tuner.

9-6. Heat shock test (1 cycle=1h (-20deg.C; 0.5h, 70deg.C;0.5h), 50 cycles))

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) Using the heat shock tester, apply heat shock to DUT. After the test, measure the values.
3) Must meet the specifications of Table 19.
4) The contact resistance of F-connector must be less than 0.02 ohm. (*)

9-7. Solderability of terminal

Pretreatment of heating terminal at 150deg.C for 1h is performed and leave it at room temperature for 2h or longer. Immerse 1.9 mm length of terminal (from the tip) to be soldered into rosin (JIS-K-5902), isopropyl alcohol (JIS-K-8839 or JIS-K-1522, rosin concentration (10-35% range) approx. 25% by weight unless otherwise specified) or equivalent solution for 3–5s, and then immerse the length of the terminal into a pool of molten solder (Sn/3.0Ag/0.5Cu, or equivalent) at 240 +/-2deg.C for 3s.Dipped terminal portion shall be wetted by more than 95%.
(Excluding the cutting plane of the chassis)

9-8. Soldering heat resistance

Immerse the terminal mounted on a PCB (1.6t thick) into solder at 350±5deg.C for 3.0-3.5 seconds or at 260 +/-5deg.C for 10 +/-1 seconds. Remove the PCB from the solder and leave it for 1 hour at room temperature. The test sample shall show no degradation in appearance and electrical characteristics.

9-9. ESD protection

Table 18; ESD Test Condition (IEC61000-4-2 Compliant)

terminal	Limits	condition
RF_IN (coaxial center)	+/-6kV DC	Air discharge 150pF/330ohm, each 5 times
Others	+/-200V DC	Contact discharge 150pF/330ohm, each 5 times

Table 19

item	specification	condition
Eb/No	(initial values)+/-1dB	BER = 2e-4 at viterbi output PC=3/4

(*)Method of measuring contact resistance

Center-contact

Insert the gauge pin(ϕ 0.8mm) to F-connector.

Measure the resistance between the gauge and the center-contact of F-connector.

Outer-shell

Connect the plug(3/8-32 UNEF-2B) to F-connector at 29.4N・cm of the clamping torque.

Measure the resistance between the plug and chassis.

(Measuring device: Milliohm meter)

・F-connector is made from iron. If the plating is peeled off, rust might occur to surface of F-connector. But it makes no influence of electric specifications, under contact resistance is less than 0.02 ohm.

・The cutting plane of chassis and shield cover is not plated, therefore rust might occur. But it makes no influence of electric specifications.

SHARP

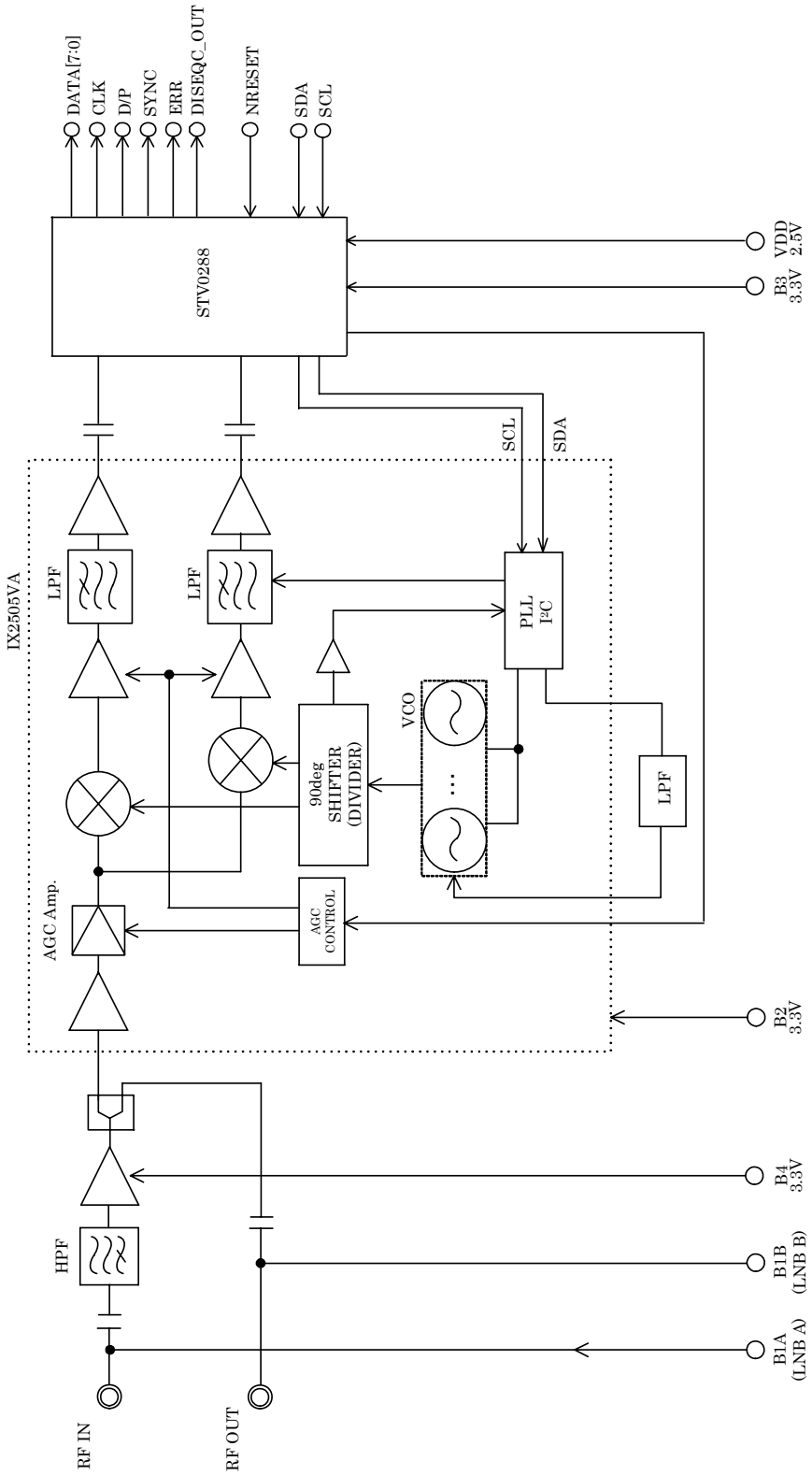


Fig 1. BLOCK DIAGRAM

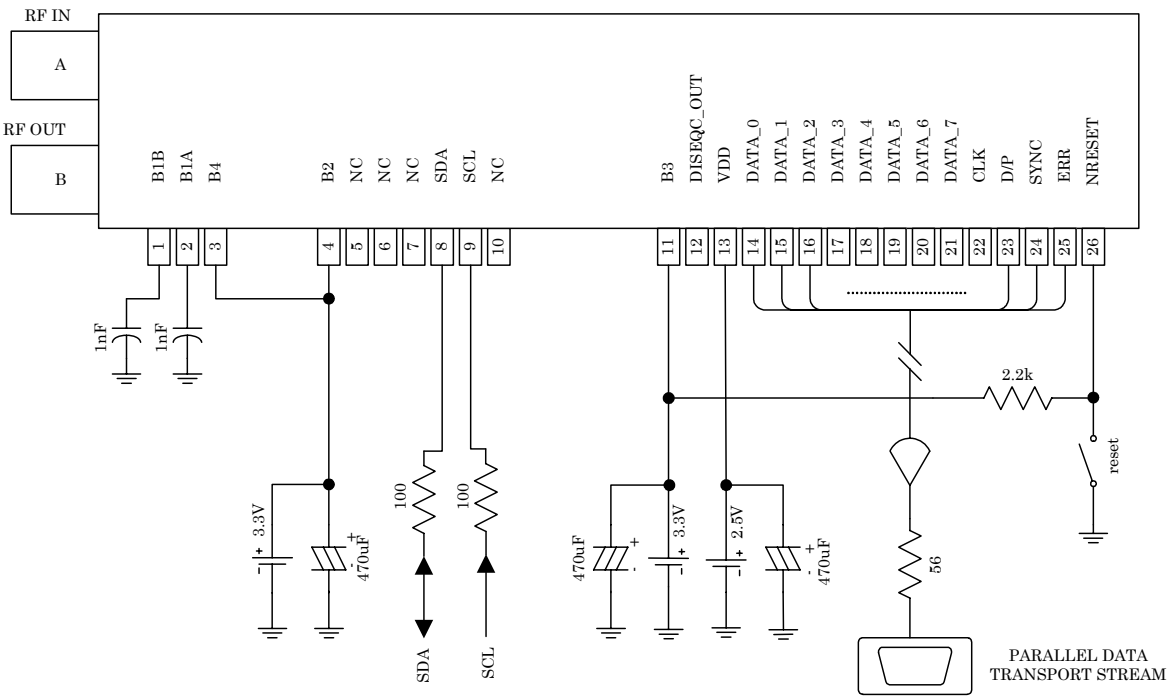


Fig 2. CONNECTION DIAGRAM

PIN LIST

PIN NAME	PIN No.	PIN DESCRIPTION
B1B	1	Voltage supply of LNB B. Please ground it with a 1000pF ceramic capacitor.
B1A	2	Voltage supply of LNB A. Please ground it with a 1000pF ceramic capacitor.
B4	3	3.3V supply for RF Booster Amp of tuner.
B2	4	3.3V supply for the RF section. Please keep a ripple at the Power Supply less than 10mVp-p.
NC	5,6,7,10	It is not connected inside the unit. We advice to ground it.
SDA	8	I²C bus. Please connect a pull-up resistor which is more than 2k ohm outside of the tuner.
SCL	9	
B3	11	3.3V supply for STV0288
DISEQC_OUT	12	Pulse output for LNB
VDD	13	2.5V supply for STV0288
DATA[7:0]	14,...,21	Transport stream (TS) parallel data
CLK	22	Transport stream byte clock.
D/P	23	Transport stream data valid signal
SYNC	24	Transport stream sync bit
ERR	25	Transport stream packet error signal
NRESET	26	Reset signal input active low

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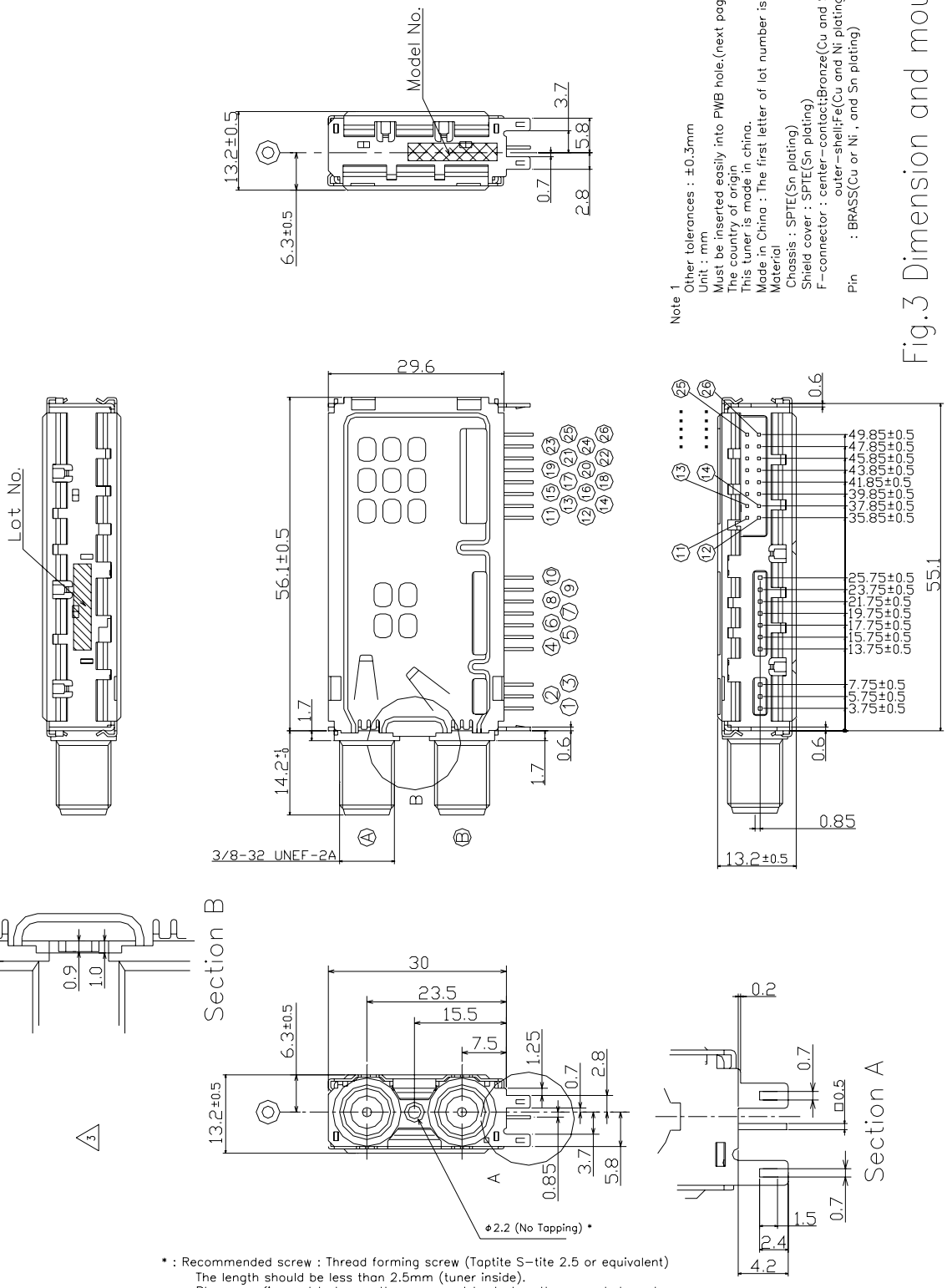
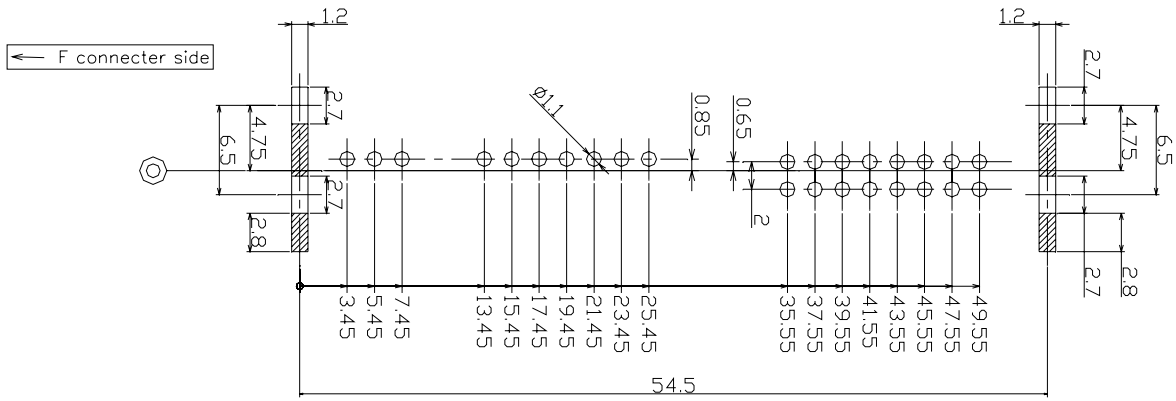
Fig.3 Dimension and mounting details



Note 1
Other tolerances : ±0.3mm
Unit : mm
Must be inserted easily into PWB hole.(next page)
The country of origin
This tuner is made in china.
Made in China : The first letter of lot number is " W "
Material
Chassis : SPTE(Sn plating)
Shield cover : SPTE(Sn plating)
F-connector : center-contact;Bronze(Cu and Sn plating)
outer-shell;Fe(Cu and Ni plating)
Pin : BRASS(Cu or Ni , and Sn plating)

* : Recommended screw : Thread forming screw (Taptite S-tite 2.5 or equivalent)
The length should be less than 2.5mm (tuner inside).
Please confirm not to loosen the screw, not to destroy the screw hole and
not to generate chips of chassis causeing short-circuit.

Recommended dimension of pin holes on mother PWB.
(Viewed from mounting side)
– Reference drawing –



Unit : mm

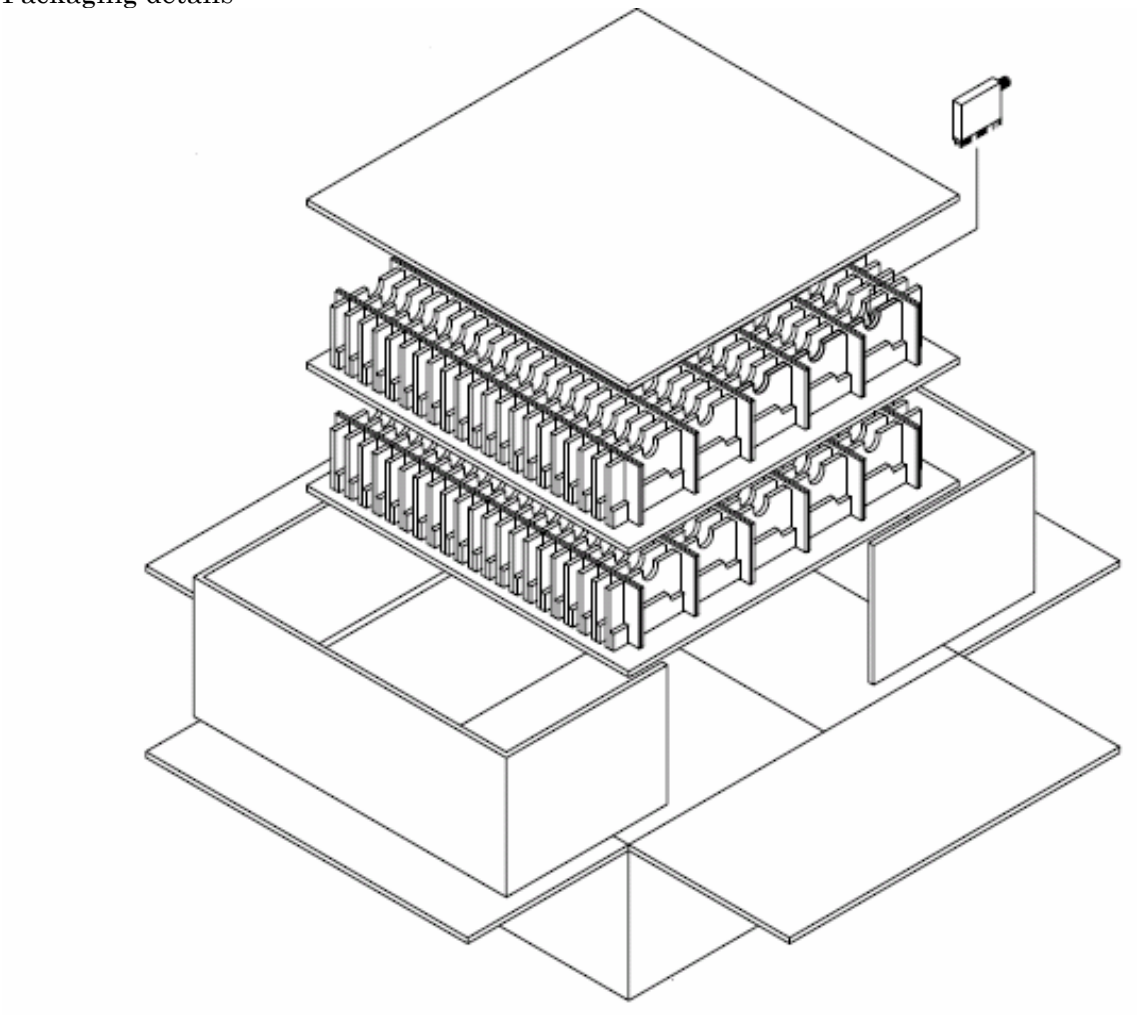
DEAD SPACE

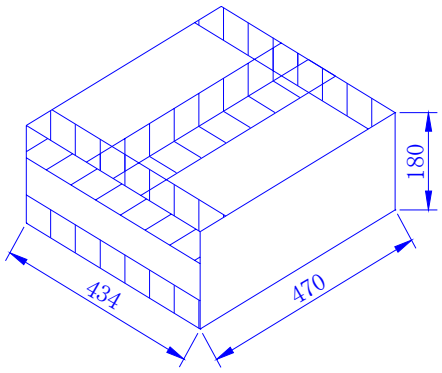
(Do not wire the signal line etc. through this area to prevent the short–ciucuit to chassis)

SHARP PROPRIETARY

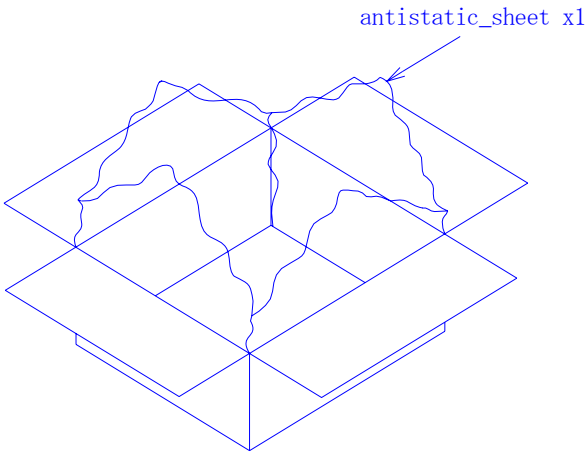
SHARP

Packaging details





<Reference drawing>



UNIT :mm
QUANTITY :200pcs