



晶丰明源半导体

BPM0306CG

30V Complementary MOSFET

General Description

The BPM0306CG uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs can be used in a wide variety of applications.

Application

- H-bridge
- Inverters

Features

- **N-Channel**
 $V_{DS} = 30V$, $I_D = 6.5A$
 $R_{DS(ON)} < 30m\Omega$ @ $V_{GS} = 10V$
- **P-Channel**
 $V_{DS} = -30V$, $I_D = -7A$
 $R_{DS(ON)} < 33m\Omega$ @ $V_{GS} = -10V$
- High power and current handing capability

Typical Application

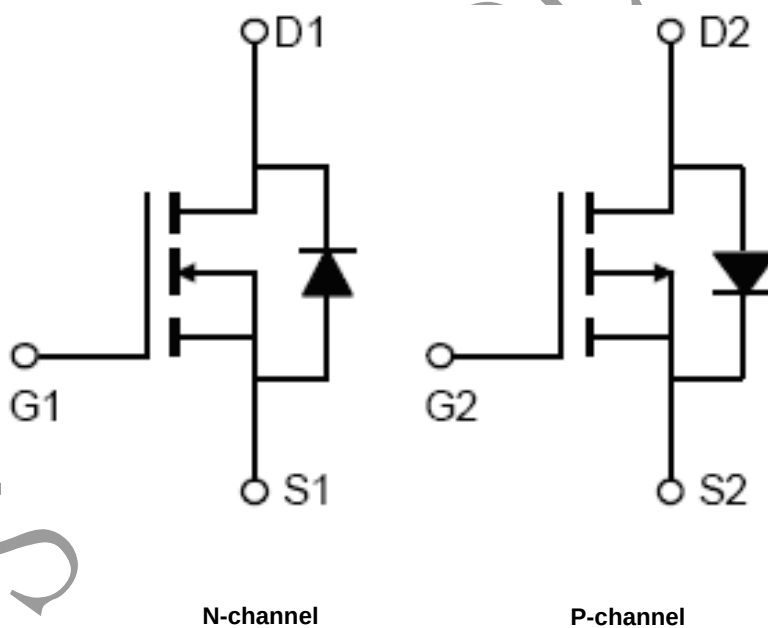


Figure 1. Schematic Diagram

Ordering Information

Part Number	Package	Operating Temperature	Packing Type	Marking
BPM0306CG	SOP-8	-40 °C to 105 °C	Tape & Reel 4,000pcs/Reel	BPM0306 XXXXXY CGXWW

Pin Configuration and Marking Information

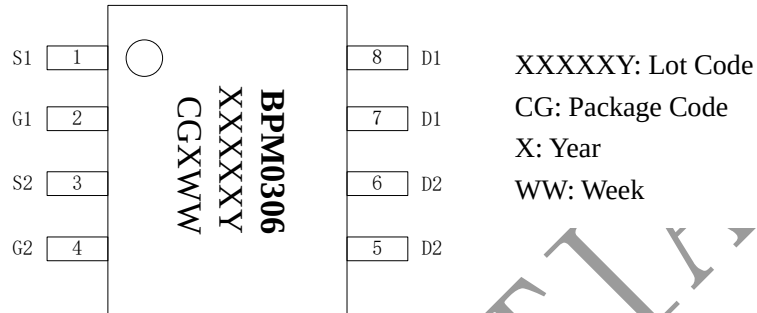


Figure 2. Pin Configuration

Pin Definition

Pin No.	Name	Description
1	S1	NMOS Source
2	G1	NMOS Gate
3	S2	PMOS Source
4	G2	PMOS Gate
5	D2	PMOS Drain
6	D2	PMOS Drain
7	D1	NMOS Drain
8	D1	NMOS Drain

Absolute Maximum Rating (note 1) (Unless otherwise specified, $T_A=25^{\circ}\text{C}$)

Symbol	Parameter	N-Channel	P-Channel	Unit
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D	Continuous Drain Current	$T_C=25^{\circ}\text{C}$	6.5	A
		$T_C=70^{\circ}\text{C}$	5.4	
I_{DM}	Pulsed Drain Current (note 2)	30	-30	A
P_D	Maximum Power Dissipation	$T_C=25^{\circ}\text{C}$	2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (note 3)	62.5	62.5	$^{\circ}\text{C/W}$

Note 1: Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Under “recommended operating conditions” the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation range of the device, the electrical characteristics is assured on DC and AC voltage by the test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.



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Note 2: Repetitive Rating: Pulse width limited by maximum junction temperature.

Note 3: Surface Mounted on FR4 Board, $t \leq 10$ sec.

N-Channel Electrical Characteristics (note 4, 5) (Unless otherwise specified, $T_A=25^\circ\text{C}$)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	30	33	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 6)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	1.6	3	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =6A	-	20	30	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =6A	15	-	-	S
Dynamic Characteristics (Note7)						
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	255	-	PF
C _{oss}	Output Capacitance		-	45	-	PF
C _{rss}	Reverse Transfer Capacitance		-	35	-	PF
Switching Characteristics (Note 7)						
t _{d(on)}	Turn-on Delay Time	V _{DD} =15V, R _L =2.5Ω V _{GS} =10V, R _{GEN} =3Ω	-	4.5	-	nS
t _r	Turn-on Rise Time		-	2.5	-	nS
t _{d(off)}	Turn-Off Delay Time		-	14.5	-	nS
t _f	Turn-Off Fall Time		-	3.5	-	nS
Q _g	Total Gate Charge	V _{DS} =15V, I _D =6A, V _{GS} =10V	-	13	-	nC
Q _{gs}	Gate-Source Charge		-	5.5	-	nC
Q _{gd}	Gate-Drain Charge		-	3.5	-	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage (Note 6)	V _{GS} =0V, I _S =6A	-	0.8	1.2	V



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P-Channel Electrical Characteristics(note 4, 5) (Unless otherwise specified, T_A=25℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =-250μA	-30	-33	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 6)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-1.9	-2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =-10V, I _D =-6.5A	-	28	33	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-6.5A	10	-	-	S
Dynamic Characteristics (Note7)						
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, F=1.0MHz	-	520	-	PF
C _{oss}	Output Capacitance		-	100	-	PF
C _{rss}	Reverse Transfer Capacitance		-	65	-	PF
Switching Characteristics (Note 7)						
t _{d(on)}	Turn-on Delay Time	V _{DD} =-15V, R _L =2.3Ω V _{GS} =-10V, R _{GEN} =6Ω	-	7.5	-	nS
t _r	Turn-on Rise Time		-	5.5	-	nS
t _{d(off)}	Turn-Off Delay Time		-	19	-	nS
t _f	Turn-Off Fall Time	V _{DS} =-20V, I _D =-6.5A, V _{GS} =-10V	-	7	-	nS
Q _g	Total Gate Charge		-	9.2	-	nC
Q _{gs}	Gate-Source Charge		-	1.6	-	nC
Q _{gd}	Gate-Drain Charge		-	2.2	-	nC
Drain-Source Diode Characteristics						
V _{SD}	Diode Forward Voltage (Note 6)	V _{GS} =0V, I _S =-6.5A	-	-0.8	-1.2	V

Note 4: Production testing of the chip is performed at 25℃.

Note 5: The maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.

Note 6: Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

Note 7: Guaranteed by design, not subject to production

N-Channel Typical Electrical and Thermal Characteristics Curves

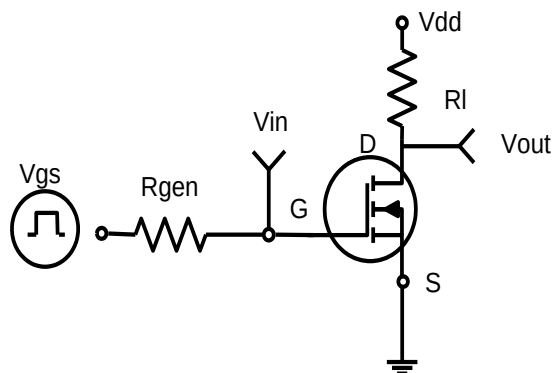


Figure 3. Switching Test Circuit

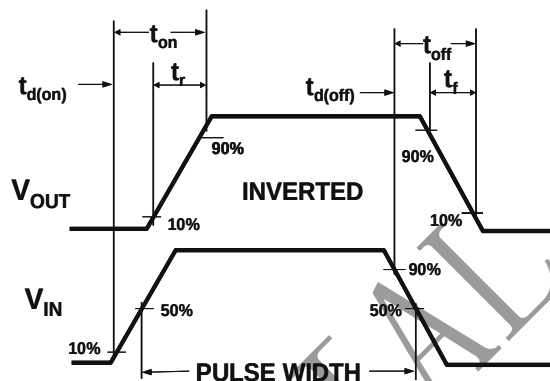


Figure 4. Switching Waveforms

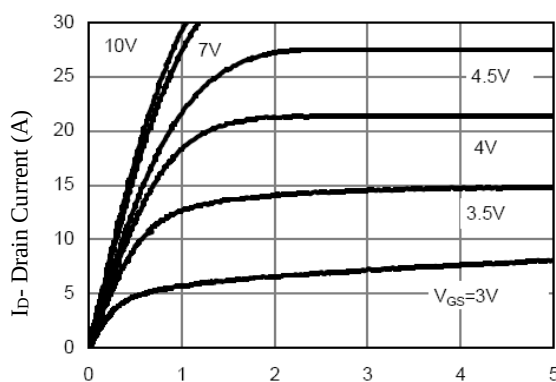


Figure 5. Output Characteristics

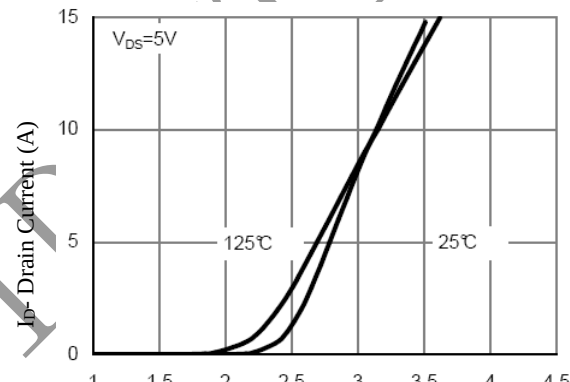


Figure 6. Transfer Characteristics

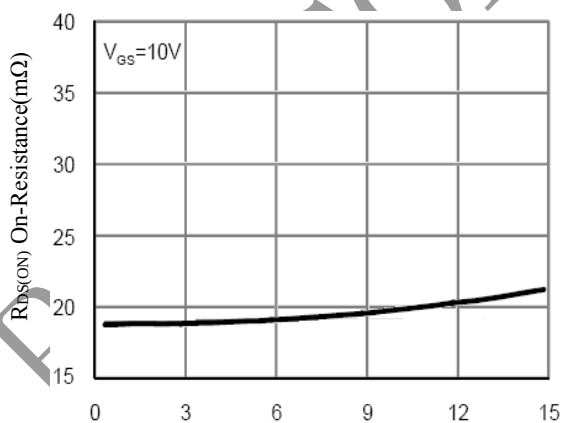


Figure 7. Drain-Source On-Resistance

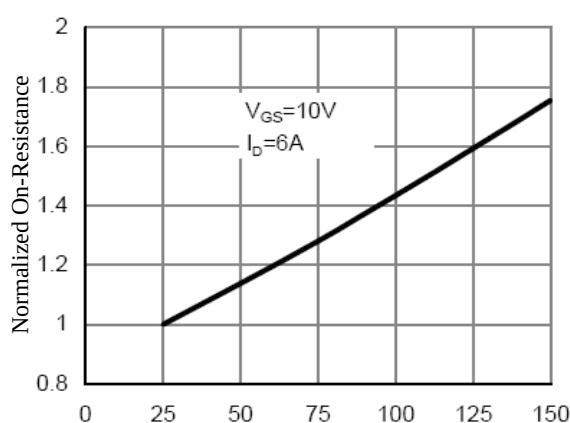


Figure 8. Drain-Source On-Resistance



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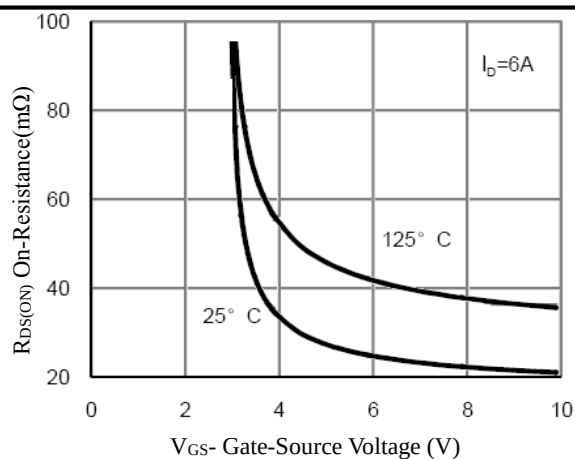


Figure 9. $R_{DS(ON)}$ vs V_{GS}

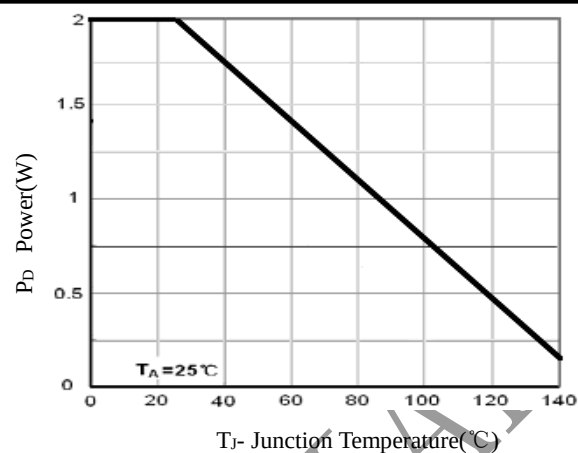


Figure 10. Power Dissipation

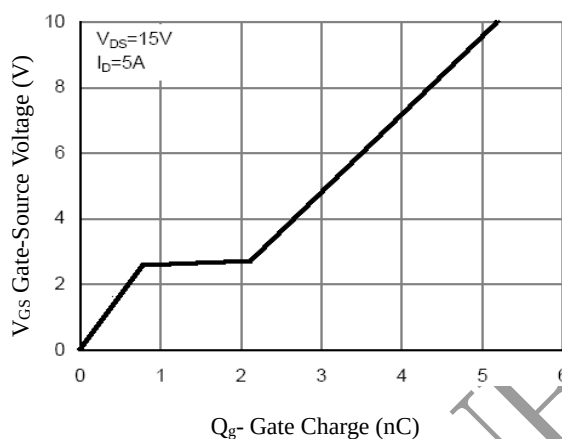


Figure 11. Gate Charge

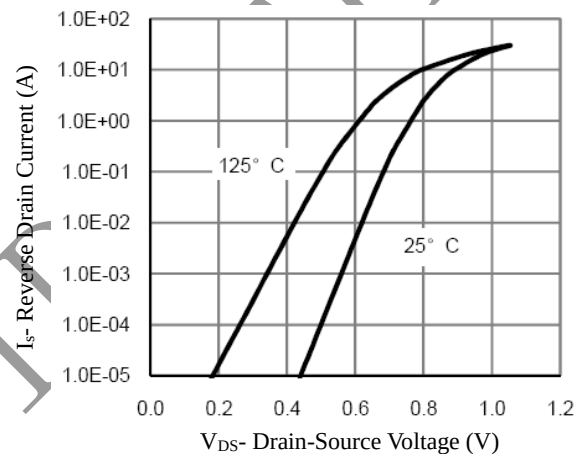


Figure 12. Source- Drain Diode Forward

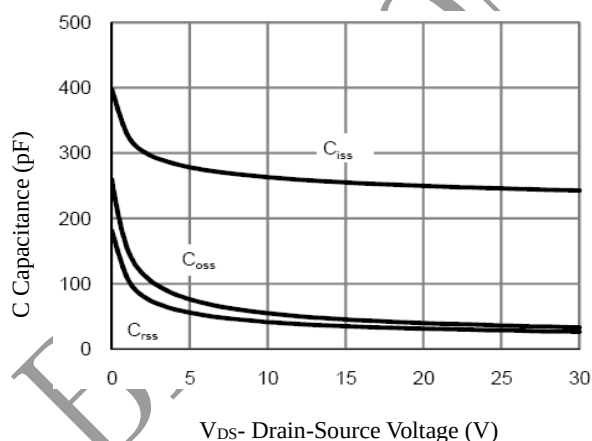


Figure 13. Capacitance vs V_{ds}

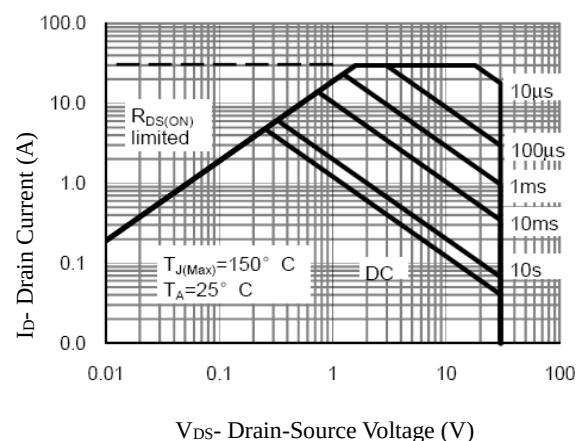


Figure 14. Safe Operation Area

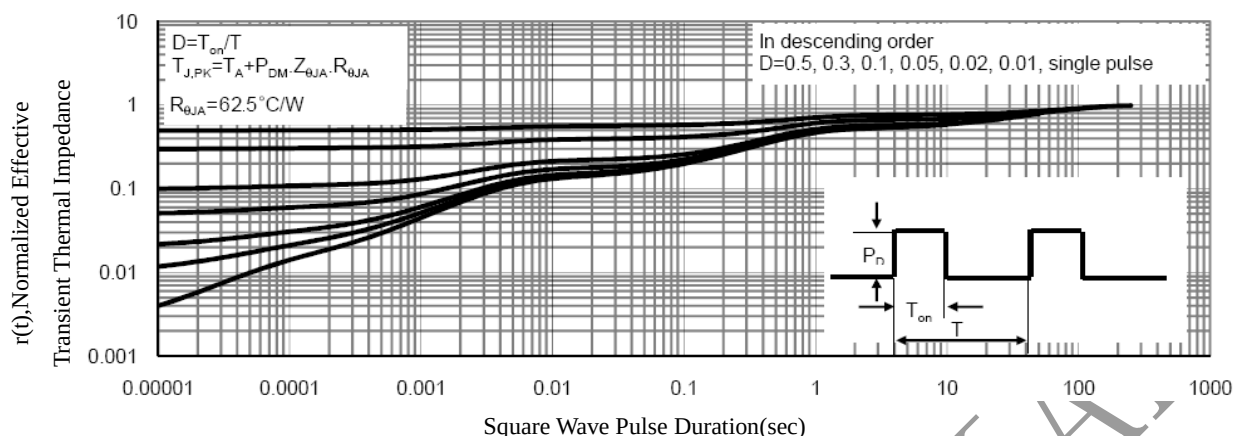


Figure 15. Normalized Maximum Transient Thermal Impedance

P-Channel Typical Electrical and Thermal Characteristics Curves

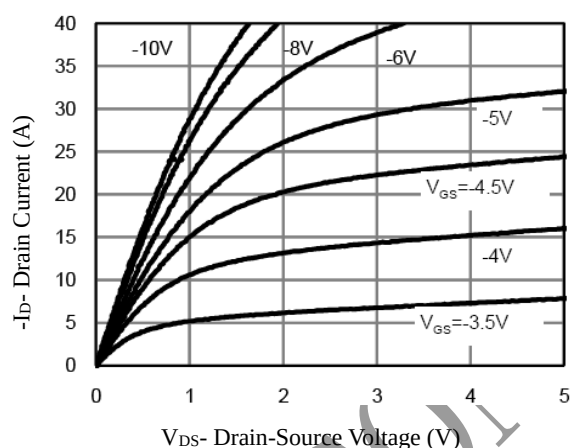


Figure 16. Output Characteristics

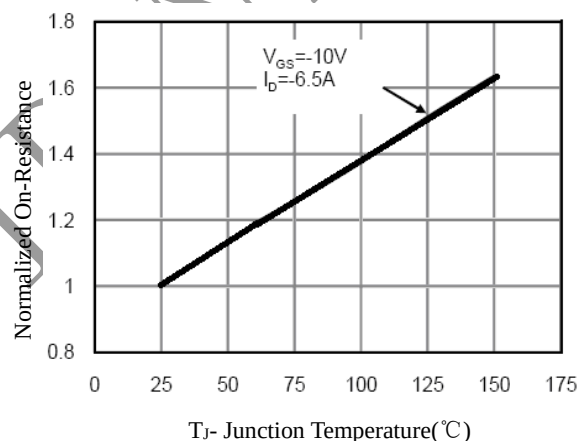


Figure 17. $R_{DS(ON)}$ -Junction Temperature

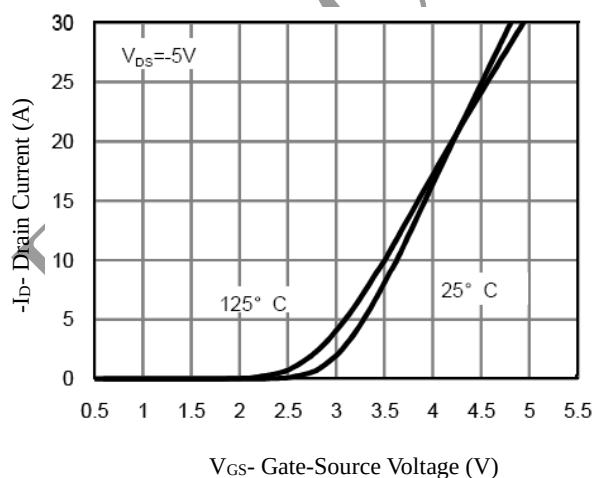


Figure 18. Transfer Characteristics

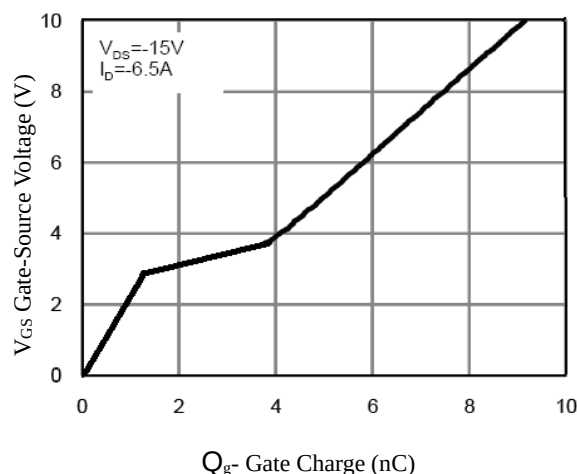


Figure 19. Gate Charge



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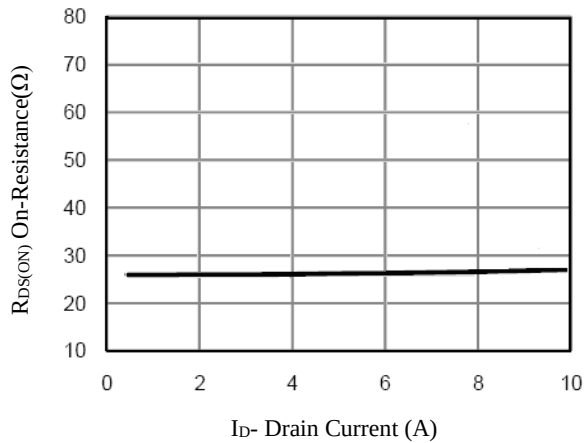


Figure 20. $R_{DS(ON)}$ - Drain Current

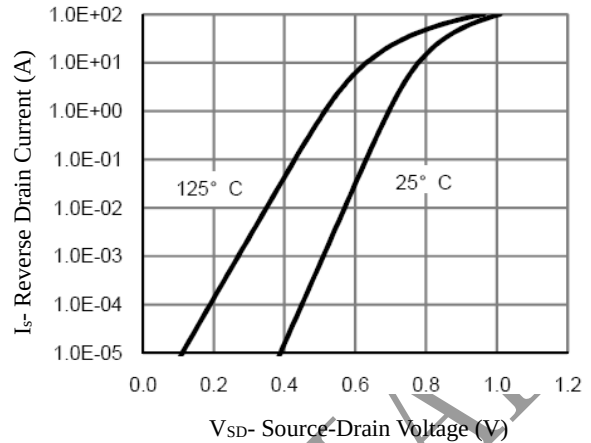


Figure 21. Source-Drain Diode Forward

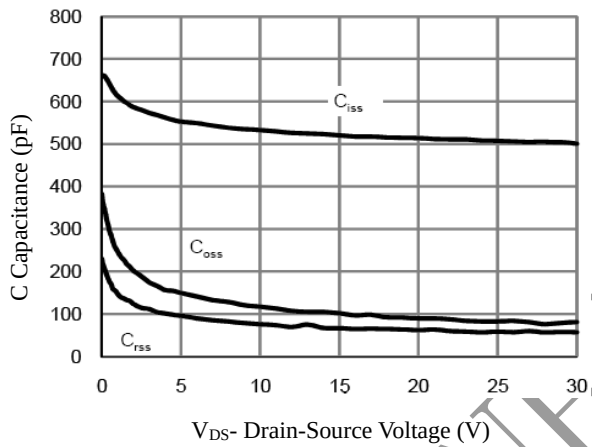


Figure 22. Capacitance vs V_{DS}

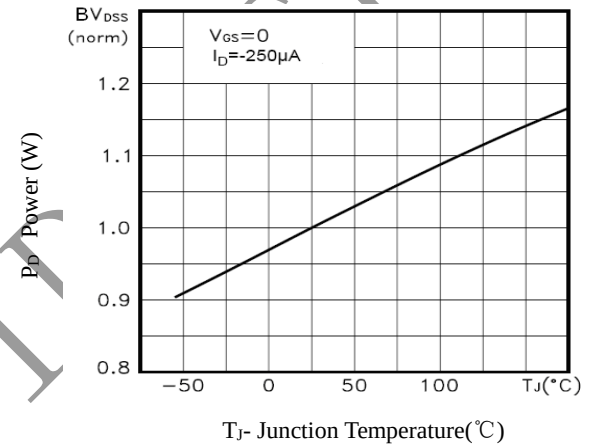


Figure 23. Power Dissipation

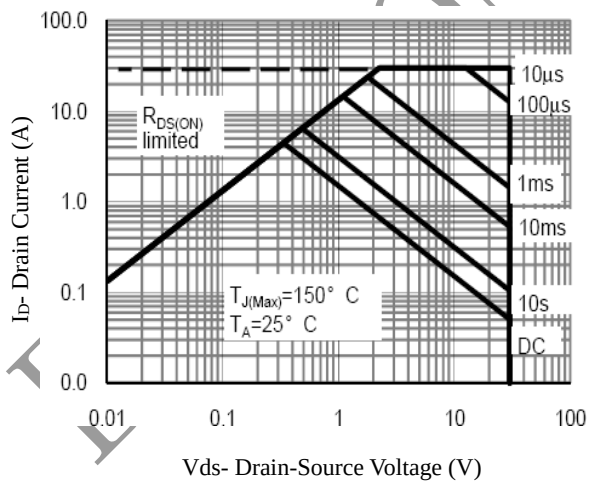


Figure 24. Safe Operation Area

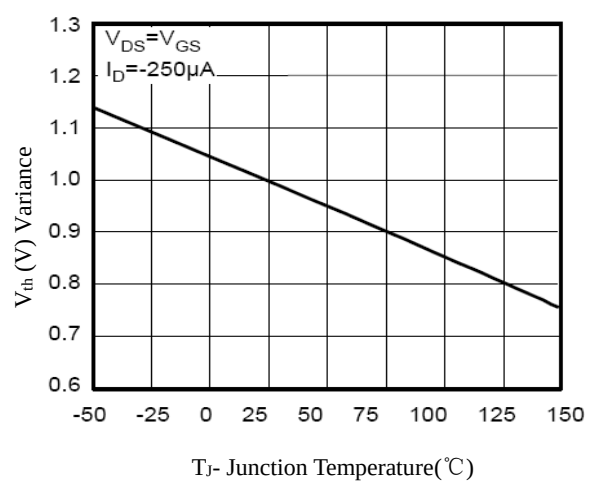


Figure 25. $V_{GS(th)}$ vs. Junction Temperature

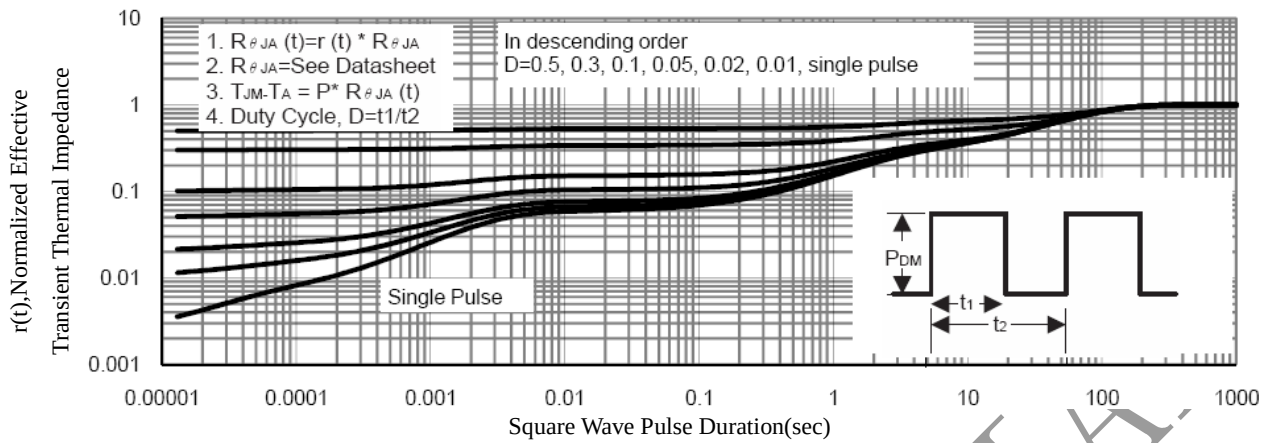
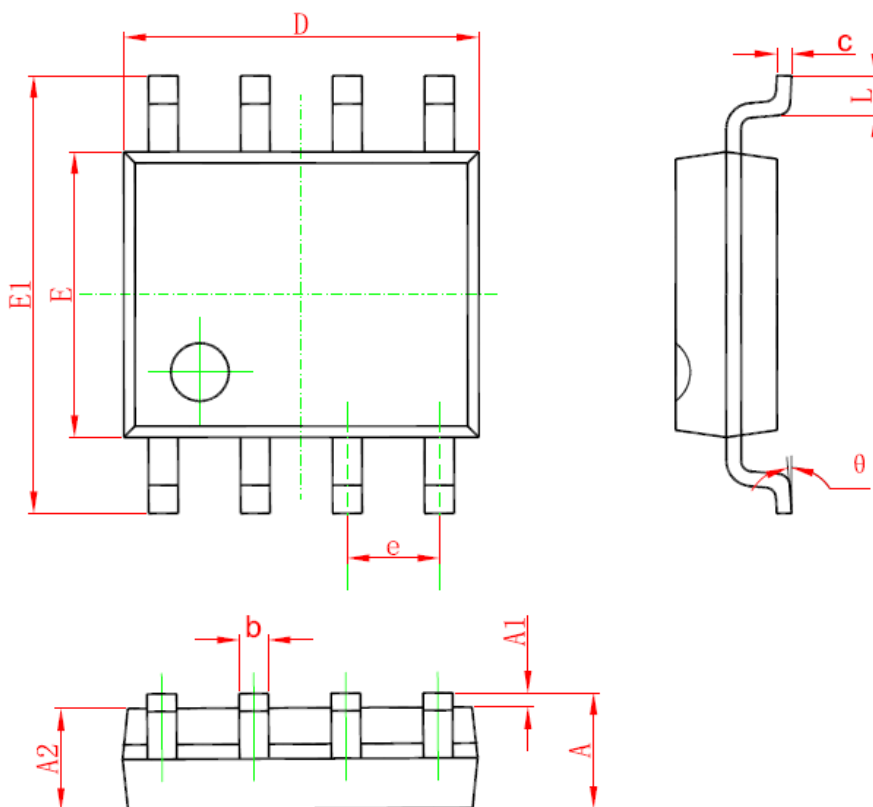


Figure 26. Normalized Maximum Transient Thermal Impedance

Physical Dimensions

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°