

AC/DC Convertor IC

PWM Type DC/DC converter IC Integrated Switching MOSFET

BM2PXXA/BM2PXXB Series

General Description

The PWM Type DC/DC converter for AC/DC provides an optimal system for all products that include an electrical outlet. BM2PXXA/BM2PXXB supports both isolated and non-isolated devices, enabling simpler design of various Types of high-efficiency electrical converters.

The built-in starter circuit which withstand 650V pressure contributes to low-power consumption. Design can be easily implemented because includes a sensing resistor. Current is restricted in each cycle and excellent performance is demonstrated in bandwidth and transient response since current mode control is utilized. The switching frequency is 100 kHz. At light load, the switching frequency is reduced and high efficiency is achieved. A frequency hopping function that contributes to low EMI is also included on chip. Design can be easily implemented because includes a 650V switching Super Junction MOSFET.

Key Features

- ■PWM frequency: 100kHz
- ■PWM current mode control
- ■Frequency hopping function
- ■Burst operation when load is light
- ■Frequency reduction function
- ■Built-in 650V starter circuit
- ■Built-in 650V switching MOSFET
- ■VCC pin Under-Voltage protection
- ■VCC pin Over-Voltage protection
- ■Per-cycle Over-Current Protection Circuit
- ■AC Correction function of Over current limiter
- ■Soft start
- ■Secondary Over-Current Protection Circuit
- ■External LATCH function
- ■X-Capacitor discharge function

Basic specifications

■Operating Power Supply Voltage Range

VCC
DRAIN
:to 650V
VH
:to 650V
■Normal Operating Current
■Burst Operating Current
■Oscillation Frequency
■Operating Temperature
■MOSFET ON Resistance
:10.9V to 26.0V
:to 650V
:1.40mA (Typ.)
:0.25mA (Typ.)
:-40°C to +105°C
:-40°C to +105°C
:2.0Ω (Typ.)

Package

DIP8 9.27mm×6.35mm×5.33mm pitch 2.54mm (Typ.) (Typ.) (Max.)



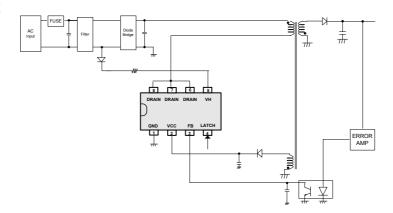
Line-up

	Current Limitter	VCCOVP	FBOLP	
BM2P01A	0.43A	Latch	Latch	
BM2P11A	0.43A	Latch	Auto Restart	
BM2P21A	0.43A	Auto Restart	Latch	
BM2P31A	0.43A	Auto Restart	Auto Restart	
BM2P01B	0.54A	Latch	Latch	
BM2P11B	0.54A	Latch	Auto Restart	
BM2P21B	0.54A	Auto Restart	Latch	
BM2P31B	0.54A	Auto Restart	Auto Restart	

Applications

For AC adapters and household appliances

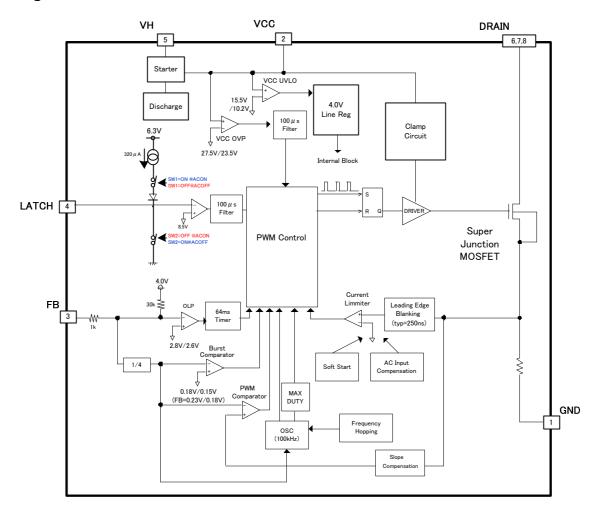
Application Circuit



Pin Descriptions

NO.	Pin Name	I/O	Function	ESD Diode	
NO.	Pin Name	1/0	Function	VCC	GND
1	GND	I/O	GND pin	~	-
2	VCC	I	Power Supply pin	-	'
3	FB	I	Feedback pin	✓	'
4	LATCH	I	External Latch	✓	'
5	VH	I	Start up pin	-	'
6	DRAIN	I/O	MOSFET DRAIN pin	-	-
7	DRAIN	I/O	MOSFET DRAIN pin	-	-
8	DRAIN	I/O	MOSFET DRAIN pin	-	-

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum applied voltage 1	V _{max1}	-0.3 to 650	V	VH
Maximum applied voltage 2	V_{max2}	-0.3 to 650	V	DRAIN
Maximum applied voltage 3	V_{max3}	-0.3 to 6.5	V	FB, LATCH
Maximum applied voltage 4	V_{max4}	-0.3 to 32.0	V	VCC
Drain current pulse	I _{DD}	10.4	Α	P _w =10µs, Duty cycle=1%
Power dissipation	P_D	1.06	W	
Ambient temperature range	T _{OPR}	-40 to +105	°C	
Maximum junction temperature	T_{JMAX}	+125	°C	
Storage temperature range	T _{STR}	-55 to +150	°C	

(Note) When mounted (on 114.5 mm \times 101.5 mm \times 1.6 mm thick, glass epoxy on single-layer substrate). De-rated by 8.52mW/°C when operating above T_a =25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating	Unit	Conditions
Power supply voltage range 1	V_{H}	to 650	٧	VH
Power supply voltage range 2	V_{DRAIN}	to 650	٧	DRAIN
Power supply voltage range 3	V _{CC}	10.9 to 26.0	V	vcc

Electrical Characteristics of MOSFET (unless otherwise noted, Ta = 25°C, VCC = 15V)

Electrical characteriotics of infect E1 (amose ethic wice hetea, 14 20 6, 100 101							
Devemeter	Current ed		Specifications			Conditions	
Parameter	Symbol Min.		Тур.	Max.	Unit	Conditions	
[MOSFET part]							
Between DRAIN and SORCE current	V _{(BR)DDS}	650	-	-	V	I _D =1mA / V _{GS} =0V	
DRAIN leak current	I _{DSS}	-	-	100	μA	V _{DS} =650V / V _{GS} =0V	
On resistance	R _{DS(ON)}	-	2.0	2.6	Ω	I _D =0.25A / V _{GS} =10V	

Electrical Characteristics of Control IC(unless otherwise noted. Ta = 25°C. VCC = 15 V)

Specifications Unit Conditions						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
[Circuit Current]						
- -						FB=2.0V(PULSE operation)
Circuit current (ON) 1	I _{ON1}	0.90	1.40	1.90	mA	DRAIN : OPEN
Circuit current (ON) 2	I _{ON2}	0.15	0.25	0.35	mA	FB=0.0V(Burst operation)
Circuit current (OFF)	I_{OFF}	10	20	30	μΑ	During Starting and VCC=14.5V
[VCC Protection Function]						
VCC UVLO voltage 1	V_{UVLO1}	14.50	15.50	16.50	V	VCC rises
VCC UVLO voltage 2	V _{UVLO2}	9.50	10.20	10.90	V	VCC falls
VCC UVLO hysteresis	V _{UVLO3}	-	5.30	-	V	Vuvlo3= Vuvlo1- Vuvlo2
VCC OVP voltage 1	V _{OVP1}	26.0	27.5	29.0	V	VCC rises
VCC OVF Voltage 1	V OVP1	20.0	21.5	29.0	V	In the case of
VCC OVP voltage 2	V _{OVP2}	-	23.5	-	V	Auto Restart Typed
VCC OVP hysteresis	V _{OVP3}	-	4.0	-	V	In the case of Auto Restart Typed
Latch released VCC voltage	V_{RESET}	-	V _{UVLO2} -0.5	-	V	, ·
VCC recharge start voltage	V _{CHG1}	9.70	10.70	11.70	V	
VCC recharge stop voltage	V _{CHG2}	14.00	15.00	16.00	V	
Latch mask time	T _{LATCH}	50	100	150	<u> </u>	
	1				μs °C	Control IC, temp rises
Thermal shut down temperature1	T _{SD1}	120	145	170	°C	
Thermal shut down temperature2	T _{SD2}	90	115	140	°C	Control IC, temp falls
[PWM Type DCDC Driver Block]						
Oscillation frequency 1	F _{SW1}	94	100	106	kHz	FB=2.00V
Oscillation frequency 2	F _{SW2}	20	25	30	kHz	FB=0.18V
Frequency hopping width	F _{DEL}		6.0		kHz	FB=2.00V
Hopping fluctuation frequency	F _{CH}	75	125	175	Hz	
Starting frequency reduction mode	V _{DLT}	1.060	1.160	1.260	V	
Maximum duty	D _{max}	68.0	75.0	82.0	%	
FB pin pull-up resistance	R _{FB}	23	30	37	kΩ	ED diese
FB burst voltage1	V _{BST1}	0.130	0.180	0.230	V	FB rises
FB burst voltage2	V _{BST2}	0.180	0.230	0.280	V	FB falls
FB OLP voltage 1a FB OLP voltage 1b	V _{FOLP1A}	2.500	2.800	3.100	V	FB rises
FB OLP Voltage 10 FB OLP LATCH ON TIMER	V _{FOLP1B}	- 40	2.600	- 00	1	FB falls
FB OLP LATCH ON TIMER FB OLP LATCH OFF TIMER	T _{FOLP1}	40 332	64 512	88 692	ms	
[Over Current Detection Block]	T_{FOLP2}	332	312	092	ms	
Over-current Limiter 1a	1	0.330	0.430	0.530	Α	Ton=0µs (BM2PXXA)
	I _{SOURCE1a}	0.330		0.550	+	. ` `
Over-current Limiter 2a	I _{SOURCE2a}	- 0.440	0.780	- 0.040	A	Ton=10µs (BM2PXXA)
Over-current Limiter 1b	I _{SOURCE1b}	0.440	0.540	0.640	A	Ton=0µs (BM2PXXB)
Over-current Limiter 2b	I _{SOURCE2b}		1.020	-	Α	Ton=10µs (BM2PXXB)
Leading edge blanking time	T_LEB	-	(250)	-	ns	
[External LATCH function]						
LATCH detect voltage	V_{LATCH}	7.80	8.50	9.20	V	
LATCH pull up current	I _{LATCH-up}	250	320	390	μΑ	AC=ON
LATCH pull down resistance	R _{LATCH-down}	100	250	400	Ω	AC=OFF, LATCH=3.0V
[VH Start Circuit Block]						-
Start current	I _{START}	1.90	5.50	10.20	mA	VH=100V/ VCC=10V
Start OFF current	I _{START_OF}	5	10	20	μΑ	VH=100V
Discharge ON voltage	VH _{DIS1}	90.2	101.5	112.8	V	
Discharge ON delay time	T _{DISON}	88	128	168	ms	
	· DISON		. = 0	. 50	0	

Block Description

(1) Start circuit / AC Voltage UVLO / Discharge function (VH: Pin 5)

This IC has a built-in start circuit. The IC also has the AC voltage UVLO (Under Voltage Lock Out) function which stops to operate the pulse operation when the AC voltage lowers at the VH pin, and the discharge function which discharges X-cap if the AC voltage outlet is pulling out.

The Application circuit and Block Diagram are shown in Figure 1 and Timing chart is shown in Figure 2.

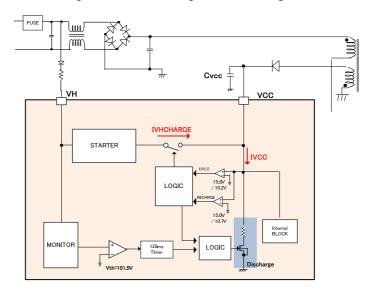


Figure 1. Application circuit and Block Diagram

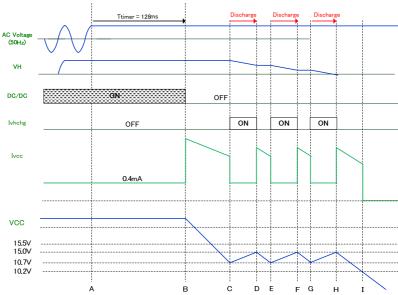


Figure 2. X-Capacitance Discharge / AC voltage UVLO Timing chart

- A: The AC voltage input is turned OFF.
- B: After T_{DISON} (Typ.=128ms), so DC/DC is turned OFF and VCC is higher than V_{CHG1}(Typ.=10.7V) that VCC capacitor is discharged.
- C: VCC becomes higher than V_{CHG1} (Typ.=10.7V), and the IC starts the recharge from VH pin to VCC pin. At this moment, VCC capacitor discharge is stopped.
- D: It stops charging to VCC pin when VCC becomes higher than V_{CHG2}(Typ.=15.0V). And it starts discharging of VCC capacitor.
- E: Same as C
- F: Same as D
- G: Same as C
- H: Same as D
- I: VCC< V_{UVLO2}(Typ.=10.2V)

(2) Start sequences

(Soft start operation, light load operation, and auto recovery operation by overload protection)

Start sequences are shown in Figure 3. See the sections below for detailed descriptions.

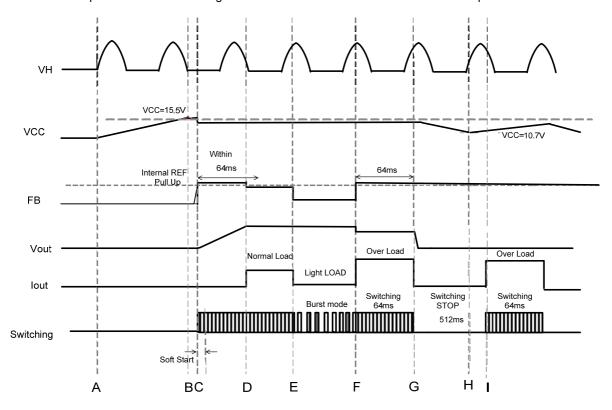


Figure 3. Start Sequences Timing Chart

- A: The input voltage VH is applied.
- B: This IC starts operating when the VCC pin voltage is higher than V_{UVLO1} (Typ.=15.5V). The Switching operation starts when the other protection functions are judged as normal. While the secondary output voltage becomes constant, the VCC pin current causes the VCC voltage to drop. As a result, the IC should be set the VCC voltage to be higher than V_{UVLO2} (Typ.=10.2V) until the IC starts to switch.
- C: With the soft start function, over current limit value is restricted to prevent any excessive rise in voltage or current.
- D: When the switching operation starts, Vout rises. After the output voltage starts, set the rated voltage within the T_{FOLP1} (Typ.=64ms) period.
- E: In case of a light load, the IC operates burst mode to reduce power consumption if the FB voltage lowers than V_{BST1} (Typ.=0.18V). During this time, it operates at low-power consumption mode.
- F: When the FB pin Voltage is higher than V_{FOLP1A} (Typ.=2.8V), it overloads.
- G: When the status that the FB voltage is higher than V_{FOLP1A} (Typ.=2.8V) continues for T_{FOLP1} (Typ.=64ms)^(NOTE1), the overload protection function is triggered and the switching stops during T_{FOLP2} (Typ.=512ms)^(NOTE2).
- H: If the VCC voltage drops to lower than $V_{\text{UVLO2}}\,$ (Typ.=10.7V), restart is executed.
- I: After T FOLP2 (Typ.=512ms), it repeats F,G and H if the condition keeps on overload.

(NOTE 1): IC internal timer is reset if the overload is released within 64ms.

(NOTE 2): IC internal timer is reset if the overload is released within 512ms.

(3) VCC pin protection function

The IC has a built-in VCC low voltage protection function VCCUVLO (Under Voltage Lock Out), an over voltage protection function VCCOVP (Over Voltage Protection), and a VCC recharge function that operates in case of a drop in VCC voltage.

The VCC charge function stabilizes the secondary output voltage charging from high voltage lines by the start circuit when the VCC voltage drops.

VCC UVLO / VCC OVP function

VCCUVLO is an auto recovery comparator with a voltage hysteresis. And VCCOVP is a latch Type or auto restart Type comparator. (The type of a latch or auto restart is different by products series.)

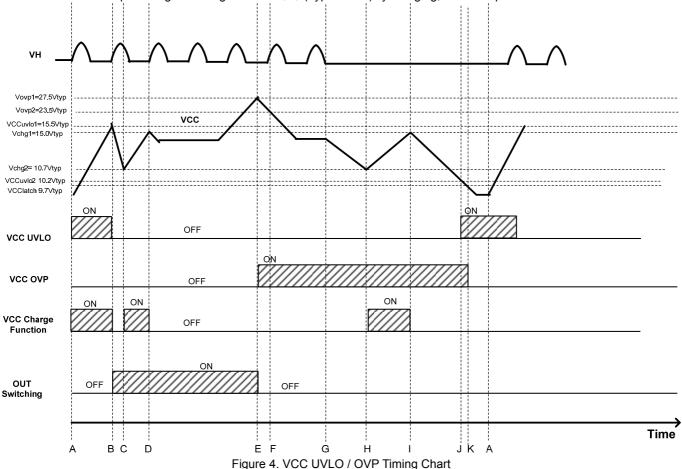
VCCOVP has a built-in mask time. This detects when the condition that VCC pin voltage is higher than V_{OVP1} (Typ.=27.5V) continues for T_{LATCH} (Typ.=100us). This function masks such as a surge generated at pin. Figure 4 is showed about the time chart of VCC OVP latch Type

VCC charge function

This IC has the recharge function.

VCC charge function operates when the VCC voltage drops lower than V_{CHG1} (Typ.=10.7V) after once VCC becomes higher than V_{UVLO1} (Typ.=15.5V) and the IC starts. At that time the VCC pin is charged from the VH pin through the start circuit. Through this operation, BM2PXXA/BM2PXXB prevents failure.

When the VCC pin voltage rises higher than V_{CHG2}(Typ.=15.0V) by charging, the IC stops it



- A: The VH voltage input, VCC pin voltage starts rising.
- B: When the VCC voltage is higher than V_{UVLO1}(Typ.=15.5V), VCC UVLO is released and DC/DC operation starts.
- C: When the VCC voltage is lower than V_{CHG1} (Typ.=10.7V), VCC charge function operates and the VCC voltage rises.
- D: When the VCC voltage is higher than V_{CHG2} (Typ.=15.0V), VCC charge function stops.
- E: When the condition that VCC voltage is higher than V_{OVP1} (Typ.=27.5V), continues for T_{LATCH} (Typ.=100us), the switching is stopped by the VCCOVP function.
- F: When the VCC voltage is lower than $V_{\text{OVP2}}(\text{Typ.=23.5V})$, DC/DC operation doesn't restarts because of latch function.
- G: The high voltage line VH is drops.
- H: Same as C
- I: Same as D
- J: When the VCC voltage is lower than V_{UVLO2} (Typ.=10.2V), VCC UVLO function operates.
- K: When the VCC voltage is lower than V_{RESET}(Typ.= V_{UVLO2}-0.5), LATCH function is released.

(4) DCDC driver (PWM comparator, frequency hopping, slope compensation, OSC, burst)

This IC has a current mode PWM control.

An internal oscillator sets a fixed switching frequency F_{SW1}(Typ.=100kHz)

It also has an integrated switching frequency hopping function, which causes the switching frequency to fluctuate. The fluctuation of cycle is F_{CH} (Typ.=125Hz).

Maximum duty cycle is fixed at D_{max} (Typ.=75%).

In current mode control, sub-harmonic oscillation may occur when the duty cycle exceeds 50%.

As a countermeasure, this IC has built-in slope compensation circuits.

This IC has built-in burst mode and frequency reduction circuits to achieve lower power consumption when the load is light.

FB pin is pulled up by R_{FB} (Typ.=30k Ω).

FB pin voltage is changed by secondary output voltage (secondary load power).

By monitoring the FB pin, burst mode operation and frequency detection start.

Figure 5 shows the FB voltage, and the DC/DC switching frequency operation.

- · mode1 : Burst operation
- mode2 : Frequency reduction operation (frequency is reduced)
- mode3: Fixed frequency operation (operates at max frequency)
- mode4 : Overload operation (stops the pulse operation and starts burst mode)

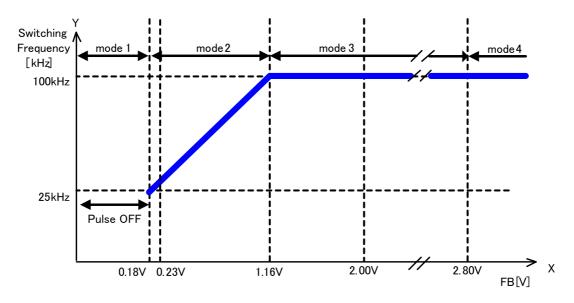
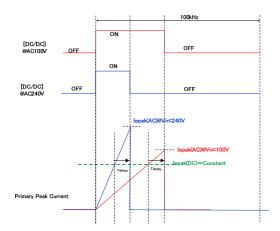


Figure 5. Switching Operation State Changes by FB Pin Voltage

(5) Over Current limiter

The IC has a built-in over current limiter per cycle. If the primary coil current exceeds a certain current, switching stops. It also has a built-in AC voltage compensation function. This is the correction function of AC voltage which increases the over current limiter level with time.

It is shown in figure 6, 7, and 8.



DC/DC]
@AC100V OFF
ON
OFF
ON
OFF
OFF
ON
Icpak/AC)@Vir=100V
Icpak/DC)=included conpensation

Figure 6. No AC Voltage Compensation Function

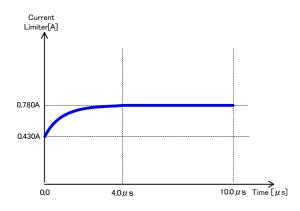
Figure 7. Built-in AC Compensation Voltage

Primary peak current is calculated using the formula below.

Primary peak current: $I_{peak} = I_{SOURCE} + V_{dc} / L_p \times T_{delay}$

 I_{SOURCE} : Over-current Limiter, V_{dc} : Input DC voltage, L_p : Primary inductance value,

T_{delay}: Delay time after detection of over current limiter



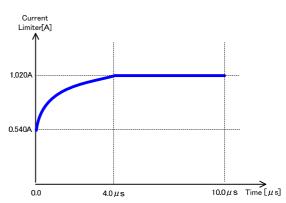
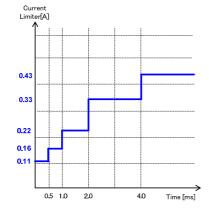


Figure 8a. Over Current Limiter (BM2PXXA)

Figure 8b. Over Current Limiter (BM2PXXB)

(6) Soft start operation

In order to prevent excessive voltage rise and current rise during startup, The IC limits the over current limiter value. The detail is shown in Figure 9. Over current limiter achieves the soft start operation by changing its value with time.



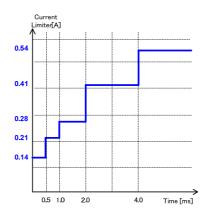


Figure 9a. Soft start (BM2PXXA/Ton=0µs)

Figure 9b. Soft start (BM2PXXB/Ton=0µs)

(7) Output over load protection function (FB OLP Comparator)

The output overload protection is the function which monitors the secondary output load status by FB pin and stops the switching at over status.

In case of overload, current no longer flows to the photo coupler because of the fall of output voltage, so FB voltage rises. If the status that FB voltage is higher than V_{FOLP1A} (Typ.=2.8V) continues for T_{FOLP1} (Typ.=64ms), IC stops the switching operation judging it is overload. If FB pin drops to lower than V_{FOLP1B} (Typ.=2.6V) from the status that FB pin is higher than V_{FOLP1A} (Typ.=2.8V) within T_{FOLP1} (Typ.=64ms), the timer of the overload protection is reset. The IC operate switching for T_{FOLP1} (Typ.=64ms). At starting, FB pin operates from more than V_{FOLP1A} (Typ.=2.8V) because it is pulled up at IC internal voltage. For that, it is necessary for the secondary output voltage to be set the startup time so that FB voltage becomes lower than V_{FOLP1B} (Typ.=2.6V) within T_{FOLP1} (Typ.=64ms).

The returning from once detecting FBOLP is after T_{FOLP2} (Typ.=512ms).

(8) External latch function (LATCH Pin)

LATCH pin has external LATCH function and LED indication.
Block Diagram and Timing chart is shown in Figure10 and Figure11.

<AC Voltage indication>

AC voltage is monitored by VH pin. AC ON : Hi (320 μ A current pull up) AC OFF : Low (250 ohm pull down)

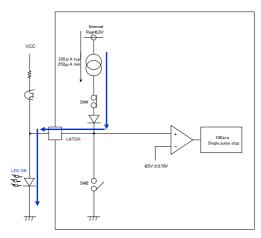


Figure 10a. AC=ON, LED connected

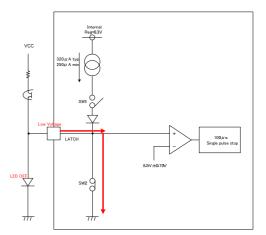


Figure 10b. AC=OFF, LED connected

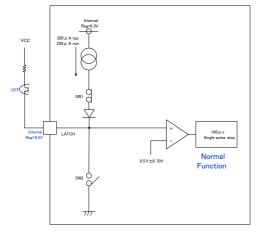


Figure 10c. LATCH=OFF, LED not connected

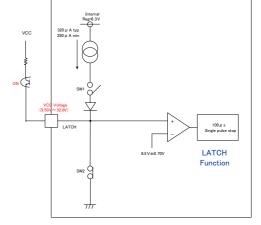


Figure 10d. LATCH=ON, LED not connected

<LATCH Function>

If the LATCH pin voltage becomes over 8.5V for more than 100µs, the IC latch-stops.

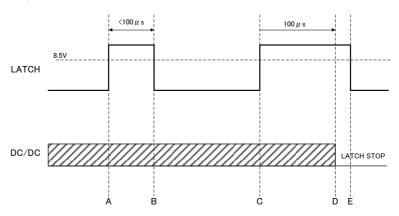


Figure 11. LATCH Function Timing chart

Operation mode of protection circuit
Operation mode of protection functions are shown in Table 1.

Table 1. Operation Mode of Protection Circuit

Function	Operation mode
VCC Under Voltage Locked Out	Auto recovery
VCC Over Voltage Protection	Auto recovery/Latch(with 100µs timer)
Thermal Shut Down	Auto recovery (with 100µs timer)
FB Over Limited Protection	Auto recovery/Latch (with 64ms timer)

Thermal loss

The thermal design should set the operation for the following conditions.

(Since the temperature shown below is the guaranteed temperature, be sure to take into account a sufficient margin.)

- 1. The ambient temperature Ta must be 105°C or less.
- 2. The IC's loss must be within the allowable dissipation P_d.

The thermal dissipation characteristics are as follows.

(PCB: 114.5 mm × 101.5mm × 1.6 mm, mounted on glass epoxy single-layer substrate)

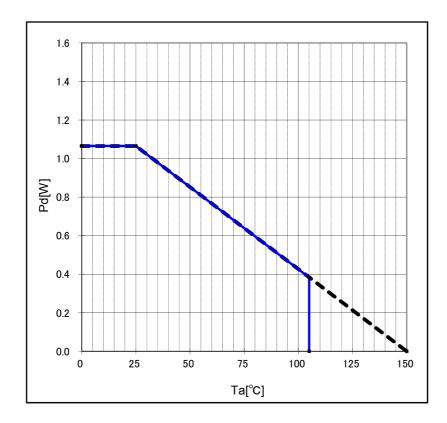
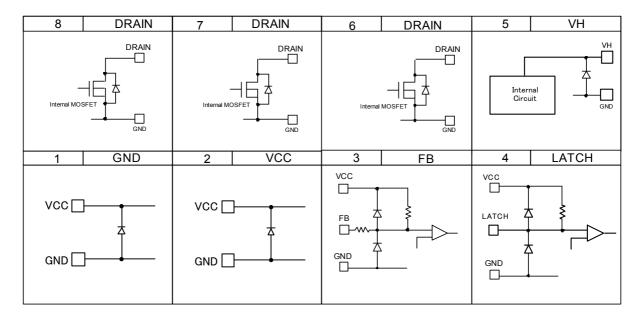
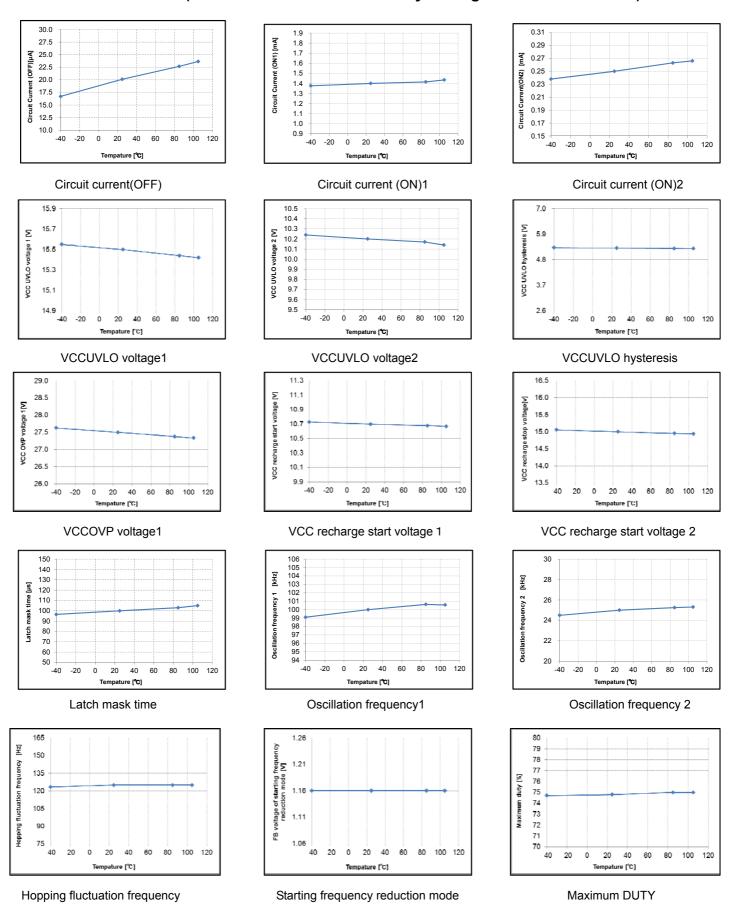


Figure 12. Thermal Dissipation Characteristics

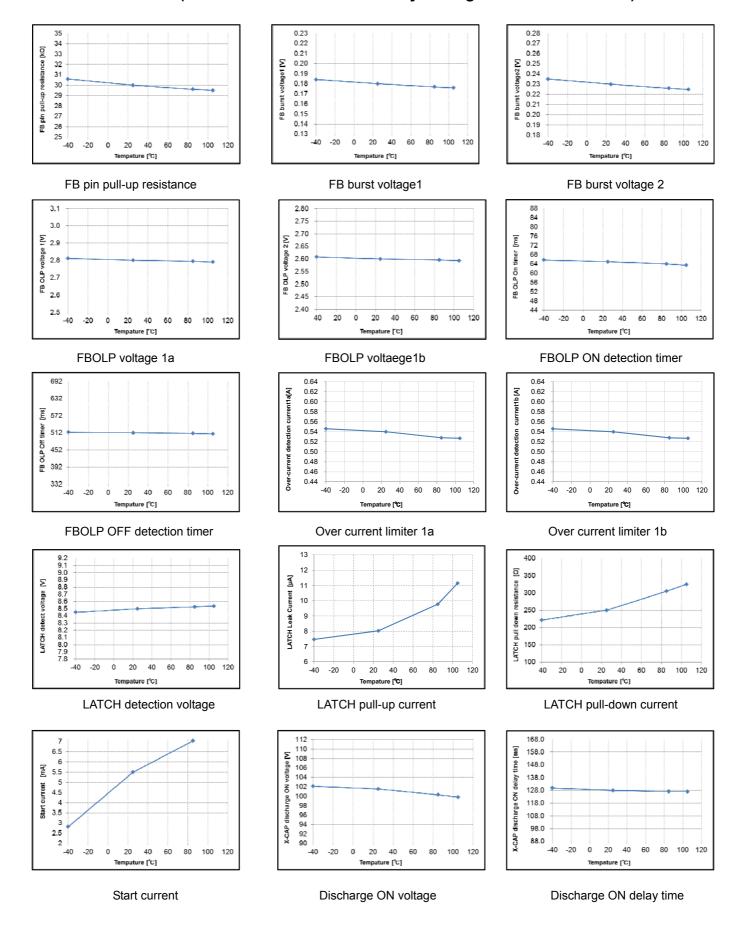
I/O Equivalent Circuit Diagram



Characteristic data (These are reference data. They can't guarantee their value.)



Characteristic data (These are reference data. They can't guarantee their value.)



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the GND and supply lines of the digital and analog blocks to prevent noise in the GND and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to GND at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. GND Voltage

Ensure that no pins are at a voltage below that of the GND pin at any time, even during transient condition.

4. GND Wiring Pattern

When using both small-signal and large-current GND traces, the two GND traces should be routed separately but connected to a single GND at the reference point of the application board to avoid fluctuations in the small-signal GND caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The GND lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, GND the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to GND, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or GND line.

Operational Notes - continued

12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

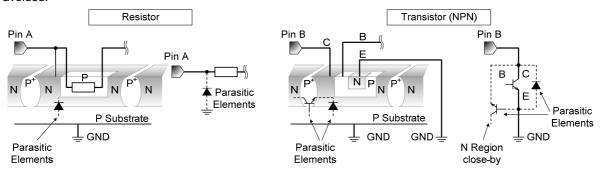


Figure 17. Example of Monolithic IC Structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

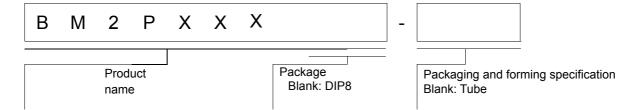
15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

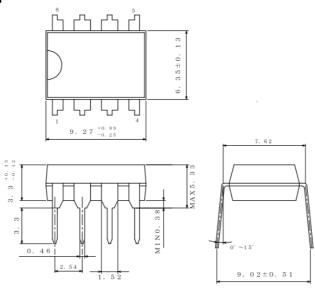
16. Over-Current Protection Circuit (OCP)

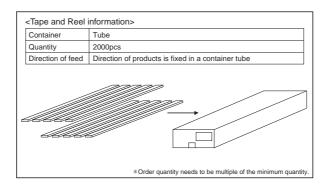
This IC has a built-in overcurrent protection circuit that activates when the output is accidentally shorted. However, it is strongly advised not to subject the IC to prolonged shorting of the output.

Ordering Information

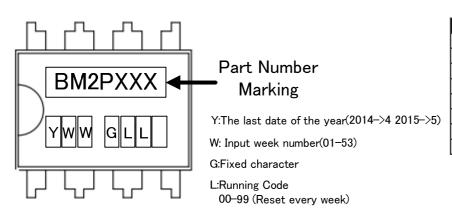


Physical Dimension Tape and Reel Information





Marking Diagram



Line - UP

Product name						
BM2P01A						
BM2P11A						
BM2P21A						
BM2P31A						
BM2P01B						
BM2P11B						
BM2P21B						
BM2P31B						

Revision History

Date	Revision	Changes
16.Nov.2015	001	New Release
22.Mar.2017	002	P1 a value of basic specifications P3 a value of operating conditions P8 a value of Figure5 P11 a value of external latch function

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JÁPAN	USA	EU	CHINA
CLASSⅢ	CL ACCIII	CLASS II b	CL ACCIII
CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ

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 - [h] Use of the Products in places subject to dew condensation
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- 8. Confirm that operation temperature is within the specified range described in the product specification.
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
 may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is
 exceeding the recommended storage time period.
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- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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