# BLM8G0710S-45AB; BLM8G0710S-45ABG

Rev. 3 — 15 October 2015

AMPLEON Product data sheet

#### **Product profile** 1.

# 1.1 General description

The BLM8G0710S-45AB(G) is a dual section, asymmetric, 2-stage power MMIC using Ampleon's state of the art GEN8 LDMOS technology. This multiband device is perfectly suited as small cell final stage in Doherty configuration, or as general purpose driver in the 700 MHz to 1000 MHz frequency range. Available in gull wing or straight lead outline.

#### Table 1. Performance

Typical RF performance at T<sub>case</sub> = 25 °C. Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF; specified in a class-AB production circuit.

Test signal	f	I <sub>Dq1</sub> [1]	I <sub>Dq2</sub> [1]	V <sub>DS</sub>	P <sub>L(AV)</sub>	Gp	η <sub>D</sub>	ACPR <sub>5M</sub>
	(MHz)	(mA)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA								
carrier section	957.5	30	120	28	3	34.7	26	-41.5
peaking section	957.5	60	240	28	6	34.7	26	-40

[1] I<sub>Da1</sub> represents driver stage; I<sub>Da2</sub> represents final stage.

## 1.2 Features and benefits

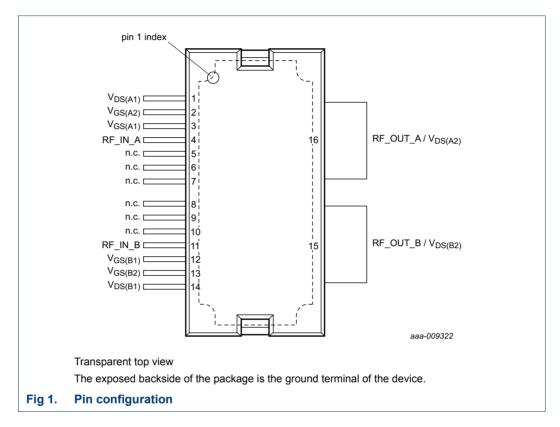
- Designed for broadband operation (frequency 700 MHz to 1000 MHz)
- High section-to-section isolation enabling multiple combinations
- High Doherty efficiency thanks to 2 : 1 asymmetry
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

## 1.3 Applications

- RF power MMIC for W-CDMA base stations in the 700 MHz to 1000 MHz frequency range. Possible circuit topologies are the following as also depicted in Section 8.1:
  - Asymmetric final stage in Doherty configuration
  - Asymmetric driver for high power Doherty amplifier

# 2. Pinning information

## 2.1 Pinning



## 2.2 Pin description

#### Table 2. **Pin description** Symbol Pin Description 1 drain-source voltage of carrier section, driver stage (A1) V<sub>DS(A1)</sub> 2 gate-source voltage of carrier section, final stage (A2) V<sub>GS(A2)</sub> 3 gate-source voltage of carrier section, driver stage (A1) V<sub>GS(A1)</sub> RF\_IN\_A 4 RF input carrier section (A) 5 not connected n.c. 6 n.c. not connected 7 n.c. not connected 8 not connected n.c. 9 n.c. not connected 10 not connected n.c. RF\_IN\_B 11 RF input peaking section (B) 12 gate-source voltage of peaking section, driver stage (B1) V<sub>GS(B1)</sub> gate-source voltage of peaking section, final stage (B2) V<sub>GS(B2)</sub> 13 14 drain-source voltage of peaking section, driver stage (B1) V<sub>DS(B1)</sub>

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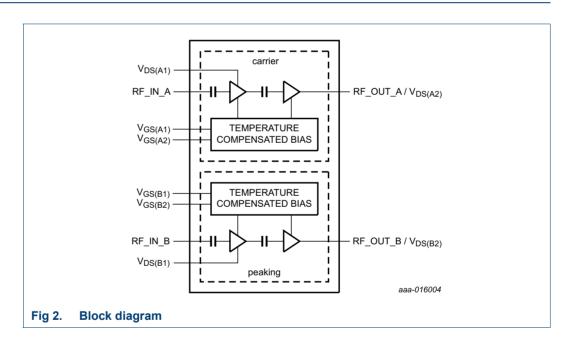
Table 2. Pin desci	ription	.continued
Symbol	Pin	Description
RF_OUT_B/V <sub>DS(B2)</sub>	15	RF output peaking section (B) / drain-source voltage of peaking section, final stage (B2)
RF_OUT_A/V <sub>DS(A2)</sub>	16	RF output carrier section (A) / drain-source voltage of carrier section, final stage (A2)
GND	flange	RF ground

# 3. Ordering information

#### Table 3.Ordering information

Type number	Package								
	Name	Description	Version						
BLM8G0710S-45AB	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-2						
BLM8G0710S-45ABG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-2						

# 4. Block diagram



# 5. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage		-	65	V
V <sub>GS</sub>	gate-source voltage		-0.5	+13	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	<u>[1]</u>	-	225	°C
T <sub>case</sub>	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

# 6. Thermal characteristics

## Table 5. Thermal characteristics

Symbol	Parameter Conditions						
Carrier s	ection						
R <sub>th(j-c)</sub>	thermal resistance from junction to case	final stage; T <sub>case</sub> = 90 °C; P <sub>L</sub> = 1.26 W	<u>[1]</u>	3	K/W		
		driver stage; T <sub>case</sub> = 90 °C; P <sub>L</sub> = 1.26 W	<u>[1]</u>	10.6	K/W		
Peaking	section						
R <sub>th(j-c)</sub>	thermal resistance from junction to case	final stage; T <sub>case</sub> = 90 °C; P <sub>L</sub> = 2.51 W	<u>[1]</u>	1.8	K/W		
		driver stage; T <sub>case</sub> = 90 °C; P <sub>L</sub> = 2.51 W	<u>[1]</u>	7.3	K/W		

[1] When operated with a CW signal.

# 7. Characteristics

#### Table 6. DC characteristics

 $T_{case}$  = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Ν	Min	Тур	Max	Unit
Carrier s	ection						
Final stag	ge						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 241.3 μA	6	65	-	-	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 28 V; I <sub>D</sub> = 120 mA	1	1.5	2	2.7	V
		V <sub>DS</sub> = 28 V; I <sub>D</sub> = 120 mA	[1] 1	1.7	2.65	3.6	V
$\Delta I_{Dq} / \Delta T$	quiescent drain current variation with temperature	$-40 ^\circ\text{C} \le T_{case} \le +85 ^\circ\text{C}$	-		±0.5	-	%
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-		-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = 5.65 V; V <sub>DS</sub> = 10 V	-		4.2	-	А
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 1.0 V; V <sub>DS</sub> = 0 V	-		-	140	nA
Driver sta	age						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 60.3 μA	6	65	-	-	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 28 V; I <sub>D</sub> = 30 mA	1	1.5	2.1	2.7	V
		V <sub>DS</sub> = 28 V; I <sub>D</sub> = 30 mA	[2] 1	1.7	2.65	3.6	V
$\Delta I_{Dq} / \Delta T$	quiescent drain current variation with temperature	$-40 ^\circ\text{C} \le T_{case} \le +85 ^\circ\text{C}$	-		±0.5	-	%
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-		-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = 5.65 V; V <sub>DS</sub> = 10 V	-		1.05	-	А
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 1.0 V; V <sub>DS</sub> = 0 V	-		-	140	nA
Peaking	section						
Final stag	ge						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$V_{GS}$ = 0 V; I <sub>D</sub> = 482.6 $\mu$ A	6	65	-	-	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 28 V; I <sub>D</sub> = 240 mA	1	1.5	2	2.7	V
		V <sub>DS</sub> = 28 V; I <sub>D</sub> = 240 mA	[1] 1	1.7	2.65	3.6	V
$\Delta I_{Dq} / \Delta T$	quiescent drain current variation with temperature	$-40 ^\circ\text{C} \le T_{case} \le +85 ^\circ\text{C}$	-		±1	-	%
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-		-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	V <sub>GS</sub> = 5.65 V; V <sub>DS</sub> = 10 V	-		8.3	-	А
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 1.0 V; V <sub>DS</sub> = 0 V	-		-	140	nA

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LDMOS 2-stage power MMIC

#### Table 6. DC characteristics ... continued

 $T_{case}$  = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
Driver sta	ge					
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 120.6 μA	65	-	-	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 28 V; I <sub>D</sub> = 60 mA	1.5	2	2.7	V
		V <sub>DS</sub> = 28 V; I <sub>D</sub> = 60 mA	<sup>2]</sup> 1.7	2.65	3.6	V
$\Delta I_{Dq} / \Delta T$	quiescent drain current variation with temperature	$-40~^{\circ}C \leq T_{case} \leq +85~^{\circ}C$	-	±1	-	%
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 28 V	-	-	1.4	μA
I <sub>DSX</sub>	drain cut-off current	$V_{GS}$ = 5.65 V; $V_{DS}$ = 10 V	-	2.1	-	А
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 1.0 V; V <sub>DS</sub> = 0 V	-	-	140	nA

[1] In production circuit with 1.3 k $\Omega$  gate feed resistor.

[2] In production circuit with 1.2 k $\Omega$  gate feed resistor.

#### Table 7. RF Characteristics

Typical RF performance at  $T_{case} = 25 \, ^{\circ}C$ ;  $V_{DS} = 28 \, V$ ;  $I_{Dq1} = 30 \, mA$  (carrier section, driver stage);  $I_{Dq2} = 120 \, mA$  (carrier section, final stage);  $P_{L(AV)} = 3 \, W$  (carrier section);  $I_{Dq1} = 60 \, mA$  (peaking section, driver stage);  $I_{Dq2} = 240 \, mA$  (peaking section, final stage);  $P_{L(AV)} = 6 \, W$  (peaking section) unless otherwise specified, measured in an Ampleon straight lead production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Carrier se	ection					
Test signa	II: single carrier W-CDMA [1]					
G <sub>p</sub>	power gain	f = 730.5 MHz	-	35.3	-	dB
		f = 957.5 MHz	33.2	34.7	36.2	dB
η <sub>D</sub>	drain efficiency	f = 730.5 MHz	-	23.4	-	%
		f = 957.5 MHz	21	26	-	%
RL <sub>in</sub>	input return loss	f = 957.5 MHz	-	-19	-10	dB
ACPR <sub>5M</sub>	adjacent channel power ratio (5 MHz)	f = 730.5 MHz	-	-38.5	-	dBc
		f = 957.5 MHz	-	-41.5	-36.5	dBc
PARO	output peak-to-average ratio	f = 730.5 MHz	-	8.1	-	dB
		f = 957.5 MHz	7.1	8.4	-	dB
Peaking s	section		I			
Test signa	II: single carrier W-CDMA [1]					
Gp	power gain	f = 730.5 MHz	-	35.6	-	dB
		f = 957.5 MHz	33.2	34.7	36.2	dB
η <sub>D</sub>	drain efficiency	f = 730.5 MHz	-	23.4	-	%
		f = 957.5 MHz	21	26	-	%
RL <sub>in</sub>	input return loss	f = 957.5 MHz	-	-17	-10	dB
ACPR <sub>5M</sub>	adjacent channel power ratio (5 MHz)	f = 730.5 MHz	-	-39.5	-	dBc
		f = 957.5 MHz	-	-40	-34.5	dBc
PARO	output peak-to-average ratio	f = 730.5 MHz	-	8	-	dB
		f = 957.5 MHz	6.7	8	-	dB

#### Table 7. RF Characteristics ...continued

Typical RF performance at  $T_{case} = 25 \, ^{\circ}C$ ;  $V_{DS} = 28 \, ^{\circ}V$ ;  $I_{Dq1} = 30 \, ^{\circ}MA$  (carrier section, driver stage);  $I_{Dq2} = 120 \, ^{\circ}MA$  (carrier section, final stage);  $P_{L(AV)} = 3 \, W$  (carrier section);  $I_{Dq1} = 60 \, ^{\circ}MA$  (peaking section, driver stage);  $I_{Dq2} = 240 \, ^{\circ}MA$  (peaking section, final stage);  $P_{L(AV)} = 6 \, W$  (peaking section) unless otherwise specified, measured in an Ampleon straight lead production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit				
Test signal: CW [2]										
$\Delta \phi_{s21}$	phase response difference	normalized; between sections	-10	-	+10	deg				
$\Delta  \mathbf{s}_{21} ^2$	insertion power gain difference	normalized; between sections	-0.5	-	+0.5	dB				

[1] 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF.

[2] f = 957.5 MHz.

# 8. Application information

#### Table 8. Doherty typical performance

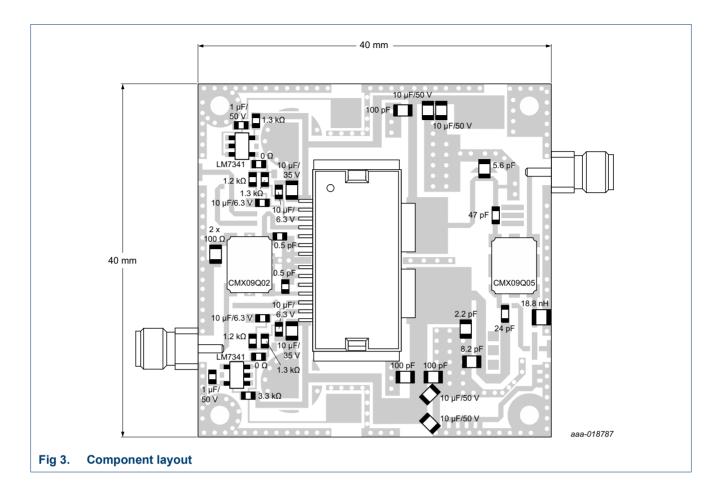
Test signal: 1-tone CW; RF performance at  $T_{case} = 25 \, ^{\circ}$ C;  $V_{DS} = 28 \, V$ ;  $I_{Dq1} = 130 \, mA$  (carrier section, final stage);  $I_{Dq2} = 4 \, mA$  (peaking section, final stage); unless otherwise specified, measured in an Ampleon,  $f = 925 \, MHz$  to 960 MHz, Doherty application circuit (see Figure 3 and Figure 4).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
P <sub>L(3dB)</sub>	output power at 3 dB gain compression	f = 942.5 MHz; 1-tone pulsed CW (10 % duty cycle)	-	63.9	-	W
η <sub>D</sub>	drain efficiency	at 9 dB OBO (P <sub>L</sub> = 8.3 W); f = 942.5 MHz; 1-tone pulsed CW (10 % duty cycle)	-	44.7	-	%
G <sub>p</sub>	power gain	P <sub>L(AV)</sub> = 8.3 W; f = 942.5 MHz	-	28.5	-	dB
B <sub>video</sub>	video bandwidth	P <sub>L(AV)</sub> = 4 W; f = 942.5 MHz; 2-tone CW	-	150	-	MHz
G <sub>flat</sub>	gain flatness	P <sub>L(AV)</sub> = 8.3 W	-	0.7	-	dB
К	Rollett stability factor	$T_{case} = -40 \text{ °C; } f = 0.1 \text{ GHz to 3 GHz}$ [1]	-	>1	-	

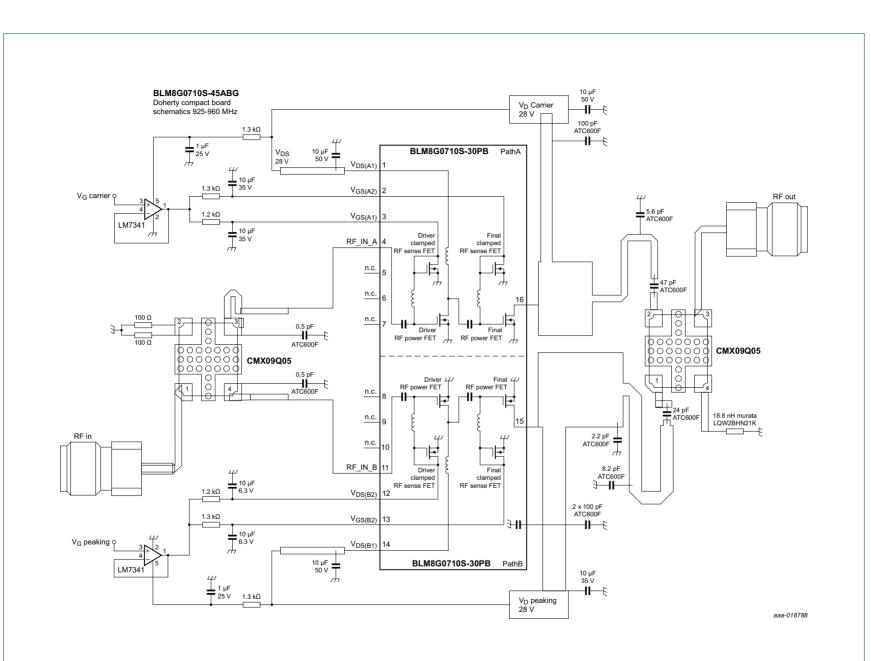
[1] For carrier and peaking sections (S-parameters measured with load-pull jig).

# BLM8G0710S-45AB(G)

LDMOS 2-stage power MMIC







LDMOS 2-stage power MMIC

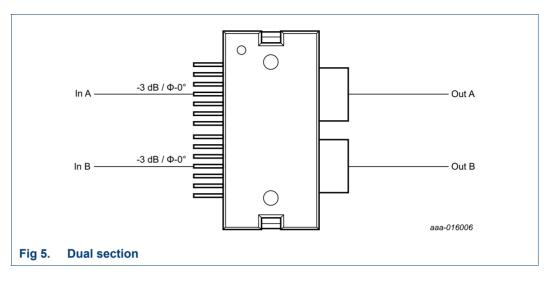
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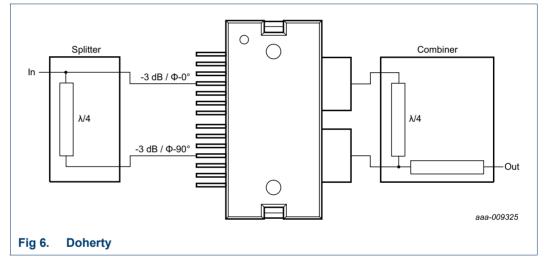
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Fig 4. Electrical schematic

LDMOS 2-stage power MMIC

# 8.1 Possible circuit topologies





## 8.2 Ruggedness in class-AB operation

The BLM8G0710S-45AB and BLM8G0710S-45ABG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: f = 840 MHz;  $V_{DS}$  = 32 V;  $I_{Dq1}$  = 40 mA (carrier section, driver stage);  $I_{Dq2}$  = 120 mA (carrier section, final stage);  $I_{Dq1}$  = 60 mA (peaking section, driver stage);  $I_{Dq2}$  = 240 mA (peaking section, final stage);  $P_i$  = 13 dBm (carrier section);  $P_i$  = 14 dBm (peaking section).  $P_i$  is measured at CW and corresponding to  $P_{L(3dB)}$  under  $Z_S$  = 50  $\Omega$  load.

## 8.3 Impedance information

#### Table 9. Typical impedance

Measured load-pull data at 3 dB gain compression point; test signal: pulsed CW;  $T_{case} = 25 \,$ °C;  $V_{DS} = 28 \,$ V;  $t_p = 100 \, \mu$ s;  $\delta = 10 \,$ %;  $Z_S = 50 \, \Omega$ ;  $I_{Dq1} = 30 \,$ mA (carrier section, driver stage);  $I_{Dq2} = 120 \,$ mA (carrier section, final stage);  $I_{Dq1} = 60 \,$ mA (peaking section, driver stage);  $I_{Dq2} = 240 \,$ mA (peaking section, final stage). Typical values unless otherwise specified.

	tuned for m	naximum o	utput p	ower		tuned for maximum power added efficiency					
f	ZL	G <sub>p(max)</sub>	PL	η <sub>add</sub>	AM-PM conversion	ZL	G <sub>p(max)</sub>	PL	η <sub>add</sub>	AM-PM conversion	
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)	
Carrier	section		1					1			
BLM8G	0710S-45AB										
700	6.2 + j3.6	33.9	44.8	56.4	-8.5	9.2 + j8.5	35.5	43.5	67.3	-10.7	
720	6.2 + j3.7	34	44.8	56.8	-8	8.8 + j9.6	35.7	43	67	-11	
740	6.3 + j3.6	33.9	44.8	57.2	-7.2	8.5 + j8.7	35.4	43.3	66.7	-9.7	
760	6.3 + j3.5	33.8	44.8	57.4	-6.1	9.4 + j8.4	35.3	43.3	66.7	-7.3	
780	6.2 + j3.5	33.6	44.8	57.7	-6.2	8.4 + j8.5	35.1	43.2	66.1	-8.2	
800	6.2 + j2.8	33.4	44.9	56.3	-5	9.2 + j8.5	35.1	43.2	65.4	-6.1	
820	6.3 + j2.9	33.3	44.8	56.8	-5.7	8.7 + j6.8	34.6	43.7	65.1	-6.3	
840	6.8 + j2.2	33.1	44.9	56.5	-4.1	7.9 + j6.9	34.6	43.7	65.1	-6.2	
860	7.4 + j1.7	33.1	44.8	56.2	-4	7.9 + j6.8	34.5	43.7	64.5	-6.2	
880	7.4 + j1.7	33.1	44.8	56.2	-3.3	7.8 + j6.8	34.5	43.6	64	-5.3	
900	7.2 + j0.9	32.9	44.8	54.3	-3.4	7.8 + j6.8	34.6	43.5	63.8	-5.2	
920	7.3 + j0.9	32.9	44.7	54.2	-2.7	8.1 + j7.8	34.8	43.1	63.1	-3.9	
940	8.1 + j0.7	33.2	44.7	55.2	-2	8.3 + j5.9	34.6	43.7	62.4	-2.8	
960	7.2 + j0.9	33.2	44.6	53.4	-2.4	8.7 + j6.7	34.8	43.3	61.8	-1.9	
980	8.0 + j0.8	33.4	44.7	55.1	-2	8.6 + j6.8	34.8	43.3	62.1	-1.5	
BLM8G	0710S-45ABG	i			l.					l	
700	6.4 + j3.1	34.4	44.4	55.3	-8.8	8.5 + j8.5	36.1	42.9	65.8	-12.7	
720	6.3 + j3.4	34.6	44.4	56.6	-8.3	8.9 + j8.8	36.1	42.8	66.8	-11	
740	6.5 + j2.6	34.4	44.5	55.5	-7.6	8.3 + j8.2	36	42.9	65.4	-10.9	
760	7.4 + j1.8	34.2	44.5	55.9	-6	8.8 + j8.7	35.9	42.6	65.1	-9.2	
780	6.5 + j1.6	33.6	44.5	53.1	-5.5	7.3 + j8.1	35.5	42.7	64.2	-10.2	
800	7.1 + j1.3	33.6	44.7	55.7	-4.8	7.1 + j8.0	35.5	42.8	64.9	-9.7	
820	6.4 + j1.2	33.3	44.7	54.2	-4.8	8.3 + j8.2	35.3	42.6	64	-6.9	
840	7.0 + j0.8	33.3	44.7	55	-4.7	8.1 + j8.1	35.3	42.5	63.5	-7	
860	7.5 + j0.5	33.3	44.6	54.7	-4.4	8.4 + j7.1	35.1	42.9	63.4	-6	
880	7.4 + j0.7	33.4	44.5	54.6	-4.3	8.2 + j7.4	35.3	42.7	62.3	-6	
900	8.2 + j0.3	33.6	44.4	54.8	-2.9	8.0 + j7.2	35.4	42.6	62.1	-4.9	
920	7.4 + j0.1	33.4	44.5	53.8	-2.8	7.3 + j6.3	35.3	42.9	61.8	-5.4	
940	8.0 + j0.1	33.5	44.4	53.9	-2.4	6.8 + j6.5	35.4	42.6	60.9	-5.7	
960	7.9 – j0.6	33.5	44.3	52.4	-2	7.0 + j6.9	35.8	42.4	60.5	-4.2	
980	7.7 – j0.5	33.7	44.4	53	-1.6	7.1 + j6.3	35.5	42.6	61.3	-3	

#### Table 9. Typical impedance ...continued

Measured load-pull data at 3 dB gain compression point; test signal: pulsed CW;  $T_{case} = 25 \,$ °C;  $V_{DS} = 28 \,$ V;  $t_p = 100 \, \mu$ s;  $\delta = 10 \,$ %;  $Z_S = 50 \, \Omega$ ;  $I_{Dq1} = 30 \,$ mA (carrier section, driver stage);  $I_{Dq2} = 120 \,$ mA (carrier section, final stage);  $I_{Dq1} = 60 \,$ mA (peaking section, driver stage);  $I_{Dq2} = 240 \,$ mA (peaking section, final stage). Typical values unless otherwise specified.

	tuned for m	aximum o	utput p	ower		tuned for maximum power added efficiency					
f	ZL	G <sub>p(max)</sub>	PL	η <sub>add</sub>	AM-PM conversion	ZL	G <sub>p(max)</sub>	PL	η <sub>add</sub>	AM-PM conversion	
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)	
Peaking	g section	I									
BLM8G	0710S-45AB										
700	3.0 + j2.1	36.1	47.2	55.1	2.4	4.2 + j5.2	37.6	45.3	65.7	-1.5	
720	3.0 + j1.7	35.9	47.3	53.4	2.5	4.4 + j5.0	37.8	45.4	64.6	-1	
740	3.0 + j1.7	35.8	47.4	54.8	3	4.2 + j4.5	37.5	45.7	64.7	-0.2	
760	3.0 + j1.3	35.4	47.4	53.5	3	4.1 + j4.8	37.2	45.4	64.3	-0.9	
780	3.3 + j1.3	35.3	47.5	55	2.4	4.0 + j4.4	37	45.7	63.7	-1.3	
800	3.2 + j0.9	35.2	47.5	53.8	3.1	3.9 + j4.2	37	45.8	64	-1	
820	3.3 + j1.0	35	47.5	54.9	2.4	4.1 + j3.8	36.7	46	63.6	-0.1	
840	3.4 + j0.5	34.8	47.5	53.2	2.3	3.8 + j4.0	36.8	45.7	63.4	-1.3	
860	3.5 + j0.5	34.7	47.5	53.8	2.1	3.8 + j3.8	36.7	45.7	63.1	-1.2	
880	3.4 + j0.4	34.8	47.4	53.2	1.8	4.0 + j3.5	36.7	45.9	63.1	-0.3	
900	3.4 + j0.3	34.7	47.4	53.4	2.1	3.7 + j3.6	36.8	45.7	63	-0.9	
920	3.4 + j0.4	34.7	47.4	54.4	1.4	3.8 + j3.7	36.8	45.5	63	-0.5	
940	3.5 + j0.0	34.5	47.3	52.9	1.1	3.5 + j3.2	36.6	45.7	62.3	-0.5	
960	3.5 – j0.1	34.2	47.3	52.7	1.3	3.5 + j3.1	36.4	45.7	62	-0.3	
980	3.5 – j0.1	34.2	47.3	53.9	0.4	3.4 + j2.8	36.2	45.8	62.2	-1	
BLM8G	0710S-45ABG	<b>I</b>	1				<b>I</b>	1	1	I	
700	3.0 + j0.6	36.3	47.5	55.1	0.3	4.5 + j3.6	37.7	45.8	66.1	-3.2	
720	3.0 + j0.6	36.4	47.5	55.6	0.6	4.4 + j3.1	37.7	46.1	65.7	-2.2	
740	2.9 + j0.3	35.9	47.6	54.6	1.9	4.1 + j3.4	37.3	45.8	65.4	-2	
760	3.0 + j0.2	35.6	47.7	56	0.6	4.4 + j2.8	37	46.1	65.1	-2.2	
780	3.3 – j0.1	35.5	47.7	55.9	0.9	4.3 + j2.9	37	46	64.7	-2.9	
800	3.3 – j0.5	35.4	47.7	54.4	0.8	3.9 + j2.6	37	46.1	64.4	-3.2	
820	3.3 – j0.5	35.8	47.7	55.2	1.3	4.1 + j2.3	37.3	46.2	64	-1.8	
840	3.3 – j0.5	35.5	47.6	55.4	1.3	4.1 + j2.1	36.6	46.3	63.7	-1.3	
860	3.5 – j0.9	34.5	47.7	54.9	0.6	3.8 + j2.0	35.9	46.3	63.7	-2.5	
880	3.4 – j1.0	34.7	47.6	54.2	-0.1	3.6 + j2.0	36.4	46.1	63.1	-3.2	
900	3.4 – j1.2	34.8	47.6	54.2	0	3.7 + j1.8	36.5	46.1	63.3	-2.7	
920	3.4 – j1.1	35	47.6	55.4	-0.4	3.7 + j1.8	36.6	45.9	63.2	-1.9	
940	3.5 – j1.4	34.7	47.5	54.7	-0.3	3.8 + j1.6	36.4	46	62.8	-1.2	
960	3.5 – j1.6	34.4	47.5	54.9	-0.4	3.5 + j1.3	36.1	46	62.8	-2.2	
980	3.2 – j1.6	33.9	47.5	54.6	-2.1	3.5 + j1.0	35.7	46.2	63.1	-2.5	

# BLM8G0710S-45AB(G)

LDMOS 2-stage power MMIC

RL<sub>in</sub>

(dB)

-10

-20

-30

-40

980

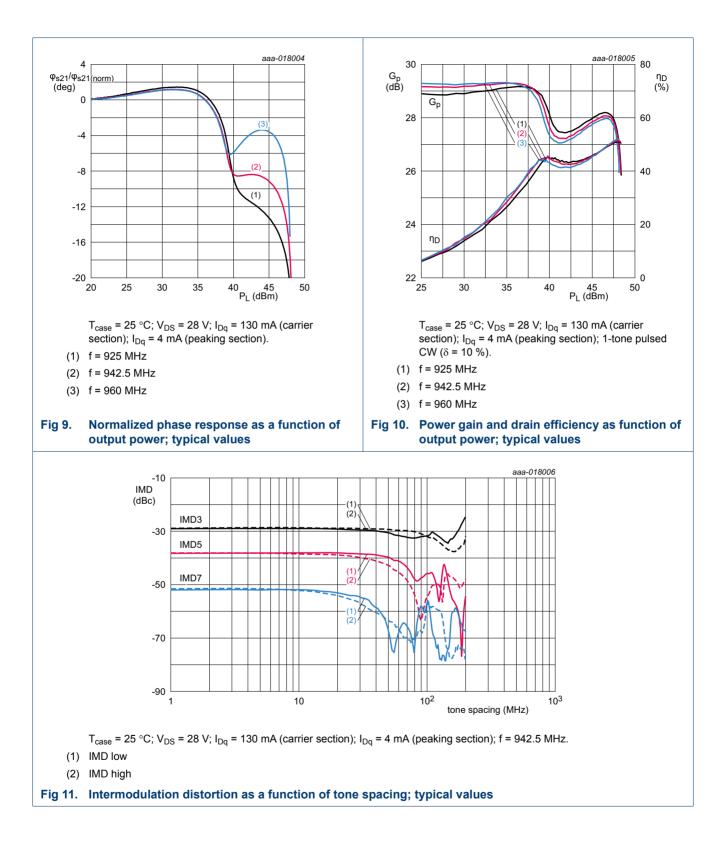
970

aaa-018002 0 aaa-018003 0 30 30 RL<sub>in</sub> G<sub>p</sub> (dB) G<sub>p</sub> (dB) G (dB) G 28 -10 28 RL **RL**in -20 26 26 24 -30 24 22 -40 22 960 97 f (MHz) 700 800 900 1000 1100 f (MHz) 1200 900 910 920 930 940 950  $T_{case}$  = 25 °C;  $V_{DS}$  = 28 V;  $I_{Dq}$  = 130 mA (carrier  $T_{case}$  = 25 °C;  $V_{DS}$  = 28 V;  $I_{Dq}$  = 130 mA (carrier section);  $I_{Dq}$  = 4 mA (peaking section);  $P_L$  = 1.25 W. section);  $I_{Dq}$  = 4 mA (peaking section);  $P_L$  = 1.25 W. (1) magnitude of G<sub>p</sub> (1) magnitude of G<sub>p</sub> (2) magnitude of RLin (2) magnitude of RLin Wideband power gain and input return loss as In-band power gain and input return loss as Fig 8. Fig 7. function of frequency; typical values function of frequency; typical values

8.4 Graphs

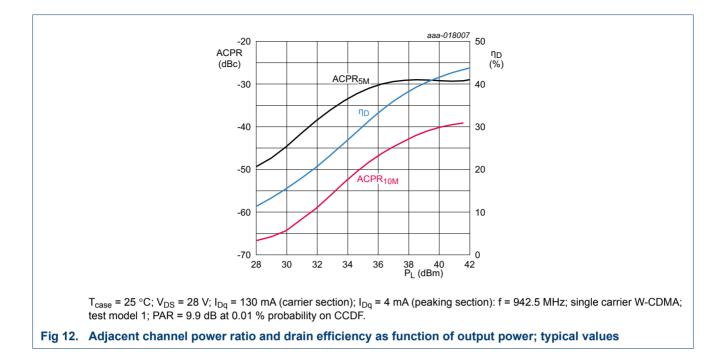
# BLM8G0710S-45AB(G)

LDMOS 2-stage power MMIC



# BLM8G0710S-45AB(G)

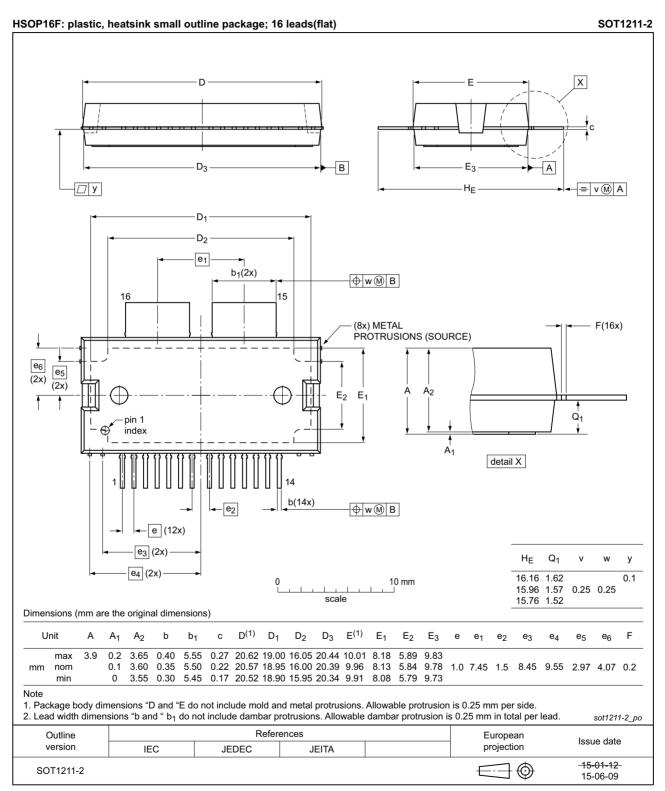
#### LDMOS 2-stage power MMIC



BLM8G0710S-45AB\_S-45ABG

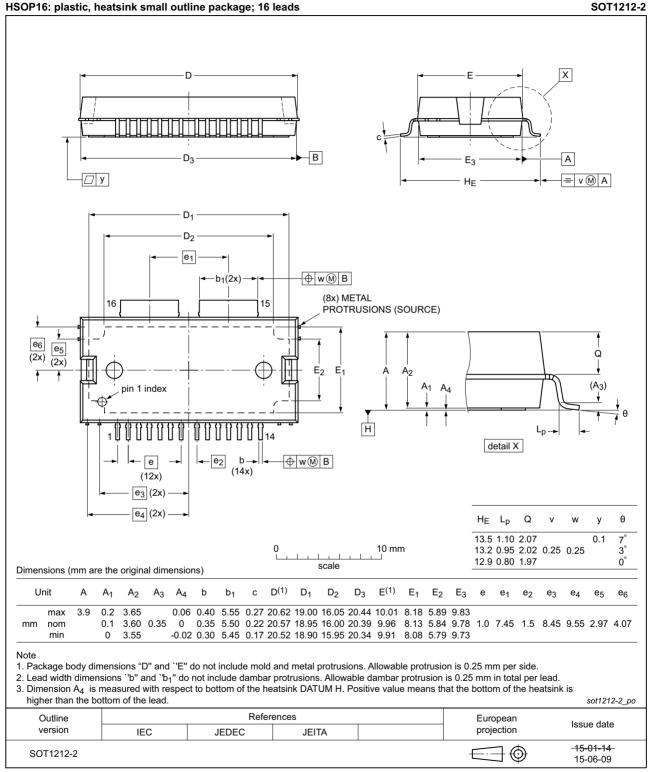
LDMOS 2-stage power MMIC

# 9. Package outline



### Fig 13. Package outline SOT1211-2 (HSOP16F)

LDMOS 2-stage power MMIC



#### Fig 14. Package outline SOT1212-2 (HSOP16)

# **10. Handling information**

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

# 11. Abbreviations

Table 10. Abbreviations				
Acronym	Description			
AM	Amplitude Modulation			
3GPP	3rd Generation Partnership Project			
CCDF	Complementary Cumulative Distribution Function			
CW	Continuous Wave			
DPCH	Dedicated Physical CHannel			
ESD	ElectroStatic Discharge			
GEN8	Eighth Generation			
LDMOS	Laterally Diffused Metal Oxide Semiconductor			
MMIC	Monolithic Microwave Integrated Circuit			
MTF	Median Time to Failure			
OBO	Output Back Off			
PAR	Peak-to-Average Ratio			
PM	Phase Modulation			
VSWR	Voltage Standing-Wave Ratio			
W-CDMA	Wideband Code Division Multiple Access			

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# 12. Revision history

## Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM8G0710S-45AB_S-45ABG v.3	20151015	Product data sheet	-	BLM8G0710S-45AB_ S-45ABG#2
Modifications:	<ul> <li>Table 5 on</li> <li>Table 6 on</li> <li>Table 7 on</li> <li>Table 8 on</li> <li>Section 8.2</li> <li>Table 9 on</li> <li>Figure 10 of</li> <li>Figure 11 of</li> </ul>	page 1: table updated page 4: table updated page 4: table updated page 5: table updated page 6: table updated con page 9: section updated page 10: table updated on page 13: figure updated on page 13: notes update on page 14: notes update	ed d	
BLM8G0710S-45AB_S-45ABG#2	20150901	Objective data sheet	-	BLM8G0710S-45AB_ S-45ABG v.1
Modifications:	<ul> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon</li> <li>Legal texts have been adapted to the new company name where appropriate</li> </ul>			
BLM8G0710S-45AB_S-45ABG v.1	20150820	Objective data sheet	-	-

# 13. Legal information

# **13.1 Data sheet status**

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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