BLF888B; BLF888BS

UHF power LDMOS transistor

Rev. 2 — 12 July 2013 **Product data sheet**

1. Product profile

1.1 General description

A 650 W LDMOS RF power transistor for broadcast transmitter applications and industrial applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

Table 1. Application information

RF performance at V_{DS} = 50 V unless otherwise specified.

Mode of operation	f (MHz)	$P_{L(AV)}$ (W)	$P_{L(M)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)	IMD_{shldr} (dBc)	PAR (dB)
RF performance in a common source 860 MHz narrowband test circuit								
2-tone, class-AB	f_1 = 860; f_2 = 860.1	250	-	21	46	–34	-	-
DVB-T (8k OFDM)	858	120	-	21	33	-	–31 [1]	8.2 [2]
RF performance in a common source 470 MHz to 860 MHz broadband test circuit								
DVB-T (8k OFDM)	858	120	-	20	32	-	–32 [1]	8.0 [2]

[1] Measured [dBc] with delta marker at 4.3 MHz from center frequency.

[2] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

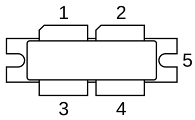
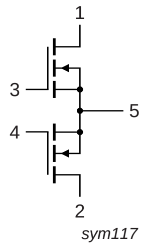
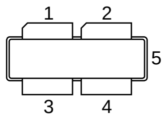
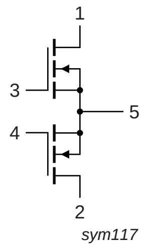
- Excellent ruggedness
- Optimum thermal behavior and reliability, $R_{th(j-c)}$ = 0.15 K/W
- High power gain
- High efficiency
- Designed for broadband operation (470 MHz to 860 MHz)
- Internal input matching for high gain and optimum broadband operation
- Excellent reliability
- Easy power control
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

1.3 Applications

- Communication transmitter applications in the UHF band
- Industrial applications in the UHF band

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF888B (SOT539A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLF888BS (SOT539B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF888B	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF888BS	-	earless flanged balanced LDMOST ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	104	V
V_{GS}	gate-source voltage		–0.5	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; $P_{L(AV)}$ = 125 W	[1]	0.15	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.4 mA	[1]	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 240 mA	[1]	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V		-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V		-	38	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V		-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.5 A	[1]	-	120	-	mΩ
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	[2]	-	210	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz		-	67	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz		-	1.35	-	pF

[1] I_D is the drain current.

[2] Capacitance values without internal matching.

Table 7. RF characteristics

RF characteristics in NXP production narrowband test circuit; T_{case} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
2-Tone, class-AB							
V_{DS}	drain-source voltage			-	50	-	V
I_{Dq}	quiescent drain current		[1]	-	1.3	-	A
$P_{L(AV)}$	average output power	f_1 = 860 MHz; f_2 = 860.1 MHz		250	-	-	W
G_p	power gain	f_1 = 860 MHz; f_2 = 860.1 MHz		20	21	-	dB
η_D	drain efficiency	f_1 = 860 MHz; f_2 = 860.1 MHz		42	46	-	%
IMD3	third-order intermodulation distortion	f_1 = 860 MHz; f_2 = 860.1 MHz		-	–34	–30	dBc

Table 7. RF characteristics *…continued*

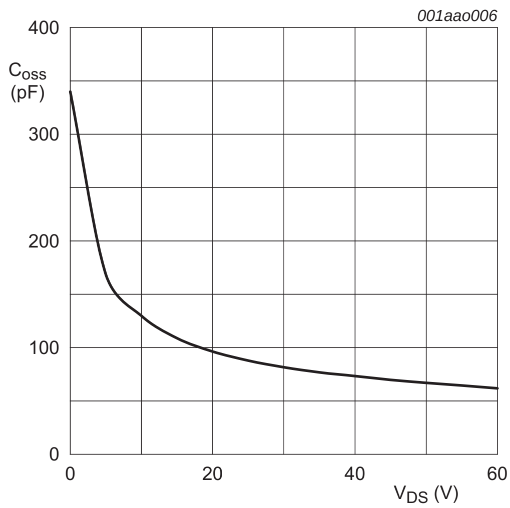
RF characteristics in NXP production narrowband test circuit; T_{case} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DVB-T (8k OFDM), class-AB							
V_{DS}	drain-source voltage			-	50	-	V
I_{Dq}	quiescent drain current		[1]	-	1.3	-	A
$P_{L(AV)}$	average output power	f = 858 MHz		120	-	-	W
G_p	power gain	f = 858 MHz		20	21	-	dB
η_D	drain efficiency	f = 858 MHz		30	33	-	%
IMD_{shldr}	intermodulation distortion shoulder	f = 858 MHz	[2]	-	–31	–27	dBc
PAR	peak-to-average ratio	f = 858 MHz	[3]	-	8.2	-	dB

[1] I_{dq} for total device

[2] Measured [dBc] with delta marker at 4.3 MHz from center frequency.

[3] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.



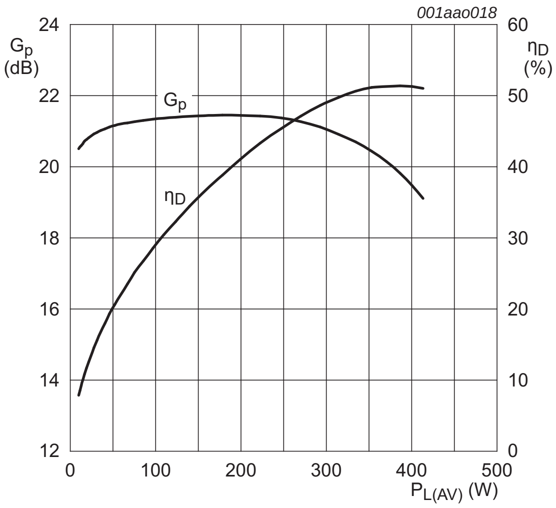
V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; typical values per section

7. Application information

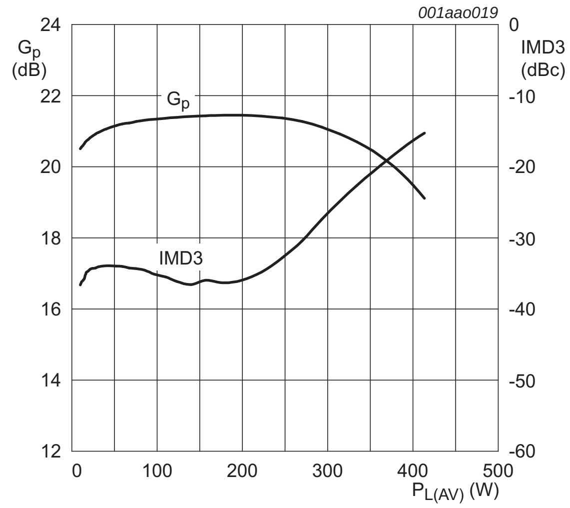
7.1 Narrowband RF figures

7.1.1 2-Tone



V_{DS} = 50 V; I_{Dq} = 1.3 A; measured in a common source narrowband 860 MHz test circuit.

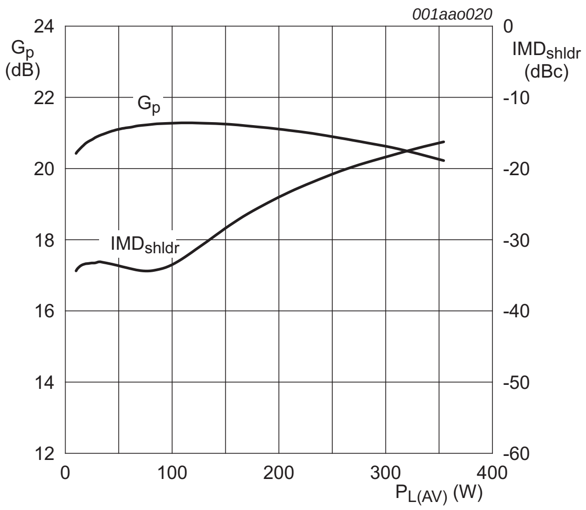
Fig 2. 2-Tone power gain and drain efficiency as function of load power; typical values



V_{DS} = 50 V; I_{Dq} = 1.3 A; measured in a common source narrowband 860 MHz test circuit.

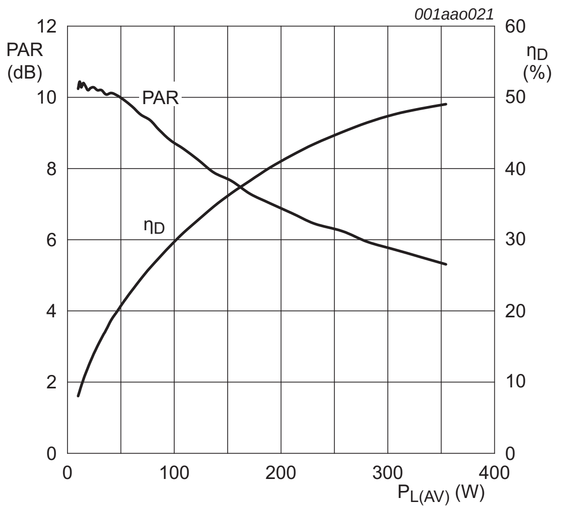
Fig 3. 2-Tone power gain and third order intermodulation distortion as load power; typical values

7.1.2 DVB-T



V_{DS} = 50 V; I_{Dq} = 1.3 A; measured in a common source narrowband 860 MHz test circuit.

Fig 4. DVB-T power gain and intermodulation distortion shoulder as function of load power; typical values

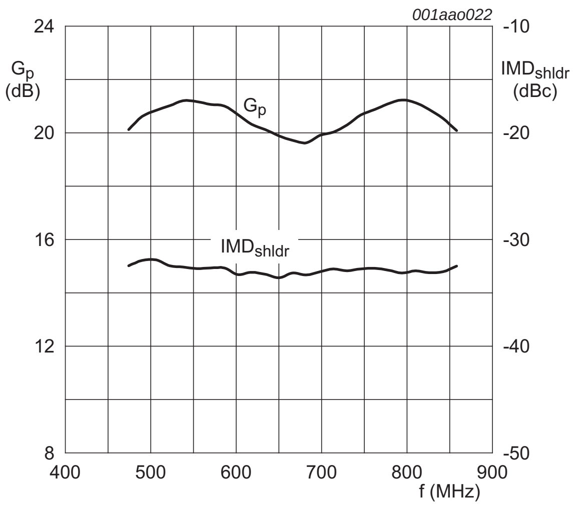


V_{DS} = 50 V; I_{Dq} = 1.3 A; measured in a common source narrowband 860 MHz test circuit.

Fig 5. DVB-T peak-to-average ratio and drain efficiency as function of load power; typical values

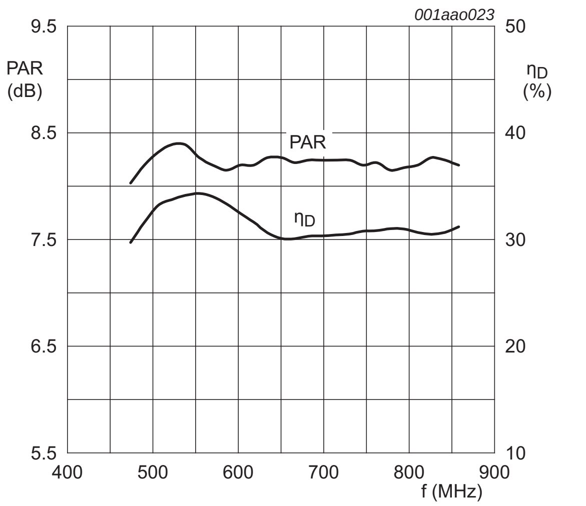
7.2 Broadband RF figures

7.2.1 DVB-T



$P_{L(AV}$ =120 W; V_{DS} = 50 V; I_{Dq} = 1.3 A; measured in a common source broadband test circuit as described in Section 8.

Fig 6. DVB-T power gain and intermodulation distortion shoulder as function of frequency; typical values



$P_{L(AV}$ =120 W; V_{DS} = 50 V; I_{Dq} = 1.3 A; measured in a common source broadband test circuit as described in Section 8.

Fig 7. DVB-T peak-to-average ratio and drain efficiency as function of frequency; typical values

7.3 Impedance information

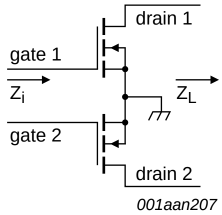


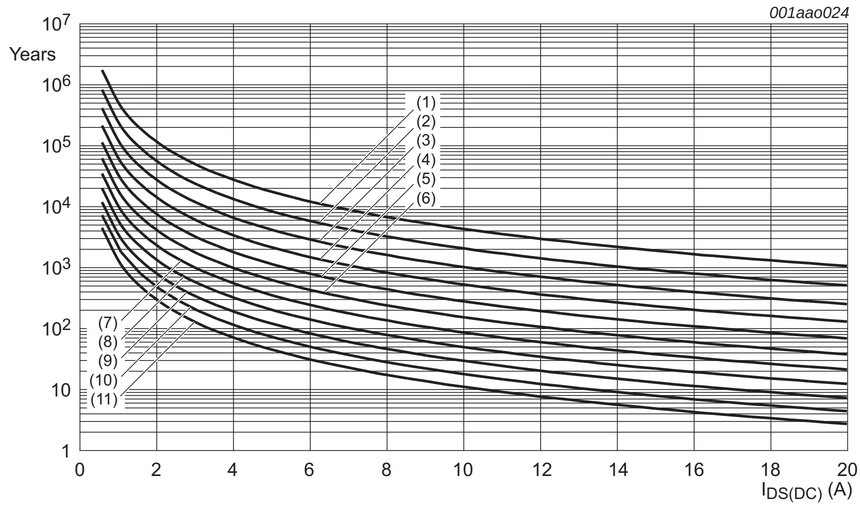
Fig 8. Definition of transistor impedance

Table 8. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and $P_{L(AV)}$ = 120 W (DVB-T).

f MHz	Z_i Ω	Z_L Ω
300	0.617 – j1.715	4.792 + j0.947
325	0.635 – j1.355	4.707 + j0.994
350	0.655 – j1.026	4.619 + j1.035
375	0.677 – j0.721	4.528 + j1.069
400	0.702 – j0.435	4.435 + j1.097
425	0.731 – j0.164	4.340 + j1.118
450	0.762 + j0.096	4.243 + j1.134
475	0.798 + j0.347	4.147 + j1.143
500	0.839 + j0.592	4.049 + j1.146
525	0.884 + j0.833	3.952 + j1.144
550	0.936 + j1.072	3.855 + j1.136
575	0.995 + j1.310	3.759 + j1.123
600	1.063 + j1.549	3.663 + j1.105
625	1.141 + j1.791	3.569 + j1.083
650	1.230 + j2.037	3.477 + j1.055
675	1.334 + j2.289	3.385 + j1.024
700	1.456 + j2.548	3.296 + j0.989
725	1.599 + j2.814	3.209 + j0.949
750	1.768 + j3.090	3.123 + j0.907
775	1.971 + j3.376	3.039 + j0.861
800	2.214 + j3.671	2.958 + j0.812
825	2.510 + j3.975	2.879 + j0.761
850	2.873 + j4.282	2.801 + j0.706
875	3.320 + j4.584	2.726 + j0.650
900	3.875 + j4.865	2.654 + j0.591
925	4.562 + j5.095	2.583 + j0.530
950	5.409 + j5.223	2.514 + j0.467
975	6.426 + j5.166	2.448 + j0.403
1000	7.587 + j4.807	2.384 + j0.337

7.4 Reliability



TTF (0.1 % failure fraction).

The reliability at pulsed conditions can be calculated as follows: TTF (0.1 %) $\times$ 1 / δ.

(1) T_j = 100 °C

(2) T_j = 110 °C

(3) T_j = 120 °C

(4) T_j = 130 °C

(5) T_j = 140 °C

(6) T_j = 150 °C

(7) T_j = 160 °C

(8) T_j = 170 °C

(9) T_j = 180 °C

(10) T_j = 190 °C

(11) T_j = 200 °C

Fig 9. BLF888B; BLF888BS electromigration ($I_{DS(DC)}$, total device)

8. Test information

Table 9. List of components

For test circuit, see Figure 10, Figure 11 and Figure 12.

Component	Description	Value		Remarks
B1, B2	semi rigid coax	25 Ω; 49.5 mm		UT-090C-25 (EZ 90-25)
C1	multilayer ceramic chip capacitor	12 pF	[1]	
C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	8.2 pF	[1]	
C7	multilayer ceramic chip capacitor	6.8 pF	[2]	
C8	multilayer ceramic chip capacitor	2.7 pF	[2]	
C9	multilayer ceramic chip capacitor	2.2 pF	[2]	
C10, C13, C14	multilayer ceramic chip capacitor	100 pF	[3]	
C11, C12	multilayer ceramic chip capacitor	10 pF	[2]	
C15, C16	multilayer ceramic chip capacitor	4.7 μF, 50 V		Kemet C1210X475K5RAC-TU or capacitor of same quality.
C17, C18, C23, C24	multilayer ceramic chip capacitor	100 pF	[2]	
C19, C20	multilayer ceramic chip capacitor	10 μF, 50 V		TDK C570X7R1H106KT000N or capacitor of same quality.
C21, C22	electrolytic capacitor	470 μF; 63 V		
C30	multilayer ceramic chip capacitor	10 pF	[4]	
C31	multilayer ceramic chip capacitor	9.1 pF	[4]	
C32	multilayer ceramic chip capacitor	3.9 pF	[4]	
C33, C34, C35	multilayer ceramic chip capacitor	100 pF	[4]	
C36, C37	multilayer ceramic chip capacitor	4.7 μF, 50 V		TDK C4532X7R1E475MT020U or capacitor of same quality.
L1	microstrip	-	[5]	(W × L) 15 mm × 13 mm
L2	microstrip	-	[5]	(W × L) 5 mm × 26 mm
L3, L32	microstrip	-	[5]	(W × L) 2 mm × 49.5 mm
L4	microstrip	-	[5]	(W × L) 1.7 mm × 3.5 mm
L5	microstrip	-	[5]	(W × L) 2 mm × 9.5 mm
L30	microstrip	-	[5]	(W × L) 5 mm × 13 mm
L31	microstrip	-	[5]	(W × L) 2 mm × 11 mm
L33	microstrip	-	[5]	(W × L) 2 mm × 3 mm
R1, R2	wire resistor	10 Ω		
R3, R4	SMD resistor	5.6 Ω		0805
R5, R6	wire resistor	100 Ω		
R7, R8	potentiometer	10 kΩ		

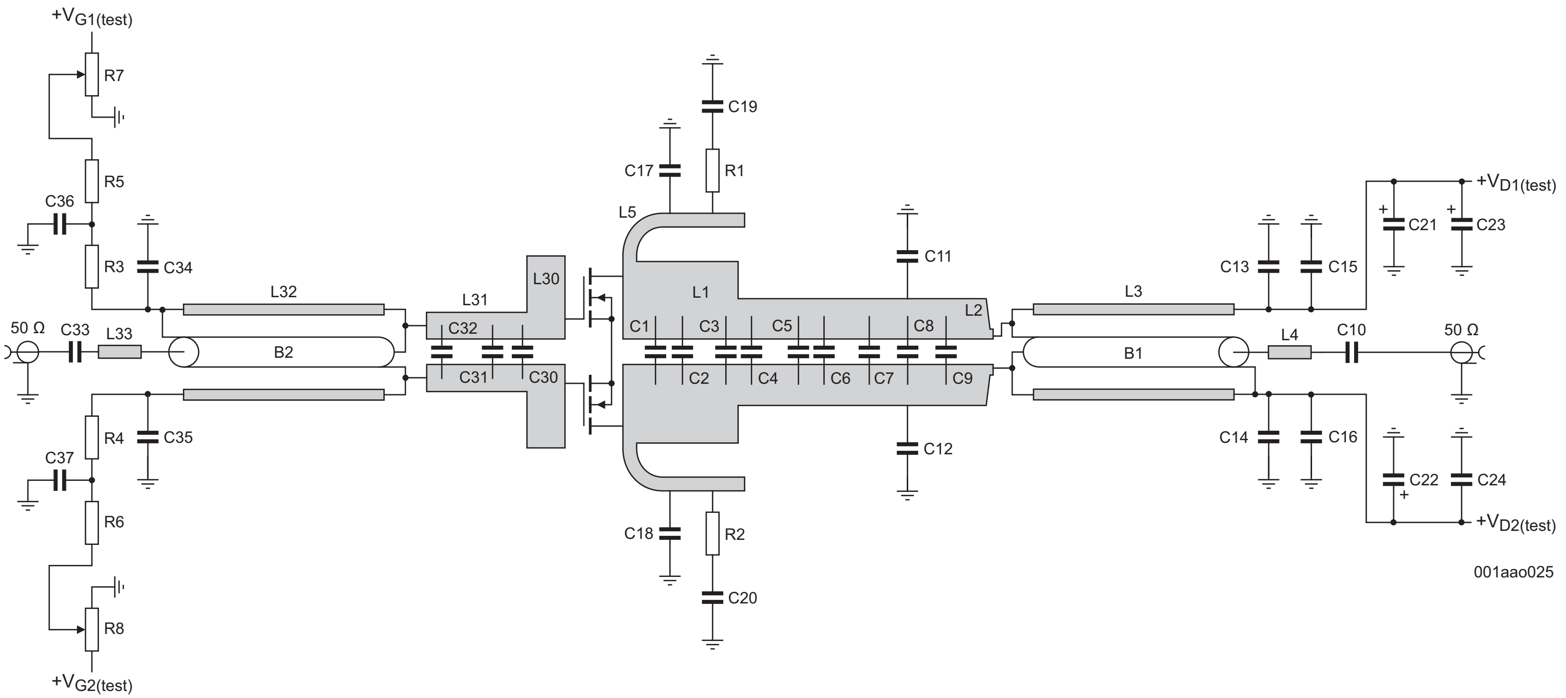
[1] American technical ceramics type 800R or capacitor of same quality.

[2] American technical ceramics type 800B or capacitor of same quality.

[3] American technical ceramics type 180R or capacitor of same quality.

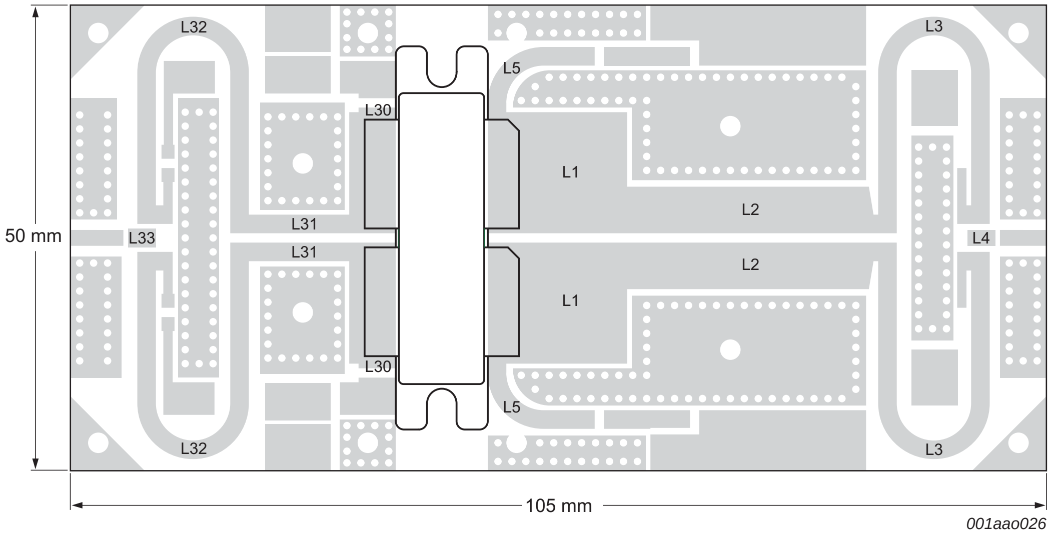
[4] American technical ceramics type 100A or capacitor of same quality.

[5] Printed-Circuit Board (PCB): Taconic RF35; ε_r = 3.5 F/m; height = 0.762 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.



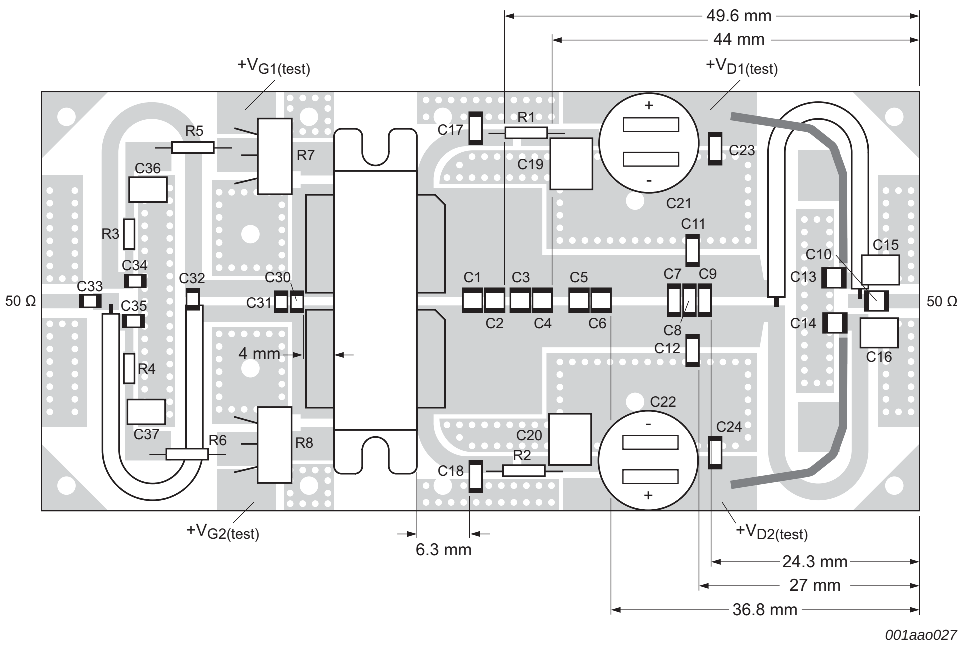
See Table 9 for a list of components.

Fig 10. Class-AB common source broadband amplifier; $V_{D1(test)}$, $V_{D2(test)}$, $V_{G1(test)}$ and $V_{G2(test)}$ are drain and gate test voltages



See Table 9 for a list of components.

Fig 11. Printed-Circuit Board (PCB) for class-AB common source amplifier

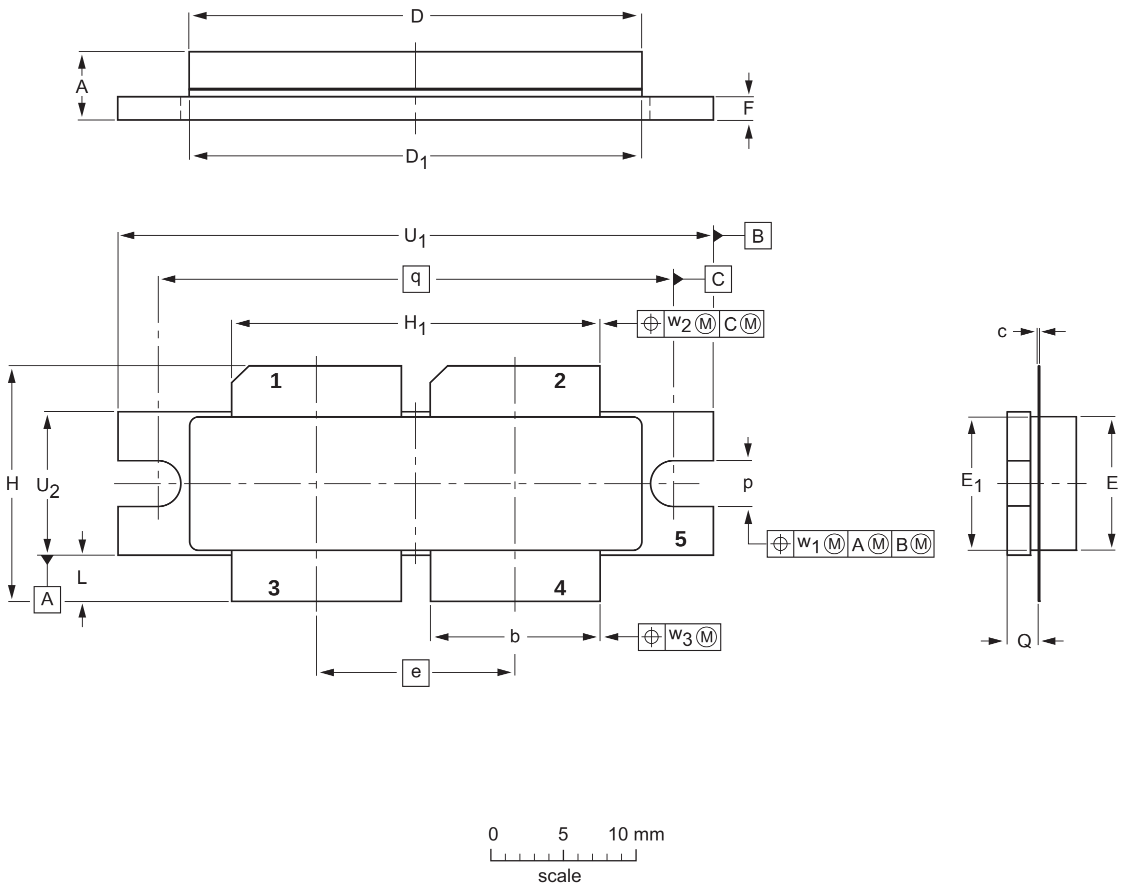


See Table 9 for a list of components.

Fig 12. Component layout for class-AB common source amplifier

9. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

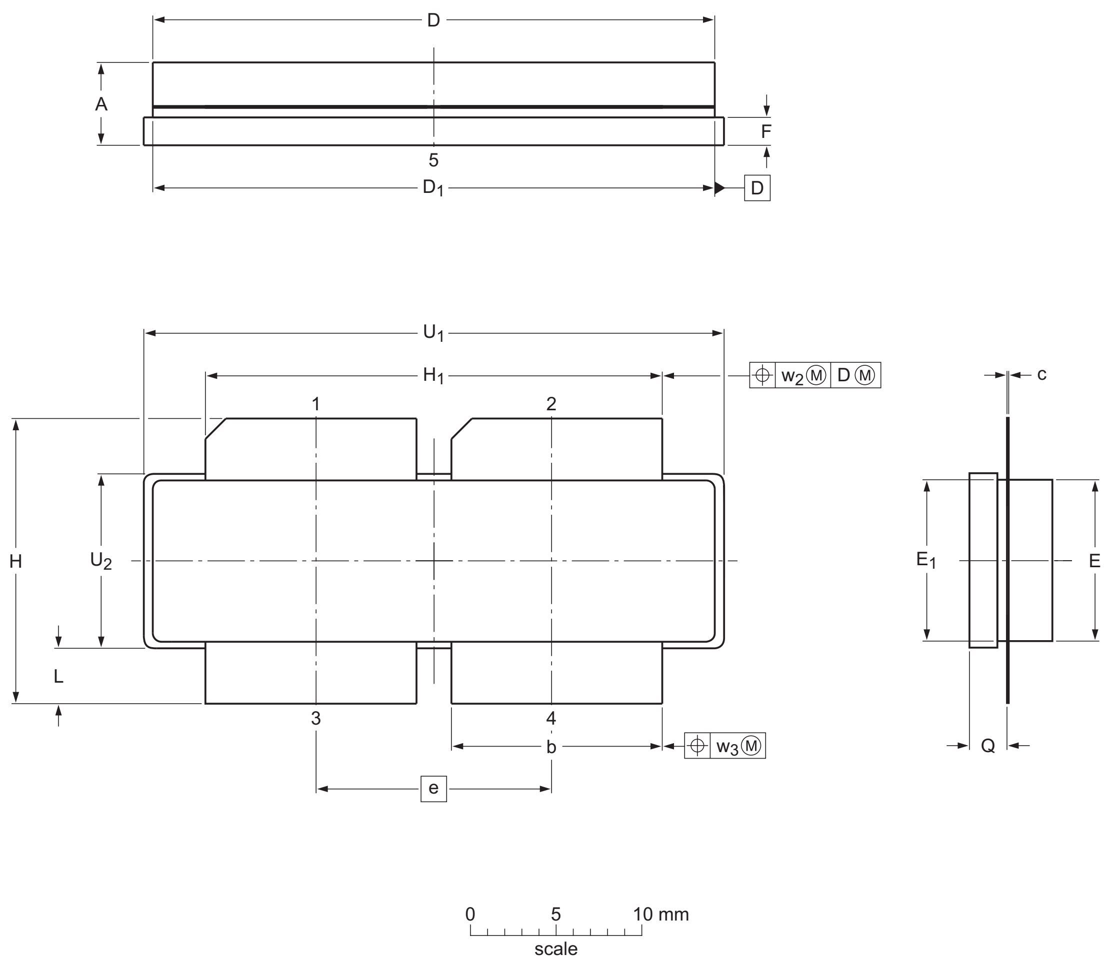
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 13. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 14. Package outline SOT539B

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
DVB	Digital Video Broadcast
DVB-T	Digital Video Broadcast - Terrestrial
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
SMD	Surface Mounted Device
TTF	Time-To-Failure
UHF	Ultra High Frequency
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF888B_BLF888BS v.2	20130712	Product data sheet	-	BLF888B_BLF888BS v.1
Modifications:	• The package outline Figure 14 is updated. • Translation disclaimer added to the legal text.			
BLF888B_BLF888BS v.1	20111017	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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