BLF882; BLF882S

UHF power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 200 W LDMOS RF power transistor for broadcast transmitter applications and industrial applications. The transistor can deliver 200 W in broadband applications from HF to 860 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital transmitter applications.

Table 1. Test information

RF performance at T_{case} = 25 °C in a class-AB test circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	PAR
	(MHz)	(V)	(W)	(dB)	(%)	(dB)
RF performance in a class-AB 705 MHz narrowband test circuit						
CW, class-AB	705	50	180	21	62	-
CW pulsed, class-AB	705	50	200	21	63	-
RF performance in a class-AB 470 MHz to 705 MHz broadband test circuit						
DVB-T (8k OFDM)	470 to 705	50	33	20	28 to 31	8.0 to 8.4 [1]

[1] PAR of output signal at 0.01% probability on CCDF; PAR of input signal = 9.5 dB at 0.01% probability on CCDF.

1.2 Features and benefits

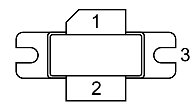
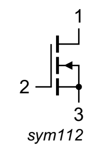
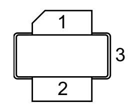
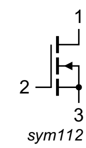
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- Transmitter applications in the HF to 860 MHz frequency range
- Industrial applications in the HF to 860 MHz frequency range
- Broadcast transmitters

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF882 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLF882S (SOT502B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF882	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF882S	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	104	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 85 °C; P_L = 180 W [1]	0.56	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.2 mA	[1]	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 120 mA	[1]	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V		-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	[1]	-	19	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V		-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 4.25 A	[1]	-	240	-	mΩ

[1] I_D is the drain current

Table 7. AC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	105	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	34	-	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.7	-	pF

Table 8. RF characteristics
Test signal: CW pulsed; RF characteristics in Ampleon production narrowband test circuit; T_j = 25 °C; unless otherwise specified.

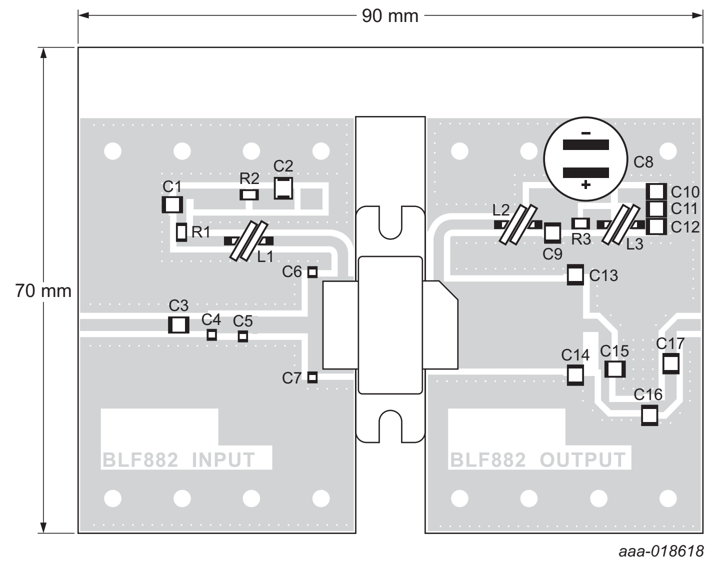
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage		-	50	-	V
I_{Dq}	quiescent drain current		-	100	-	mA
$P_{L(AV)}$	average output power	f = 705 MHz; t_p = 100 μs; δ = 10 %	196	200	-	W
G_p	power gain		19.6	20.6	-	dB
η_D	drain efficiency		60	63	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF882 and BLF882S are capable of withstanding a load mismatch corresponding to VSWR ≥ 20 : 1 through all phases under the following conditions: V_{DS} = 50 V; f = 705 MHz at rated $P_{L(1dB)}$.

7.2 Test circuit



Printed-Circuit Board (PCB): Taconic RF-35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm, gold plated.

See Table 9 for a list of components.

Fig 1. Component layout for class-AB production test circuit

Table 9. List of components

For test circuit see Figure 1.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	62 pF [1]	
C2	multilayer ceramic chip capacitor	100 nF	
C3, C9	multilayer ceramic chip capacitor	56 pF [1]	
C4	multilayer ceramic chip capacitor	12 pF [2]	
C5	multilayer ceramic chip capacitor	11 pF [2]	
C6, C7	multilayer ceramic chip capacitor	24 pF [2]	
C8	electrolytic capacitor	220 μF	
C10, C11, C12	electrolytic capacitor	750 pF [1]	
C13	multilayer ceramic chip capacitor	16 pF [3]	
C14	multilayer ceramic chip capacitor	18 pF [3]	
C15	multilayer ceramic chip capacitor	5.6 pF [3]	
C16	multilayer ceramic chip capacitor	6.8 pF [3]	
C17	multilayer ceramic chip capacitor	56 pF [3]	
L1, L2, L3	3 turn 1 mm spiral coil	D = 3.0 mm; 120 nH	
R1, R2	resistor	10 Ω	SMD 1206
R3	resistor	15 Ω	SMD 1206

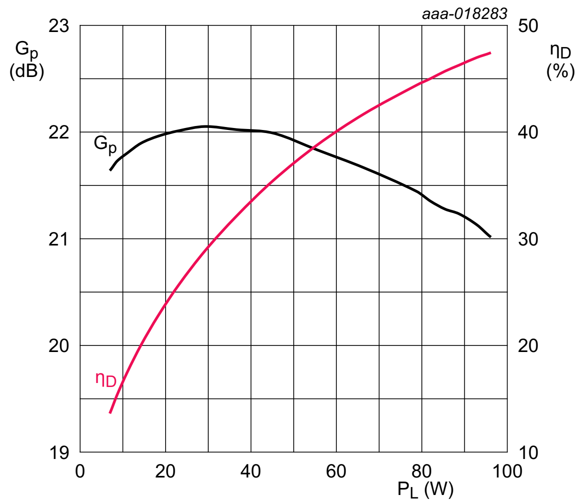
[1] American Technical Ceramics type 100B.

[2] American Technical Ceramics type 800A.

[3] American Technical Ceramics type 800B.

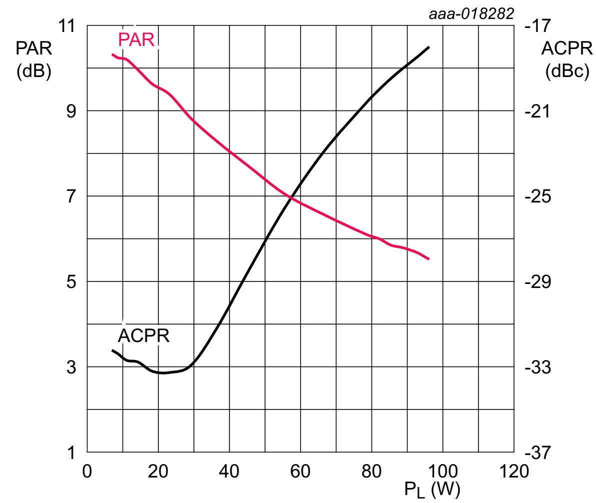
7.3 Graphical data

7.3.1 DVB-T



V_{DS} = 50 V; I_{Dq} = 100 mA; f = 705 MHz.

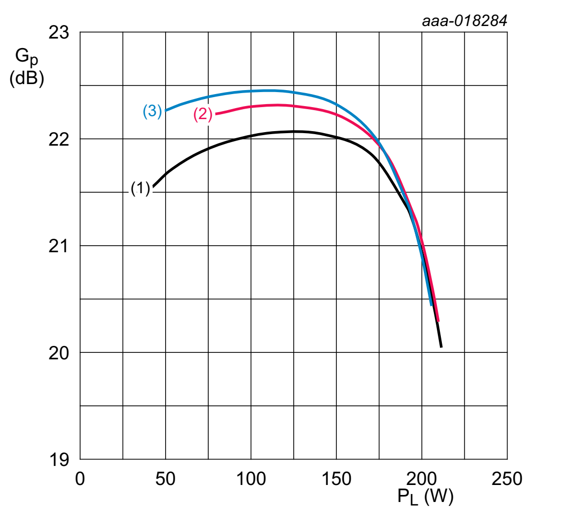
Fig 2. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 100 mA; f = 705 MHz; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

Fig 3. Peak-to-average ratio and adjacent channel power ratio as function of output power; typical values

7.3.2 CW pulsed



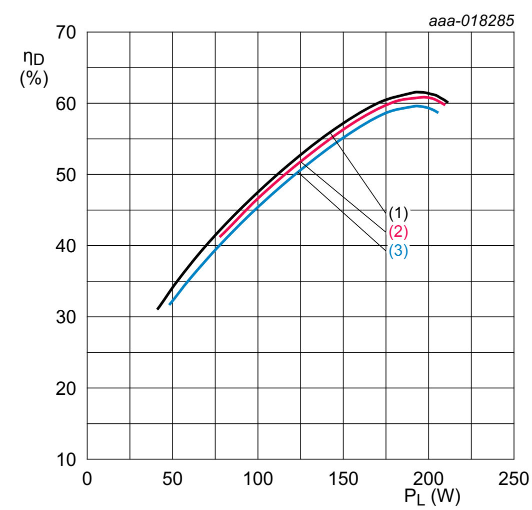
V_{DS} = 50 V; f = 705 MHz; t_p = 100 µs; δ = 10 %.

(1) I_{Dq} = 100 mA

(2) I_{Dq} = 200 mA

(3) I_{Dq} = 300 mA

Fig 4. Power gain as a function of output power; typical values



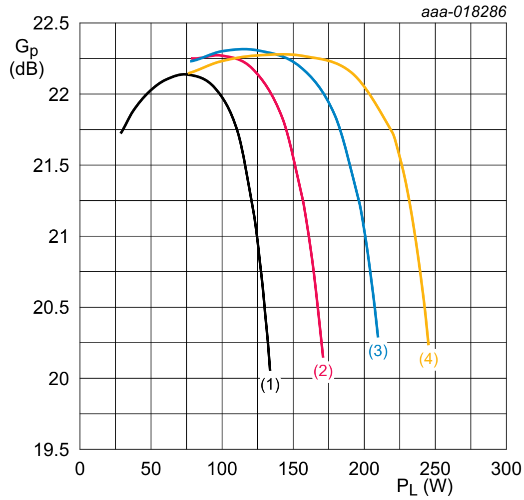
V_{DS} = 50 V; f = 705 MHz; t_p = 100 µs; δ = 10 %.

(1) I_{Dq} = 100 mA

(2) I_{Dq} = 200 mA

(3) I_{Dq} = 300 mA

Fig 5. Drain efficiency as a function of output power; typical values



I_{Dq} = 100 mA; f = 705 MHz; t_p = 100 μs; δ = 10 %.

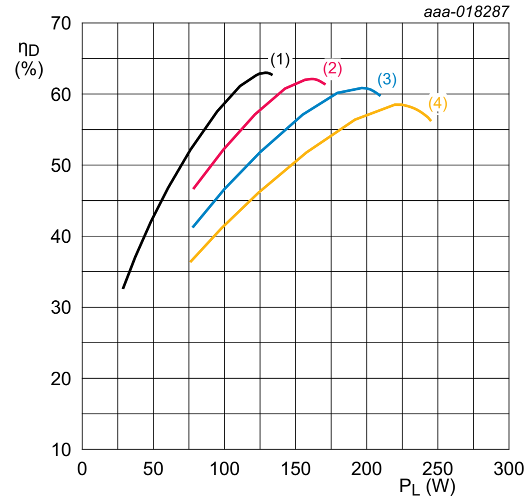
(1) V_{DS} = 40 V

(2) V_{DS} = 45 V

(3) V_{DS} = 50 V

(4) V_{DS} = 55 V

Fig 6. Power gain as a function of output power; typical values



I_{Dq} = 100 mA; f = 705 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 40 V

(2) V_{DS} = 45 V

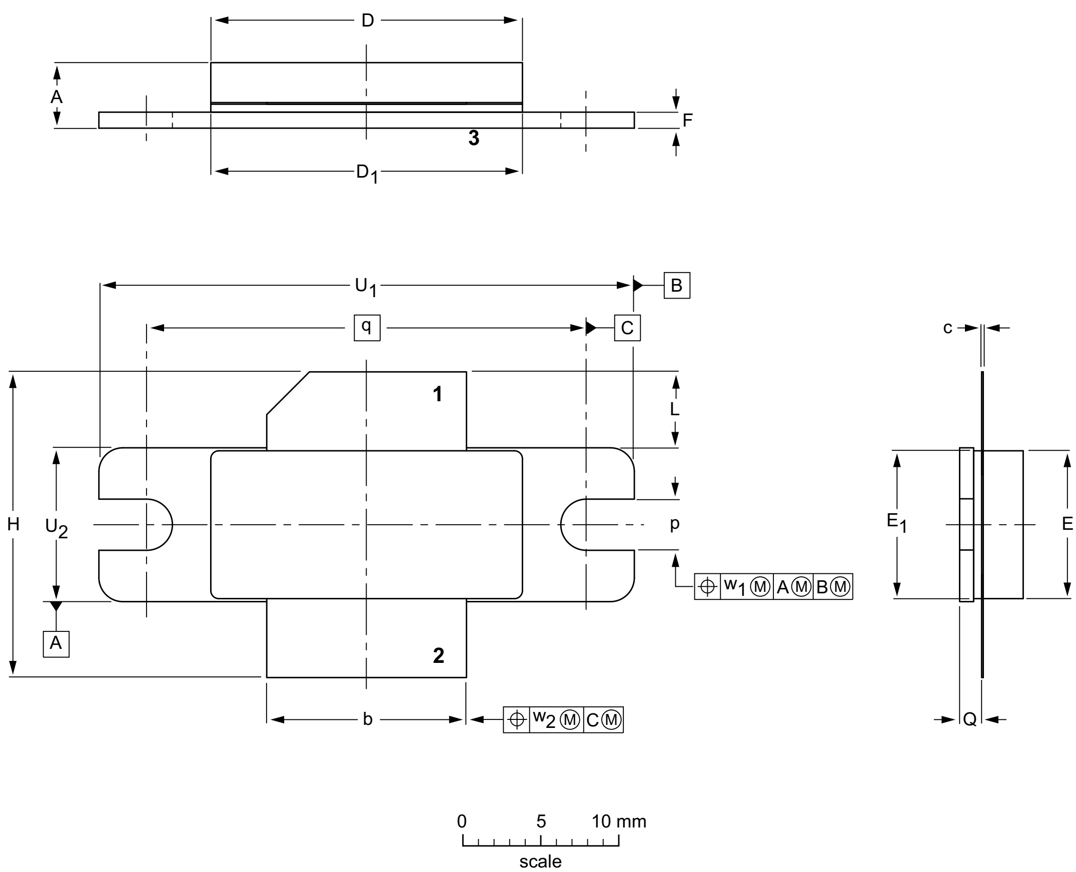
(3) V_{DS} = 50 V

(4) V_{DS} = 55 V

Fig 7. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



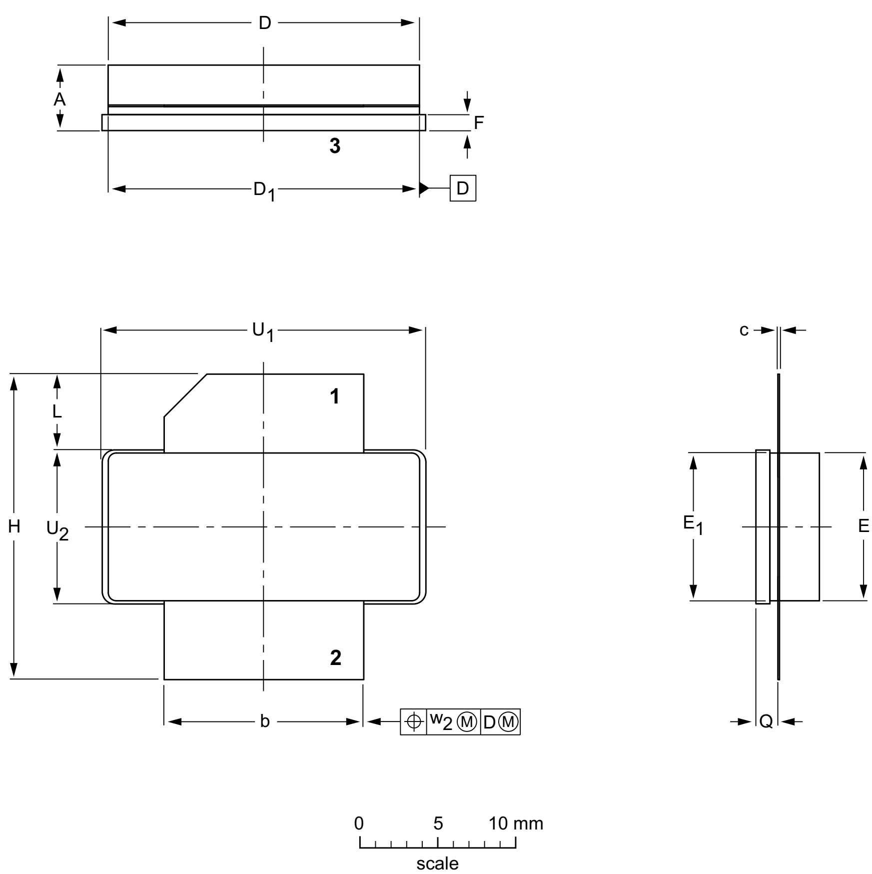
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 8. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 9. Package outline SOT502B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuos Wave
ESD	ElectroStatic Discharge
DVB-T	Digital Video Broadcast - Terrestrial
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF882_BLF882S#3	20150901	Product data sheet	-	BLF882_BLF882S v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF882_BLF882S v.2	20150703	Product data sheet	-	BLF882_BLF882S v.1
BLF882_BLF882S v.1	20141219	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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