BLF647P

Broadband power LDMOS transistor

Rev. 2 — 12 April 2013 **Product data sheet**

1. Product profile

1.1 General description

A 200 W LDMOS RF power transistor for broadcast transmitter and industrial applications. The transistor is suitable for the frequency range HF to 1500 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

Table 1. Application information

RF performance at T_h = 25 °C in a common source test circuit.

Test signal	f (MHz)	V_{DS} (V)	I_{Dq} (A)	$P_{L(AV)}$ (W)	$P_{L(M)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)
Pulsed, class-B	1300	32	0.1	-	200	18	70	-
CW, class-B	1300	32	0.1	200	-	18	70	-
2-tone, class-AB	f_1 = 1299.95; f_2 = 1300.05	32	0.7	75	-	19	48	–33

1.2 Features and benefits

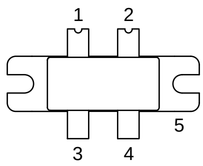
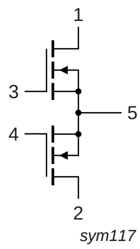
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications in the HF to 1500 MHz frequency range
- Industrial applications in the HF to 1500 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF647P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 200 W [1]	0.34	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 28 V; I_D = 110 mA	1.55	1.8	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	18.1	20	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 20 V; I_D = 5500 mA	-	7.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.85 A	-	140	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	78	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	30	-	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	1.3	-	pF

Table 8. RF characteristics

Test signal: CW; f = 1300 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

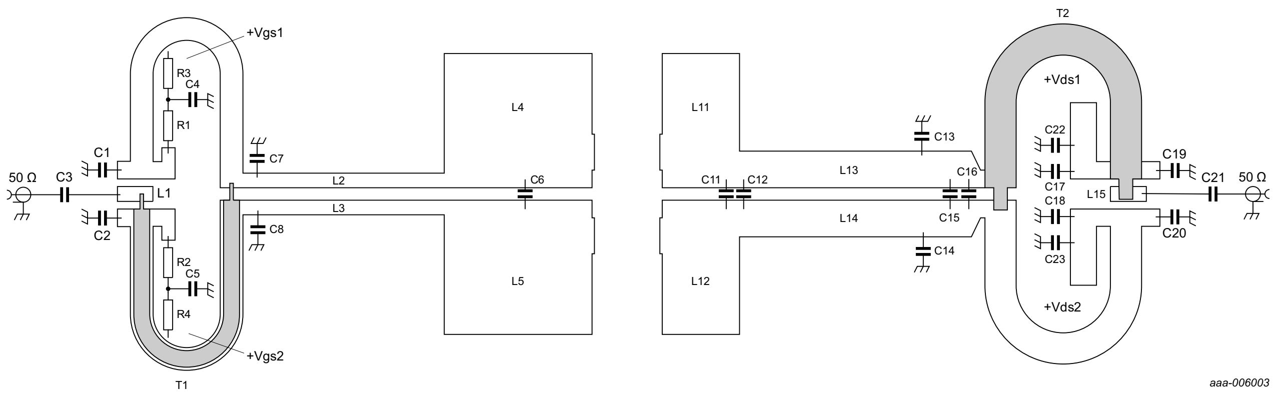
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 200 W	17	18	-	dB
η_D	drain efficiency	P_L = 200 W	66	70	-	%

7. Test information

7.1 Ruggedness in class-AB operation

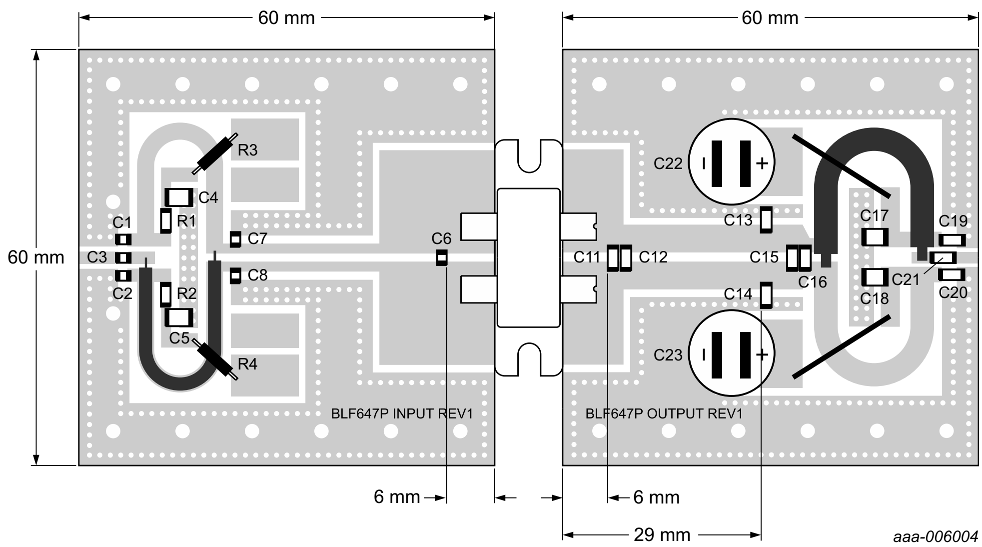
The BLF647P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 1300 MHz at rated load power.

7.2 Test circuit information



See Table 9 for a list of components.

Fig 1. Schematic for class-AB production test circuit



See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

Table 9. List of components

Printed-Circuit Board (PCB): RF 35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm. See Figure 1 and Figure 2.

Component	Description	Value		Remarks
C1, C2, C3	multilayer ceramic chip capacitor	68 pF	[1]	
C4, C5	multilayer ceramic chip capacitor	4.7 μF, 50 V		
C6	multilayer ceramic chip capacitor	2.4 pF	[2]	
C7, C8	multilayer ceramic chip capacitor	4.7 pF	[1]	
C11	multilayer ceramic chip capacitor	3.3 pF	[3]	
C12	multilayer ceramic chip capacitor	2.4 pF	[3]	
C13, C14	multilayer ceramic chip capacitor	3.3 pF	[3]	
C15, C16	multilayer ceramic chip capacitor	1.2 pF	[3]	
C17, C18	multilayer ceramic chip capacitor	4.7 μF, 50 V		
C19, C20, C21	multilayer ceramic chip capacitor	220 pF	[3]	
C22, C23	electrolytic capacitor	470 μF, 63 V		
L1	microstrip			(L × W) 4 mm × 1.7 mm
L2, L3	microstrip			(L × W) 22.5 mm × 1.6 mm
L4, L5	microstrip			(L × W) 16.5 mm × 15 mm
L11, L12	microstrip			(L × W) 8.5 mm × 15 mm
L13, L14	microstrip			(L × W) 26 mm × 4.2 mm
L15	microstrip			(L × W) 4 mm × 1.7 mm
R1, R2	SMD resistor	5.6 Ω		SMD1206
R3, R4	WIRE resistor	100 Ω		
T1	semi rigid coax	25 Ω, 40 mm		UT-090C-25
T2	semi rigid coax	25 Ω, 40 mm		UT-141C-25

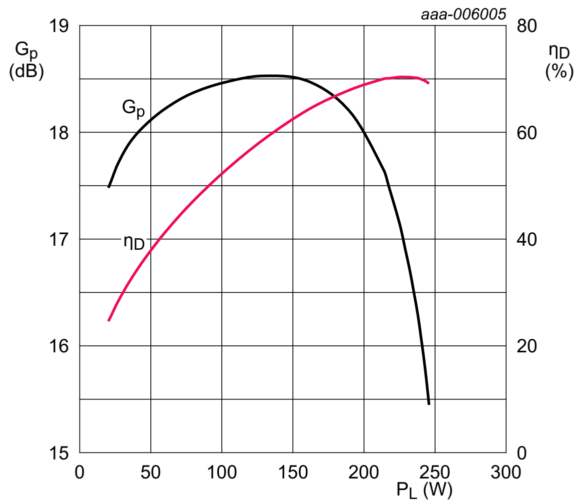
[1] American Technical Ceramics type 800A or capacitor of same quality.

[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.

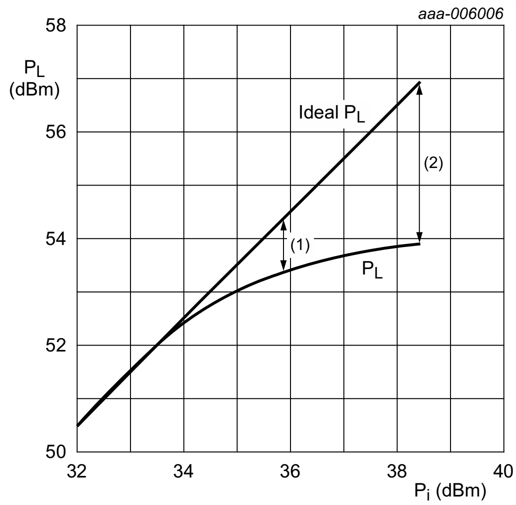
7.3 Graphical data

7.3.1 1-Tone CW



V_{DS} = 32 V; I_{Dq} = 100 mA; f = 1300 MHz.

Fig 3. Power gain and drain efficiency as function of output power; typical values

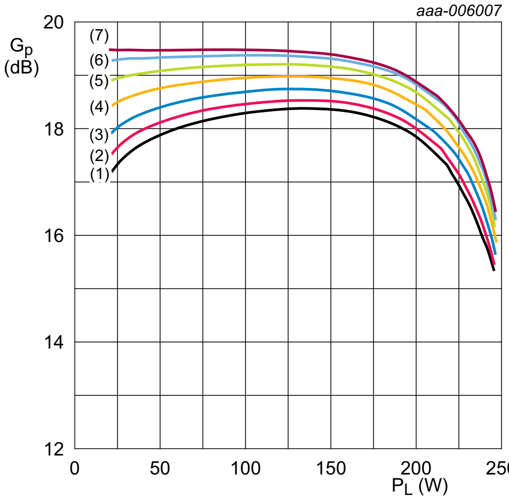


V_{DS} = 32 V; I_{Dq} = 100 mA; f = 1300 MHz.

(1) $P_{L(1dB)}$ = 53.4 dBm (217 W)

(2) $P_{L(3dB)}$ = 53.9 dBm (245 W)

Fig 4. Output power as a function of input power; typical values



V_{DS} = 32 V; f = 1300 MHz.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

(3) I_{Dq} = 200 mA

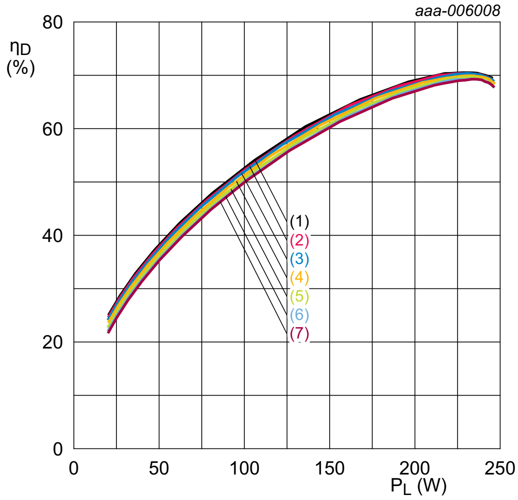
(4) I_{Dq} = 300 mA

(5) I_{Dq} = 700 mA

(6) I_{Dq} = 1000 mA

(7) I_{Dq} = 1200 mA

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 32 V; f = 1300 MHz.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

(3) I_{Dq} = 200 mA

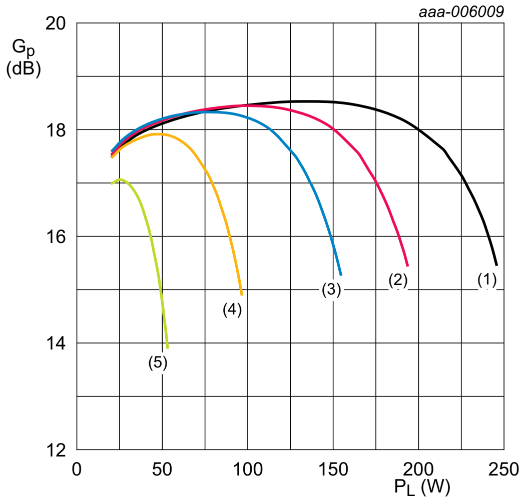
(4) I_{Dq} = 300 mA

(5) I_{Dq} = 700 mA

(6) I_{Dq} = 1000 mA

(7) I_{Dq} = 1200 mA

Fig 6. Drain efficiency as a function of output power; typical values



I_{Dq} = 100 mA; f = 1300 MHz.

(1) V_{DS} = 32 V

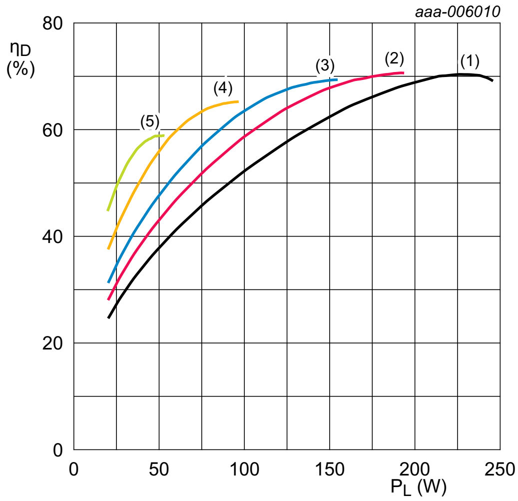
(2) V_{DS} = 28 V

(3) V_{DS} = 25 V

(4) V_{DS} = 20 V

(5) V_{DS} = 15 V

Fig 7. Power gain as a function of output power; typical values



I_{Dq} = 100 mA; f = 1300 MHz.

(1) V_{DS} = 32 V

(2) V_{DS} = 28 V

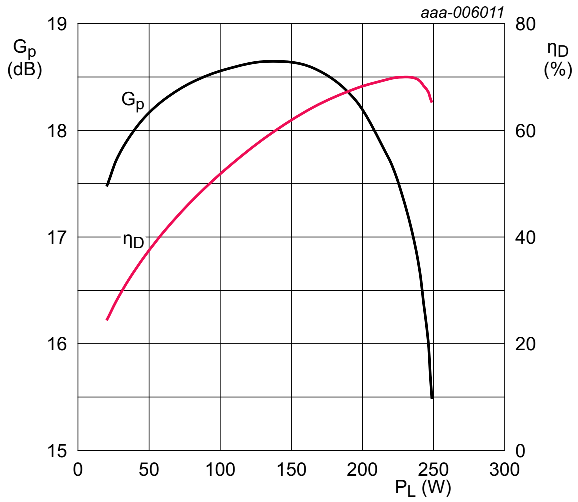
(3) V_{DS} = 25 V

(4) V_{DS} = 20 V

(5) V_{DS} = 15 V

Fig 8. Drain efficiency as a function of output power; typical values

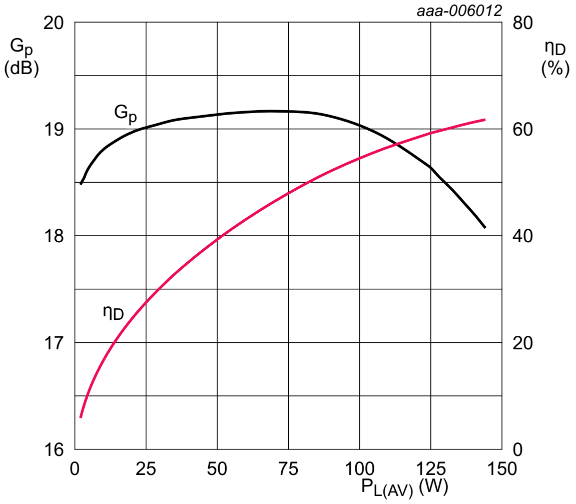
7.3.2 1-Tone pulsed



V_{DS} = 32 V; I_{Dq} = 100 mA; f = 1300 MHz; t_p = 100 μs; δ = 20%.

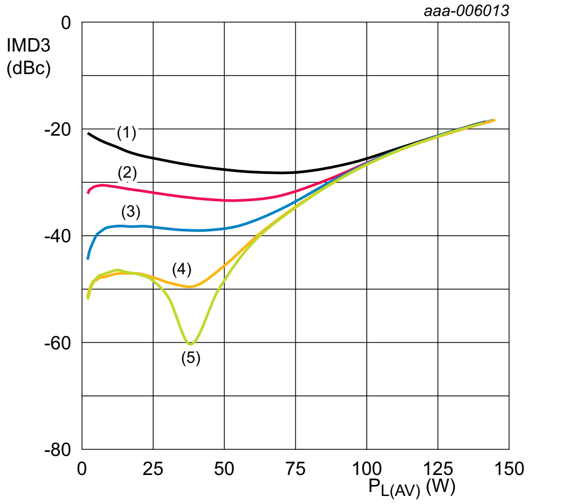
Fig 9. Power gain and drain efficiency as function of output power; typical values

7.3.3 2-Tone CW



V_{DS} = 50 V; I_{Dq} = 700 mA; f_1 = 1299.95 MHz; f_2 = 1300.05 MHz.

Fig 10. Power gain and drain efficiency as function of average output power; typical values



V_{DS} = 32 V; f_1 = 1299.95 MHz; f_2 = 1300.05 MHz.

(1) I_{Dq} = 100 mA

(2) I_{Dq} = 400 mA

(3) I_{Dq} = 700 mA

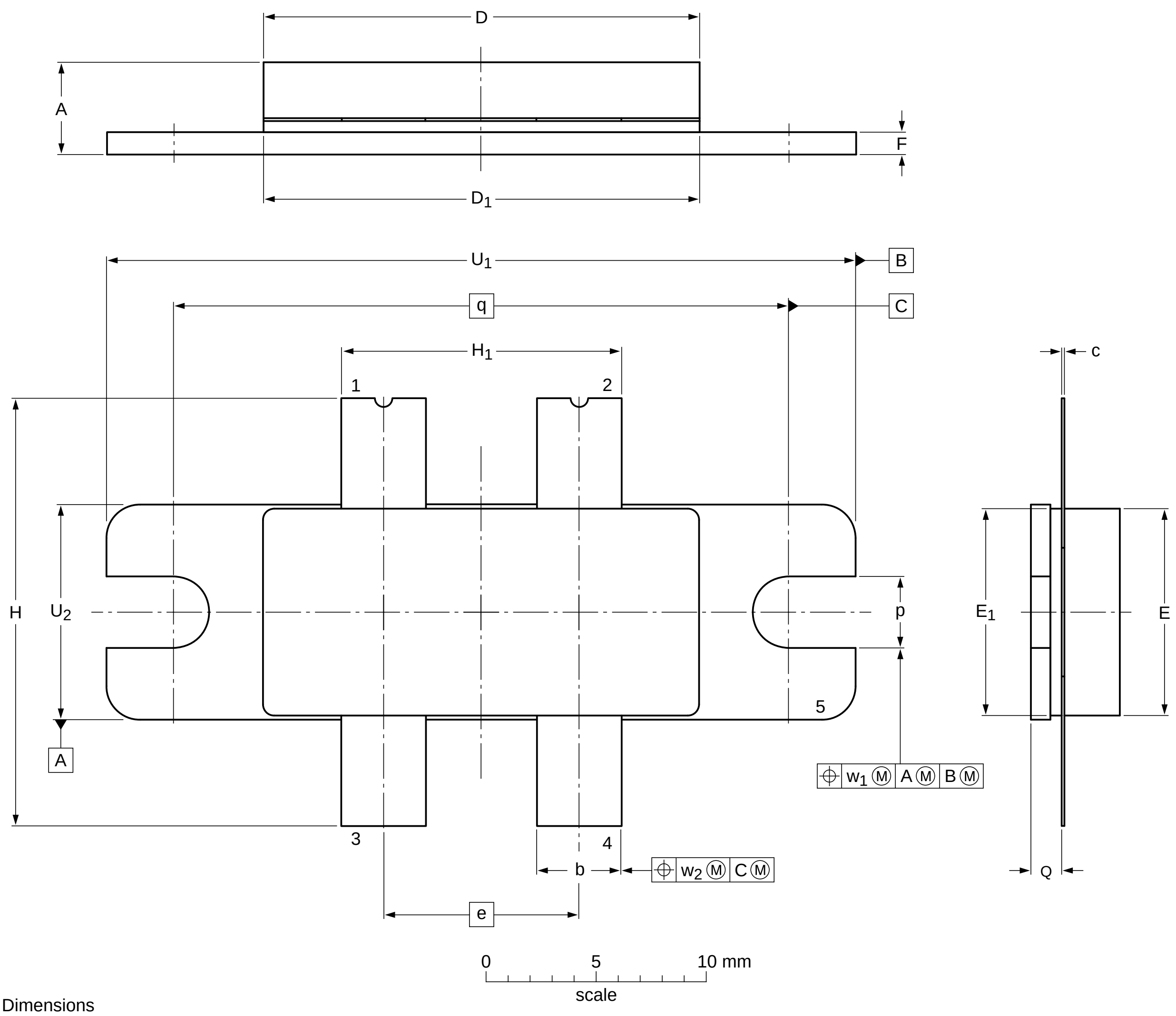
(4) I_{Dq} = 1000 mA

(5) I_{Dq} = 1200 mA

Fig 11. Third order intermodulation distortion as a function of average output power; typical values

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads **SOT1121A**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q(2)	q	U_1	U_2	w_1	w_2
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70		34.16	9.91		
	nom						8.89								27.94			0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66		9.27	9.27	0.89	18.92	12.57	3.12	1.45		33.91	9.65		
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067		1.345	0.39		
	nom						0.35								1.1			0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.123	0.057		1.335	0.38		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121A						~~09-10-12~~ 10-02-02

Fig 12. Package outline SOT1121A

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF647P v.2	20130412	Product data sheet	-	BLF647P_BLF647PS v.1
Modifications:	• This document now only describes the BLF647P product. • Table 1 on page 1: table has been updated • Section 1.2 on page 1: some items have been removed • Table 4 on page 2: table has been updated • Table 5 on page 2: typical value has been changed to 0.34 • Table 6 on page 3: table has been updated • Table 8 on page 3: table has been updated • Section 7 on page 3: section has been added • Section 7.1 on page 3: section has been moved to Section 7 • Section 9 on page 11: section has been added			
BLF647P_BLF647PS v.1	20120803	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

Date of release: 12 April 2013
Document identifier: BLF647P