# BLF2425M8L140; BLF2425M8LS140 Power LDMOS transistor Rev. 2 — 1 September 2015

**AMMPLEON** 

Product data sheet

## **Product profile**

#### 1.1 General description

140 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M8L140 and BLF2425M8LS140 are designed for high-power CW applications and are assembled in high performance ceramic packages, available in eared and earless versions

#### **Typical performance** Table 1.

Typical RF performance at  $T_{case}$  = 25 °C;  $I_{Dq}$  = 1300 mA in a common source class-AB production

Test signal	f	V <sub>DS</sub>	P <sub>L(AV)</sub>	Gp	$\eta_{D}$
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	28	140	19	56

#### 1.2 Features and benefits

- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

#### 1.3 Applications

Industrial, scientific and medical applications in the frequency range from 2400 MHz to 2500 MHz

## 2. Pinning information

Table 2. Pinning

Table 2.	Filling			
Pin	Description		Simplified outline	Graphic symbol
BLF2425	M8L140 (SOT502A)			
1	drain			,
2	gate			1 
3	source	<u>[1]</u>		2
				3 sym112
DI E2425	M8LS140 (SOT502B)			3911112
DLFZ4Z5	W6L5140 (501502B)			
1	drain			4
2	gate			, L <sup>'</sup>
3	source	<u>[1]</u>		2
				3
				sym112

<sup>[1]</sup> Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Packag	Package				
	Name	Description	Version			
BLF2425M8L140	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A			
BLF2425M8LS140	-	earless flanged ceramic package; 2 leads	SOT502B			

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage			-	65	V
V <sub>GS</sub>	gate-source voltage			-0.5	+13	V
T <sub>stg</sub>	storage temperature			-65	-	°C
Tj	junction temperature		<u>[1]</u>	-	225	°C

<sup>[1]</sup> Continuous use at maximum temperature will affect the reliability

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$R_{\text{th(j-c)}}$	thermal resistance from junction to case	$T_{case}$ = 80 °C; $P_L$ = 125 W	0.28	K/W

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#### 6. Characteristics

Table 6. DC characteristics

 $T_i = 25$  °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.16 \text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS}$ = 10 V; $I_{D}$ = 216 mA	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V}$	-	-	5	μА
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	41	-	Α
$I_{GSS}$	gate leakage current	$V_{GS}$ = 11 V; $V_{DS}$ = 0 V	-	-	500	nA
g <sub>fs</sub>	forward transconductance	$V_{DS}$ = 10 V; $I_{D}$ = 10.8 A	-	16	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 7.56 \text{ A}$	-	69	-	mΩ

Table 7. RF characteristics

Test signal: CW; f = 2450 MHz;  $V_{DS} = 28$  V;  $I_{Dq} = 1300$  mA;  $T_{case} = 25$  °C unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	$P_{L} = 140 \text{ W}$	17.5	19	-	dB
RLin	input return loss	$P_{L} = 140 \text{ W}$	-	-16	-8	dB
$\eta_{D}$	drain efficiency	$P_{L} = 140 \text{ W}$	51	56	-	%

#### 7. Test information

#### 7.1 Ruggedness in class-AB operation

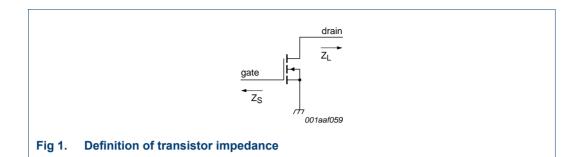
The BLF2425M8L140 and BLF2425M8LS140 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 1300 \text{ mA}$ ;  $P_L = 140 \text{ W}$  (CW); f = 2450 MHz.

## 7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified.  $I_{Dq} = 1300$  mA;  $V_{DS} = 28$  V.  $Z_S$  and  $Z_L$  defined in Figure 1.

f	Z <sub>S</sub>	Z <sub>L</sub>
(MHz)	(Ω)	(Ω)
2400	3.7 - 5.4j	1.3 – 1.5j
2450	6.9 – 5.0j	1.5 – 1.6j
2500	8.7 – 2.0j	1.5 – 1.6j



#### 7.3 Circuit information

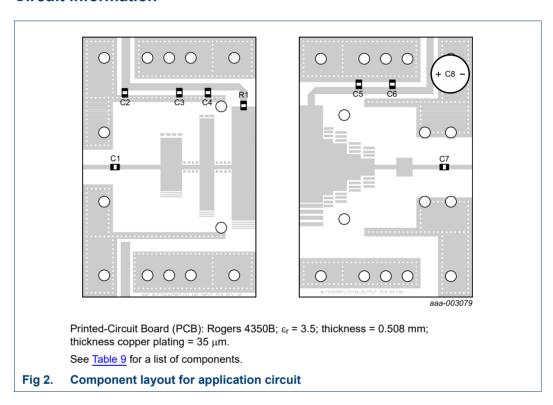
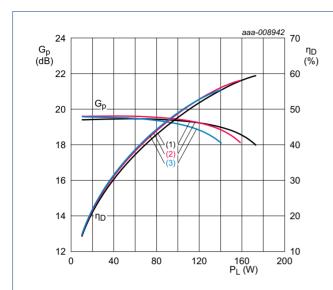


Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C4, C5	multilayer ceramic chip capacitor	15 pF	ATC100B
C2, C6	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C3	multilayer ceramic chip capacitor	100 nF	Murata
C7	multilayer ceramic chip capacitor	62 pF	ATC100B
C8	electrolytic capacitor	22 μF, 63 V	
R1	resistor	10 Ω	SMD 0805; Bourns

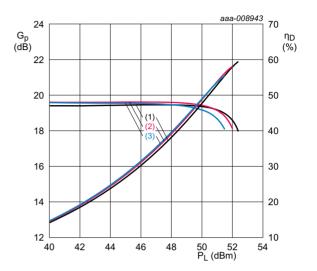
## 7.4 Graphical data



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 1300 mA.

- (1) f = 2400 MHz
- (2) f = 2450 MHz
- (3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of output power, typical values



 $V_{DS}$  = 28 V;  $I_{Dq}$  = 1300 mA.

- (1) f = 2400 MHz
- (2) f = 2450 MHz
- (3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of output power, typical values

## 8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

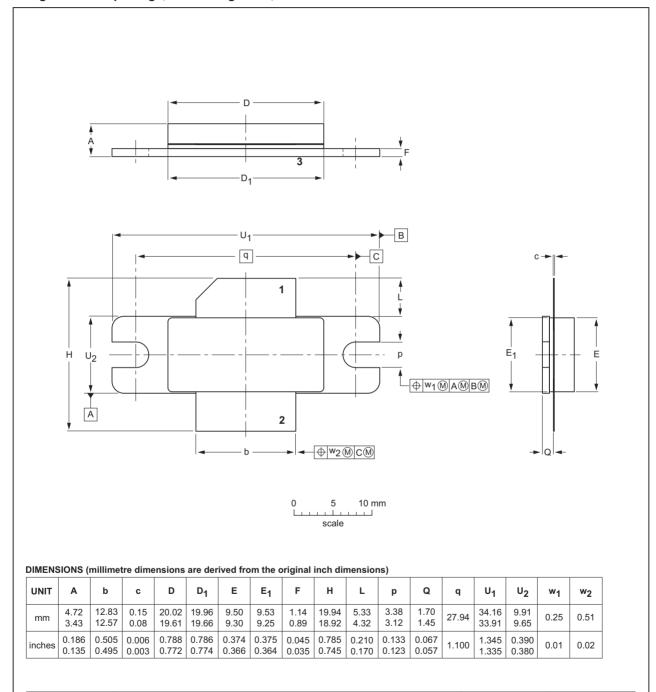


Fig 5. Package outline SOT502A

**IEC** 

OUTLINE

VERSION

SOT502A

**JEITA** 

REFERENCES

**JEDEC** 

**ISSUE DATE** 

03-01-10

12-05-02

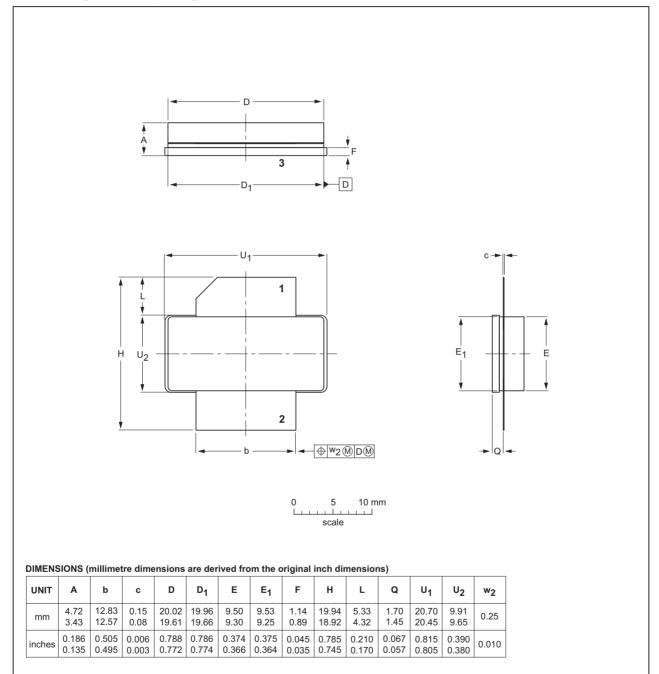
**EUROPEAN** 

**PROJECTION** 

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#### Earless flanged ceramic package; 2 leads

SOT502B



OUTLINE	ITLINE REFERENCES				EUROPEAN	ISSUE DATE
VERSION	N IEC JEDEC JEITA		PROJECTION	ISSUE DATE		
SOT502B						<del>07-05-09</del> 12-05-02

Fig 6. Package outline SOT502B

## 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
BLF2425M8L140_2425M8LS140 v.2	20150901	Product data sheet	-	BLF2425M8L140_ 2425M8LS140 v.1		
Modifications:	The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.					
	Legal texts have been adapted to the new company name where appropriate.					
BLF2425M8L140_2425M8LS140 v.1	20130827	Product data sheet	-	-		

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#### 12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## BLF2425M8L(S)140

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## **AMPLEON**

## BLF2425M8L(S)140

**Power LDMOS transistor** 

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