## BLF184XR; BLF184XRS

# Power LDMOS transistor Rev. 4 — 1 September 2015

**AMPLEON** 

Product data sheet

#### **Product profile** 1.

#### 1.1 General description

A 700 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. **Application information** 

Test signal	f	V <sub>DS</sub>	PL	Gp	$\eta_D$
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	700	23.9	73.5
CW	108	50	750	23.5	81.9

#### 1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

#### 1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified of	outline Graphic symb	ool
BLF184)	(R (SOT1214A)			
1	drain1		_	
2	drain2	1 ]	2 1	
3	gate1	2[	5	
4	gate2	3	4	<b>-</b> 5
5	source	[1]	4 —	
			' <b>-</b>	
			2 sym	117
BLF184X	(RS (SOT1214B)			
1	drain1			
2	drain2	1 ]	2 1	
3	gate1		_]	
4	gate2	3	4 5 3 -	<b>-</b> 5
5	source	[1]	4	
			<b>'</b> ⊢¬	
			2 sym	117

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Packag	Package				
	Name	Name Description				
BLF184XR	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1214A			
BLF184XRS	-	earless flanged ceramic package; 4 leads	SOT1214B			

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	135	V
$V_{GS}$	gate-source voltage		-6	+11	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

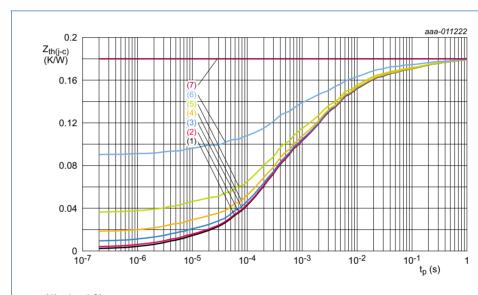
[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Тур	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	T <sub>j</sub> = 150 °C	[1][2]	0.18	K/W
Z <sub>th(j-c)</sub>	transient thermal impedance from junction to case	$T_j$ = 150 °C; $t_p$ = 100 μs; $\delta$ = 20 %	[3]	0.065	K/W

- [1] T<sub>i</sub> is the junction temperature.
- [2]  $R_{th(j-c)}$  is measured under RF conditions.
- [3] See Figure 3.



- (1)  $\delta = 1 \%$
- (2)  $\delta = 2 \%$
- (3)  $\delta = 5 \%$
- (4)  $\delta = 10 \%$
- (5)  $\delta = 20 \%$
- (6)  $\delta = 50 \%$
- (7)  $\delta = 100 \% (DC)$

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

## 6. Characteristics

Table 6. DC characteristics

 $T_j = 25$  °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.75 \text{ mA}$	135	-	-	٧
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_D = 275 \text{ mA}$	1.25	1.9	2.25	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 50 \text{ V}; I_{D} = 50 \text{ mA}$	-	1.6	-	V

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Table 6. DC characteristics ...continued

 $T_i$  = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I <sub>DSS</sub>	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}$	-	-	1.4	μΑ
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	38.5	-	Α
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	140	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ $I_D = 9.625 A$	-	0.16	-	Ω

#### Table 7. AC characteristics

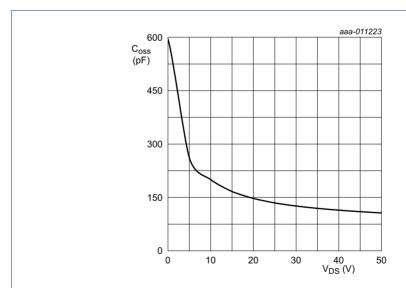
 $T_i$  = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C <sub>rs</sub>	feedback capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	3.1	-	pF
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	292	-	pF
Coss	output capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; f = 1 MHz	-	107	-	pF

#### Table 8. RF characteristics

Test signal: pulsed RF;  $t_p$  = 100  $\mu$ s;  $\delta$  = 20 %; f = 108 MHz; RF performance at  $V_{DS}$  = 50 V;  $I_{Dq}$  = 100 mA;  $T_{case}$  = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$G_p$	power gain	P <sub>L</sub> = 700 W	22.8	23.9	-	dB
RLin	input return loss	P <sub>L</sub> = 700 W	-	-20	-13	dB
$\eta_{D}$	drain efficiency	P <sub>L</sub> = 700 W	71	73.5	-	%



 $V_{GS} = 0 V$ ; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

## 7. Test information

#### 7.1 Ruggedness in class-AB operation

The BLF184XR and BLF184XRS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions:  $V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 100 \text{ mA}$ ;  $P_L = 700 \text{ W}$  pulsed; f = 108 MHz.

#### 7.2 Impedance information

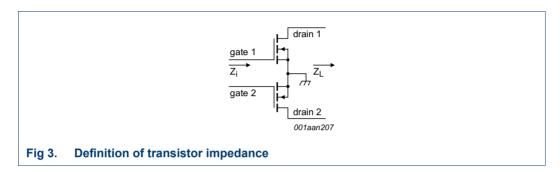


Table 9. Typical push-pull impedance

Simulated  $Z_i$  and  $Z_L$  device impedance; impedance info at  $V_{DS}$  = 50 V and  $P_L$  = 700 W.

f	Z <sub>i</sub>	$Z_L$
(MHz)	(Ω)	(Ω)
108	5.8 – j19.1	5.5 + j1.0

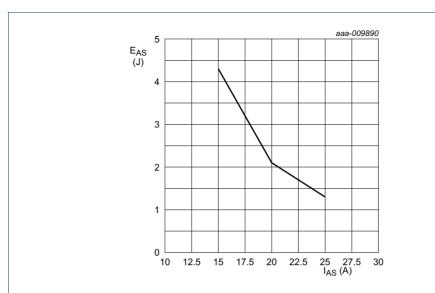
#### 7.3 UIS avalanche energy

#### Table 10. Typical avalanche data per section

 $T_{amb}$  = 25 °C; typical test data; test jig without water cooling.

las	E <sub>AS</sub>
(A)	(J)
	4.3
20	2.1
25	1.3

For information see application note AN10273.



Non-repetitive avalanche energy as a function of single pulse avalanche current, Fig 4. typical values

#### 7.4 Test circuit

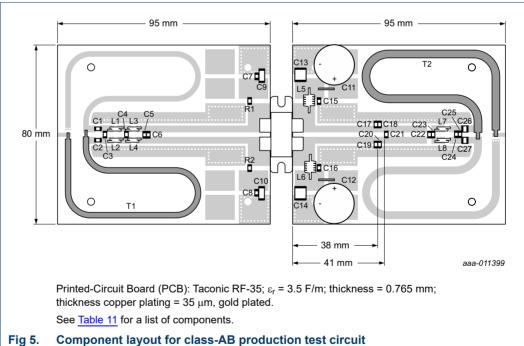


Table 11. List of components For test circuit see Figure 5.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	910 pF [1]	
C3	multilayer ceramic chip capacitor	47 pF [1]	
C4	multilayer ceramic chip capacitor	51 pF [1]	

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**Table 11.** List of components ...continued For test circuit see Figure 5.

Component	Description	Value	Remarks
C5	multilayer ceramic chip capacitor	100 pF [1]	
C6, C23	multilayer ceramic chip capacitor	20 pF	
C7, C8, C15, C16	multilayer ceramic chip capacitor	820 pF [1]	
C9, C10, C13, C14	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK C5750X7R2A475KT
C11, C12	electrolytic capacitor	1000 μF, 63 V	
C17, C19	multilayer ceramic chip capacitor	39 pF [1]	
C18, C20	multilayer ceramic chip capacitor	27 pF [1]	
C21	multilayer ceramic chip capacitor	7.5 pF [1]	
C22	multilayer ceramic chip capacitor	22 pF [1]	
C24, C25	multilayer ceramic chip capacitor	27 pF [1]	
C26, C27	multilayer ceramic chip capacitor	1 nF [2]	
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 2.8 mm	
L5, L6	5.5 turn 0.8 mm copper wire	D = 3.6 mm	
L7, L8	1 turn 1.5 mm copper wire	D = 4 mm	
R1, R2	resistor	10 Ω	SMD 1206
T1	semi rigid coax	25 Ω, length = 160 mm	Micro-Coax UT-090C-25
T2	semi rigid coax	25 Ω, length = 160 mm	Micro-Coax UT-141C-25

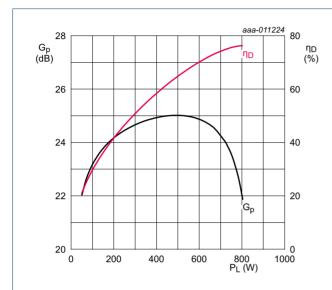
<sup>[1]</sup> American Technical Ceramics type 800B or capacitor of same quality.

<sup>[2]</sup> American Technical Ceramics type 100B or capacitor of same quality.

#### 7.5 Graphical data

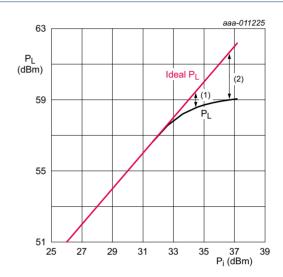
The following figures are measured in a class-AB production test circuit.

#### 7.5.1 1-Tone CW pulsed



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 100 mA; f = 108 MHz;  $t_p$  = 100  $\mu s;$   $\delta$  = 20 %.

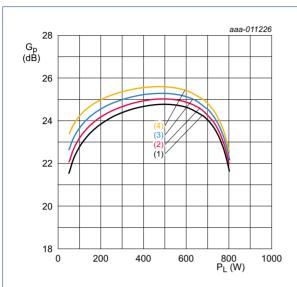
Fig 6. Power gain and drain efficiency as function of output power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 100 mA; f = 108 MHz;  $t_p$  = 100  $\mu s;$   $\delta$  = 20 %.

- (1)  $P_{L(1dB)} = 58.6 \text{ dBm} (720 \text{ W})$
- (2)  $P_{L(3dB)} = 59 \text{ dBm } (800 \text{ W})$

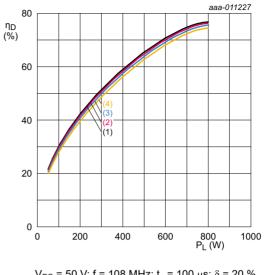
Fig 7. Output power as a function of input power; typical values



 $V_{DS}$  = 50 V; f = 108 MHz;  $t_p$  = 100  $\mu$ s;  $\delta$  = 20 %.

- (1)  $I_{Dq} = 50 \text{ mA}$
- (2)  $I_{Dq} = 100 \text{ mA}$
- (3)  $I_{Dq} = 200 \text{ mA}$
- (4)  $I_{Dq} = 400 \text{ mA}$

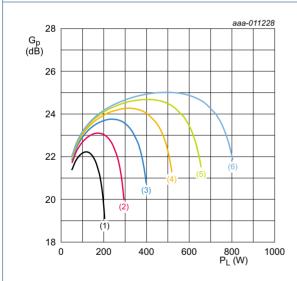
Power gain as a function of output power; typical values



 $V_{DS}$  = 50 V; f = 108 MHz;  $t_p$  = 100  $\mu$ s;  $\delta$  = 20 %.

- (1)  $I_{Dq} = 50 \text{ mA}$
- (2)  $I_{Dq} = 100 \text{ mA}$
- (3)  $I_{Dq} = 200 \text{ mA}$
- (4)  $I_{Dq} = 100 \text{ mA}$

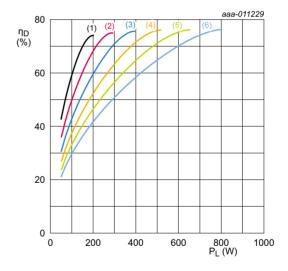
Fig 9. Drain efficiency as a function of output power; typical values



 $I_{Dq}$  = 100 mA; f = 108 MHz;  $t_p$  = 100  $\mu s;$   $\delta$  = 20 %.

- (1)  $V_{DS} = 25 \text{ V}$
- (2)  $V_{DS} = 30 \text{ V}$
- (3)  $V_{DS} = 35 \text{ V}$
- (4)  $V_{DS} = 40 \text{ V}$
- (5)  $V_{DS} = 45 \text{ V}$
- (6)  $V_{DS} = 50 \text{ V}$

Fig 10. Power gain as a function of output power; typical values



 $I_{Dq}$  = 100 mA; f = 108 MHz;  $t_p$  = 100  $\mu s;$   $\delta$  = 20 %.

- (1)  $V_{DS} = 25 \text{ V}$
- (2)  $V_{DS} = 30 \text{ V}$
- (3)  $V_{DS} = 35 \text{ V}$
- (4)  $V_{DS} = 40 \text{ V}$
- (5)  $V_{DS} = 45 \text{ V}$
- (6)  $V_{DS} = 50 \text{ V}$

Fig 11. Drain efficiency as a function of output power; typical values

## 8. Package outline

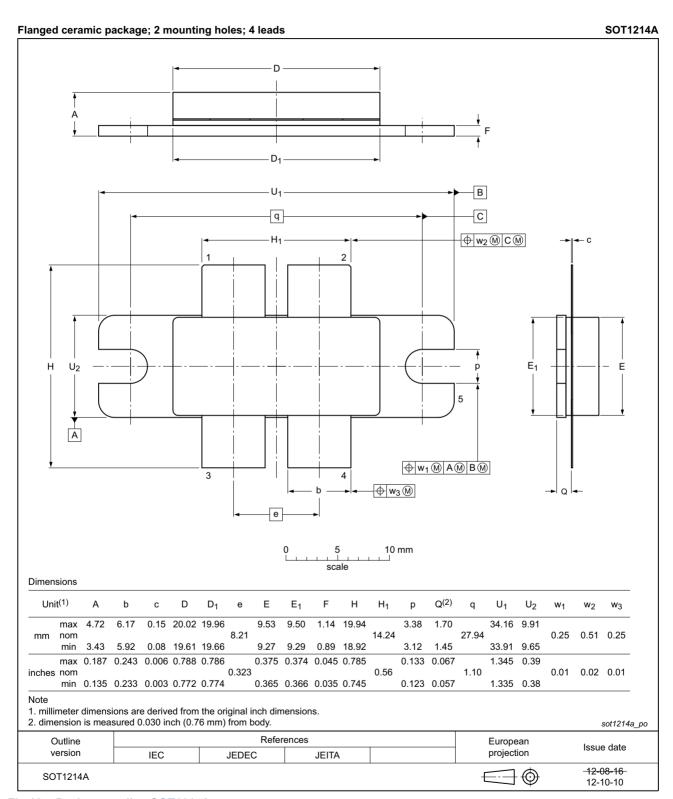


Fig 12. Package outline SOT1214A

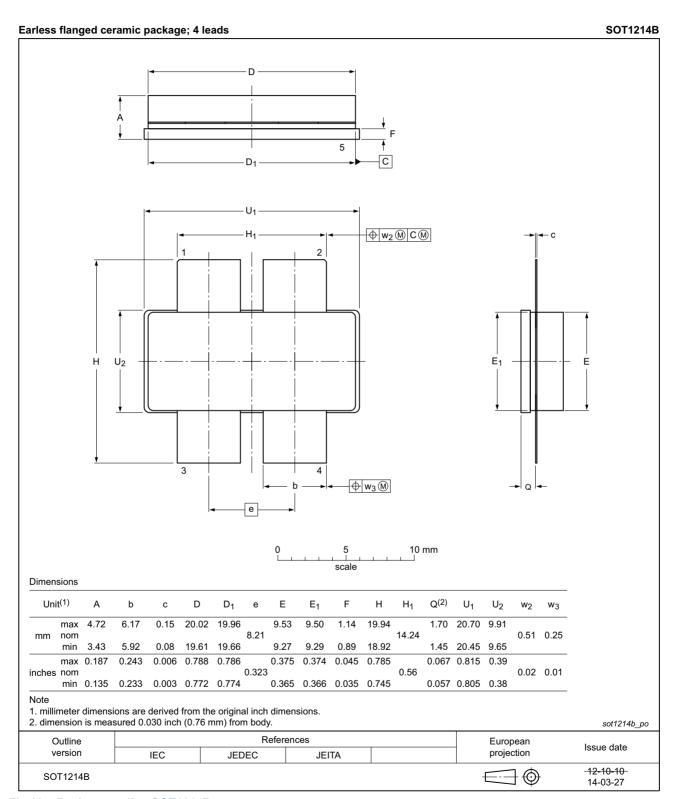


Fig 13. Package outline SOT1214B

## **Handling information**

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

## 10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF184XR_BLF184XRS v.4	20150901	Product data sheet	-	BLF184XR_BLF184XRS v.3
Modifications:	<ul> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLF184XR_BLF184XRS v.3	20140401	Product data sheet	-	BLF184XR_BLF184XRS v.2
BLF184XR_BLF184XRS v.2	20140227	Preliminary data sheet	-	BLF184XR_BLF184XRS v.1
BLF184XR_BLF184XRS v.1	20130506	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [1] Please consult the most recently issued document before initiating or completing a design.
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**Power LDMOS transistor** 

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## **AMPLEON**

## BLF184XR; BLF184XRS

**Power LDMOS transistor** 

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