BLA6G1011-200R; BLA6G1011L(S)-200RG

Power LDMOS transistor

AMPLEON

Rev. 6 — 1 September 2015

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

Table 1. Test information

Typical RF performance at $T_{case} = 25$ °C.

Test signal	f	V _{DS}	P_L	Gp	η_D	t _r	t _f
	(MHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
Typical RF performance in a class-AB production test circuit for SOT502A							
pulsed RF	1030 to 1090	28	200	20	65	10	6
Typical RF performance in a Gullwing application for SOT502C and SOT502D							
pulsed RF	1030 to 1090	28	200	20	65	15	6

1.2 Features and benefits

- Typical pulsed RF performance at frequencies from 1030 MHz to 1090 MHz, a supply voltage of 28 V and an I_{Dq} of 100 mA:
 - ◆ Output power = 200 W
 - Power gain = 20 dB
 - ◆ Efficiency = 65 %
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	S	Simplified outline	Graphic symbol
BLA6G10	11-200R (SOT502A)			
1	drain			
2	gate		5 1 23	1
3	source	[1]	2	2 3 sym112
BLA6G10	11L-200RG (SOT502D)	-		
1	drain			
2	gate		1 3	1 ,
3	source	[1]		2 3 sym112
BLA6G10	11LS-200RG (SOT502C)	1		
1	drain		4	
2	gate		1	1 L
3	source	[1]	2 3	2 3 3 sym112

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package		
	Name	Description	Version	
BLA6G1011-200R	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A	
BLA6G1011L-200RG	-	eared flanged ceramic package; 2 mounting holes; 2 leads	SOT502D	
BLA6G1011LS-200RG	-	earless flanged ceramic package; 2 leads	SOT502C	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I _D	drain current		-	49	Α
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		-	225	°C

BLA6G1011-200R_L-200RG_LS-200RG#6

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Туре	Тур	Unit
() 0)		ouse /	BLA6G1011-200R	0.085	K/W
	from junction to case	$t_p = 50 \mu s;$ δ = 2 %	BLA6G1011L-200RG	0.065	K/W
			BLA6G1011LS-200RG	0.065	K/W

6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.9 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 270 mA	1.4	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 1620 mA	1.7	2.2	2.7	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	4.2	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	40	48	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	420	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 9.45 A	11	18	26	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 9.45 \text{ A}$	0.012	0.07	0.093	Ω
C _{rs}	feedback capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 28 \text{ V};$ f = 1 MHz	-	3	-	pF

Table 7. RF characteristics

Test signal: Pulsed RF; $t_p = 50 \ \mu s$; $\delta = 2 \ \%$; $V_{DS} = 28 \ V$; $I_{Dq} = 100 \ mA$; $T_{case} = 25 \ ^{\circ}C$; unless otherwise specified; in a class-AB production test circuit for straight leads.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
P_L	output power		200	-	-	W
Gp	power gain	P _L = 200 W	18	20	-	dB
RLin	input return loss	P _L = 200 W	-	-10	-8	dB
η_{D}	drain efficiency	P _L = 200 W	58	65	-	%
t _r	rise time	P _L = 200 W	-	10	20	ns
t _f	fall time	P _L = 200 W	-	6	20	ns

6.1 Ruggedness in class-AB operation

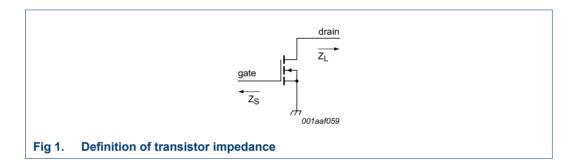
The BLA6G1011-200R, BLA6G1011L-200RG and BLA6G1011LS-200RG are enhanced rugged devices and are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: t_p = 50 μ s; δ = 2 %; V_{DS} = 28 V; I_{Dq} = 100 mA; P_L = 200 W; f = 1030 MHz to 1090 MHz.

7. Application information

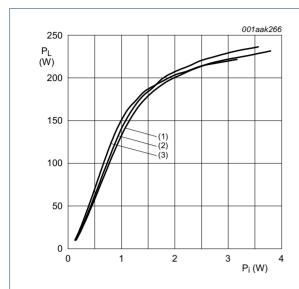
7.1 Impedance information

Table 8. Typical impedance *Typical values unless otherwise specified.*

f	Z _S	Z _L		
(MHz)	(Ω)	(Ω)		
BLA6G1011-200R				
1030	0.57 – j0.94	0.80 - j0.68		
1060	0.70 – j1.13	0.84 - j0.52		
1090	0.80 - j1.53	0.86 - j0.35		
BLA6G1011L-200RG and BLA6	BLA6G1011L-200RG and BLA6G1011LS-200RG			
1030	0.69 – j2.18	0.84 - j0.59		
1060	0.86 – j2.36	0.85 – j0.73		
1090	1.12 – j2.54	0.86 – j0.87		



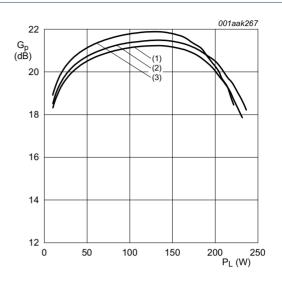
7.2 RF performance



 V_{DS} = 28 V; t_p = 50 μ s; δ = 2 %; I_{Dq} = 100 mA.

- (1) f = 1030 MHz
- (2) f = 1060 MHz
- (3) f = 1090 MHz

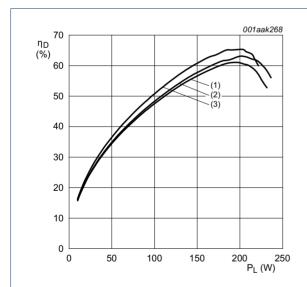
Fig 2. Output power as a function of input power; typical values



 V_{DS} = 28 V; t_p = 50 $\mu s;~\delta$ = 2 %; I_{Dq} = 100 mA.

- (1) f = 1030 MHz
- (2) f = 1060 MHz
- (3) f = 1090 MHz

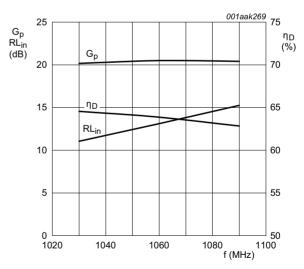
Fig 3. Power gain as a function of output power; typical values



 V_{DS} = 28 V; t_p = 50 $\mu s;~\delta$ = 2 %; I_{Dq} = 100 mA.

- (1) f = 1030 MHz
- (2) f = 1060 MHz
- (3) f = 1090 MHz

Fig 4. Drain efficiency as a function of output power; typical values

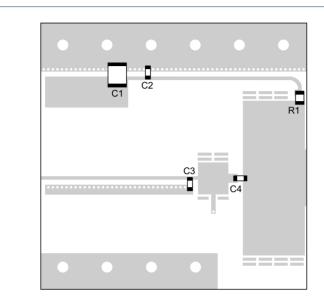


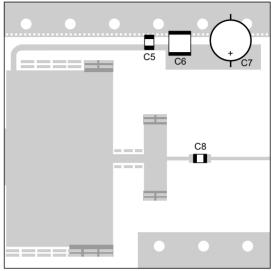
 P_L = 200 W; V_{DS} = 28 V; t_p = 50 $\mu s;~\delta$ = 2 %; I_{Dq} = 100 mA.

Fig 5. Power gain, input return loss and drain efficiency as function of frequency; typical values

7.3 Application circuit

Remark: For BLA6G1011-200R with straight leads





001aak270

See Table 9 for list of components.

Fig 6. Component layout for class-AB application circuit

Table 9. List of components

See Figure 6.

Striplines are on a Rogers Duroid 6006 Printed-Circuit Board (PCB); $\varepsilon_r = 6.15$ F/m; thickness = 0.64 mm

Component	Description	Value	Remarks
C1, C6	multilayer ceramic chip capacitor	10 μF	TDK
C2	multilayer ceramic chip capacitor	68 pF [1]	
C3	multilayer ceramic chip capacitor	1.5 pF [1]	
C4	multilayer ceramic chip capacitor	3.9 pF [1]	
C5, C8	multilayer ceramic chip capacitor	30 pF [2]	
C7	electrolytic capacitor	470 μF; 63 V	
R1	SMD resistor	12 Ω	SMD 1206

- [1] American Technical Ceramics type 100A or capacitor of same quality.
- [2] American Technical Ceramics type 100B or capacitor of same quality.

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

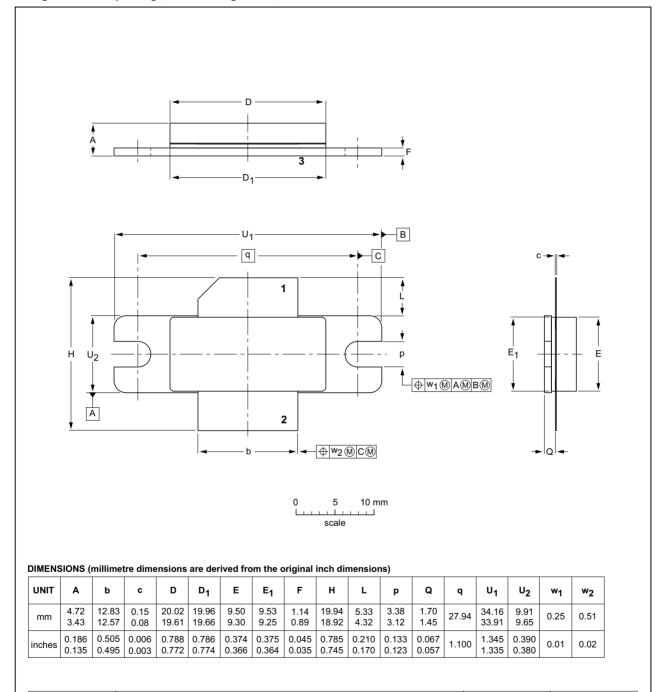


Fig 7. Package outline SOT502A

IEC

OUTLINE

VERSION

SOT502A

JEITA

REFERENCES

JEDEC

ISSUE DATE

03-01-10

12-05-02

EUROPEAN

PROJECTION

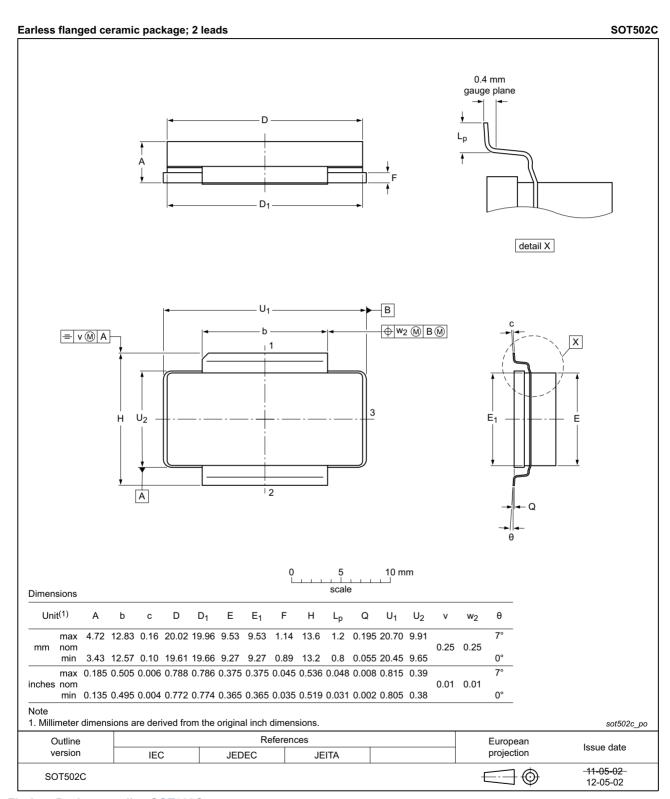


Fig 8. Package outline SOT502C

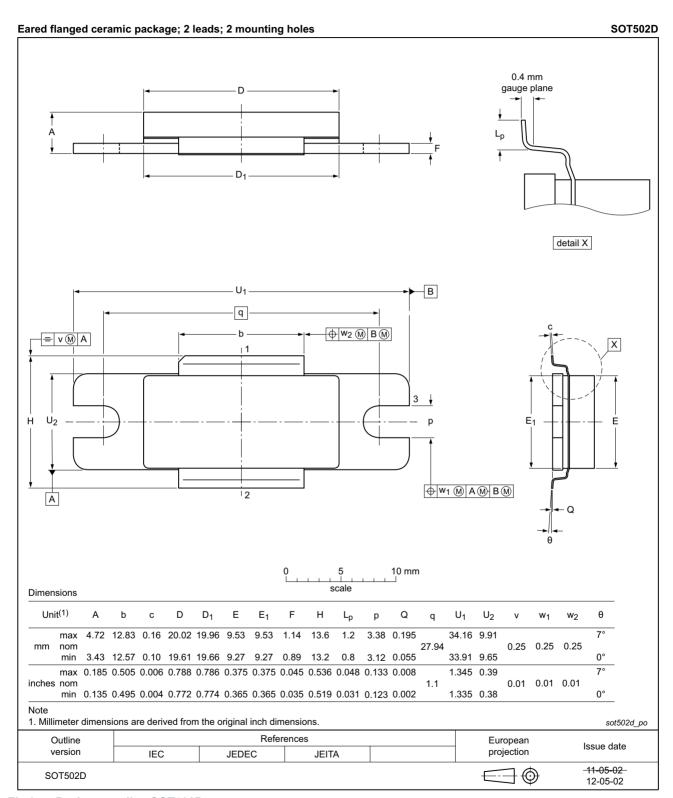


Fig 9. Package outline SOT502D

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA6G1011-200R_L-200RG_LS-200RG#6	20150901	Product data sheet		BLA6G1011-200R v.5
Modifications:	The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.			
	 Legal texts have been adapted to the new company name where appropriate. 			ny name where
BLA6G1011-200R_L-200RG_LS-200RG v.5	20150317	Product data sheet		BLA6G1011-200R v.4
BLA6G1011-200R_L-200RG_LS-200RG v.4	20111109	Product data sheet		BLA6G1011-200R v.3
BLA6G1011-200R v.3	20100714	Product data sheet	-	-

Product data sheet

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Power LDMOS transistor

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