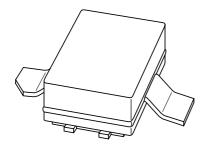
DISCRETE SEMICONDUCTORS

DATA SHEET



BLA1011-2Avionics LDMOS transistor

Product specification Supersedes data of 2002 Oct 02 2003 Nov 19





Avionics LDMOS transistor

BLA1011-2

FEATURES

- · High power gain
- · Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

APPLICATIONS

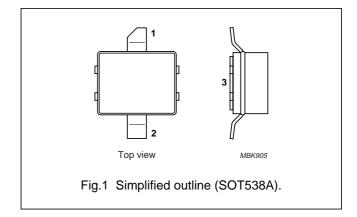
 Avionics applications in the 1030 to 1090 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flangeless package (SOT538A) with a ceramic cap. The common source is connected to the mounting base.

PINNING - SOT538A

PIN	DESCRIPTION		
1	drain		
2	gate		
3	source, connected to mounting base		



QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f	V _{DS}	P _L	G _p
	(MHz)	(V)	(W)	(dB)
Pulsed class-AB; $t_p = 50 \ \mu s; \ \delta = 2\%$	1 1030 to 1090 1		2	>16

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
I TPE NUMBER	NAME	IAME DESCRIPTION VERSION			
BLA1011-2	_	ceramic surface mounted package; 2 leads SOT538			

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		_	75	V
V_{GS}	gate-source voltage		_	±15	V
I _D	drain current (DC)		_	2.2	Α
P _{tot}	total power dissipation	T _h ≤ 25 °C	_	10	W
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	200	°C

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Z _{th(j-mb)}	thermal impedance from junction to mounting base	note 1	1	K/W
R _{th(mb-h)}	thermal resistance from mounting base to heatsink	note 2	6.5	K/W

Notes

- 1. Thermal impedance is determined under RF operating conditions with pulsed bias and T_h = 25 °C.
- 2. Typical value for mounting on PCB with 32 0.4 mm thermal vias with 20 μ m tin plating and thermal compound between PCB and heatsink.

CHARACTERISTICS

 $T_i = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.2 \text{ mA}$	75	_	_	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_{D} = 20 \text{ mA}$	2	_	5	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 26 V	_	_	0.1	mA
I _{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9 \text{ V}; V_{DS} = 10 \text{ V}$	2.8	_	_	Α
I_{GSS}	gate leakage current	$V_{GS} = \pm 15 \text{ V}; V_{DS} = 0$	_	_	40	nA
9fs	forward transconductance	$V_{DS} = 10 \text{ V}; I_D = 0.75 \text{ A}$	_	0.5	_	S
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 0.75 \text{ A}$	_	1.2	_	Ω
C _{is}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 26 \text{ V}; f = 1 \text{ MHz}$	_	11	_	pF
Cos	output capacitance	V _{GS} = 0 V; V _{DS} = 26 V; f = 1 MHz	_	9	_	pF
C _{rs}	feedback capacitance	V _{GS} = 0 V; V _{DS} = 26 V; f = 1 MHz	_	0.5	_	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25$ °C; $R_{th\ mb-h} = 6.5$ K/W unless otherwise specified.

MODE OF OPERATION	f	V _{DS}	I _{DQ}	P _L	G _p	t _r	t _f	PULSE DROOP
	(MHz)	(V)	(mA)	(W)	(dB)	(ns)	(ns)	(dB)
Pulsed class-AB; $t_p = 50 \mu s; \delta = 2\%$	1030 to 1090	36	50	2	>16	<15	<15	<0.5

Ruggedness in class-AB operation

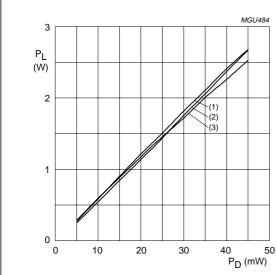
The BLA1011-2 is capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the operating conditions.

Typical impedance values

FREQUENCY (MHz)	Z _S (Ω)	Z _L (Ω)
1030	1.51 + j 11.76	6.9 + j 5
1060	1.51 + j 11.26	6.7 + j 5.9
1090	1.52 + j 10.77	5.1 + j 6.6

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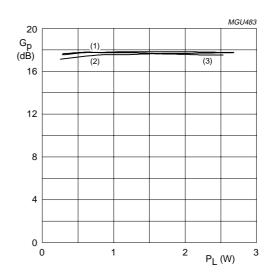


 $T_h = 25 \, ^{\circ}\text{C}; V_{DS} = 36 \, \text{V}; I_{DQ} = 50 \, \text{mA}; \text{ class-AB};$

 $t_p = 50 \ \mu s; \ \delta = 2\%.$

- (1) f = 1060 MHz.
- (2) f = 1030 MHz.
- (3) f = 1090 MHz.

Fig.2 Load power as a function of drive power; typical values.



 T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB;

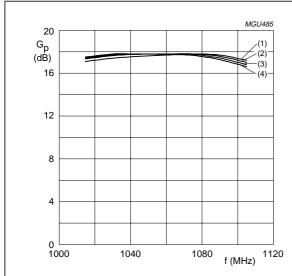
 $t_p = 50 \ \mu s; \ \delta = 2\%.$ (1) $f = 1060 \ MHz.$

(2) f = 1030 MHz.

(3) f = 1090 MHz.

(3) 1 = 1090 MHZ.

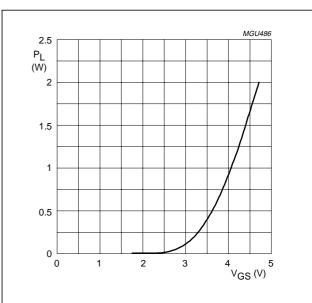
Fig.3 Power gain as a function of load power; typical values.



 T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB; t_p = 50 $\mu s; \, \delta$ = 2%.

- (1) $P_L = 1 W$.
- (3) $P_L = 3 W$.
- (2) $P_L = 2 W$.
- (4) $P_L = 4 W$.

Fig.4 Power gain as a function of frequency; typical values.

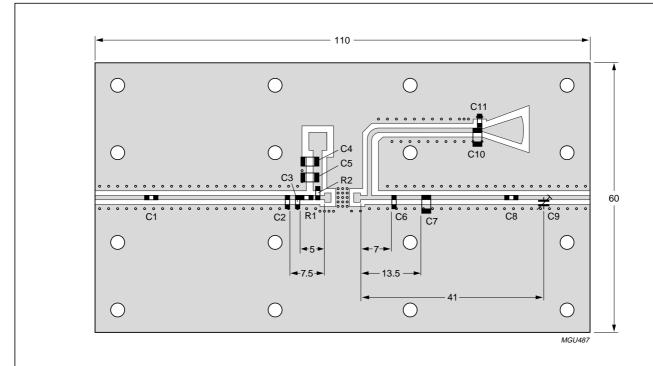


 T_h = 25 °C; V_{DS} = 36 V; I_{DQ} = 50 mA; class-AB; f = 1090 MHz; t_p = 50 $\mu s;$ δ = 2%.

Fig.5 Load power as a function of gate-source voltage; typical values.

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Dimensions in mm.

The components are situated on one side of the Rogers 6006 printed-circuit board (thickness = 0.64 mm; ϵ_r = 6.2), the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through-metallization.

Fig.6 Printed-circuit board for class-AB test circuit.

List of components for class-AB test circuit (see Fig.6)

COMPONENT	DESCRIPTION	VALUE
C1, C8	multilayer ceramic chip capacitor; note 1	56 pF
C2	multilayer ceramic chip capacitor; note 1	7.5 pF
C3	multilayer ceramic chip capacitor; note 1	1.8 pF
C4, C10	multilayer ceramic chip capacitor; note 2	20 nF
C5	multilayer ceramic chip capacitor; note 3	33 pF
C6	multilayer ceramic chip capacitor; note 1	5.6 pF
C7	multilayer ceramic chip capacitor; note 3	6.2 pF
C9	tekelec trimmer; type 37283	0.4 to 2.5 pF
C11	multilayer ceramic chip capacitor; note 1	33 pF
R1	SMD resistor	2.2 Ω (2 in parallel)
R2	SMD resistor	22 Ω

Notes

- 1. American Technical Ceramics type 100A or capacitor of same quality.
- 2. American Technical Ceramics type 200B or capacitor of same quality.
- 3. American Technical Ceramics type 100B or capacitor of same quality.

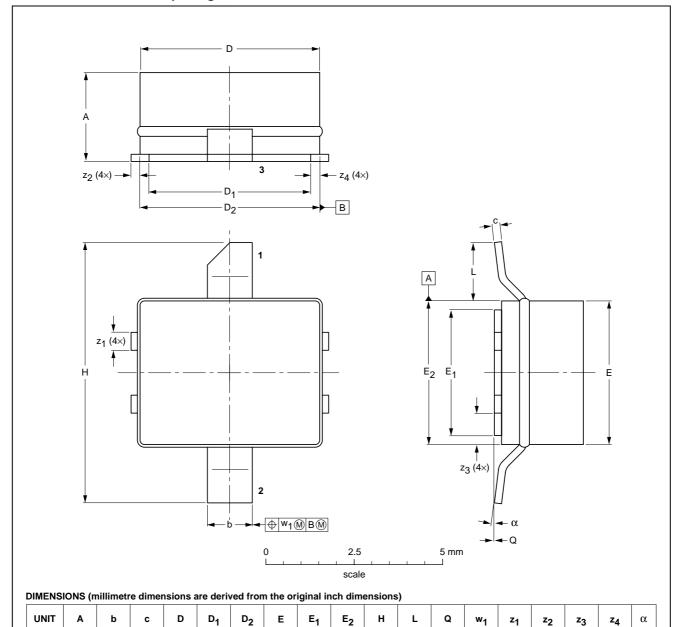
Avionics LDMOS transistor

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PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads

SOT538A



OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT538A						00-03-03 02-08-20

4.14

3.99

0.163

7.24

0.295

2.03

1.27

0.080

0.10

0.00

0.004

0.000

0.25

0.010

0.58

0.43

0.023

0.017

0.25

0.18

0.010

0.97

0.81

0.038

0.51

0.00

0.020

0°

3.63

3.48

0.143

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0.23

0.18

0.009

1.19

0.053

4.65

4.50

0.183

0.177

5.16

5.00

0.203

5.16

5.00

0.203

0.197

3.99

0.163

2.95

2.29

0.116

mm

inches

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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