BL24211

I²C interface 10bit resolution drive for VCM
V1.0

1. Introduction

BL24211 applied to smart of phone the camera. It can control voice coil motor and it can sink 100mA current of 10 bit DAC component.

BL24211 contains power on reset (POR), power down (PD), fast smart mode (FSC). The POR can allow sink pin to output 0V after power on. When user closed the camera, The PD could down power consumption until 1uA. The lens of camera would produce to damping vibration during the auto-focusing. The vibration can affect that the lens move to clear of position. Using FSC mode can reduce damping vibration. FSC make lens to fast of stabilize.

2. Performance

- IC of ID： 00010100.
- Power on reset (POR)
- Power down（PD）
- Direct mode control
- Fast Smart control（FSC）
  - FSC1
  - FSC2
  - FSC3
- 10bit resolution for 100mA current

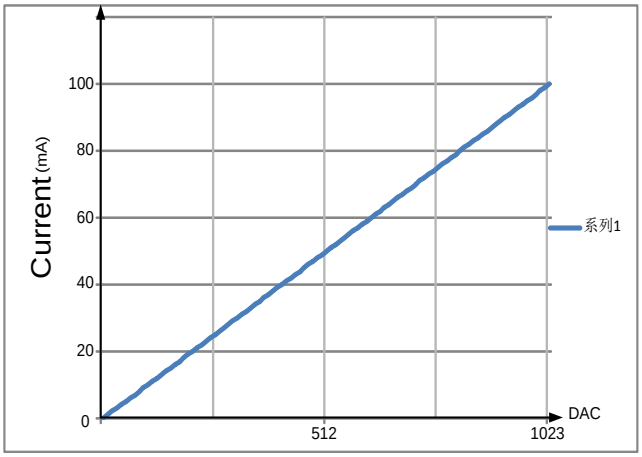


Figure1:10bit & 100mA

- Voltage rang (VDD)
  - Supply to： 2.3V to 4.2V
  - I²C interface： 1.8V or 3.3V
- Interface
  - I²C Serial Communication Rate 400KHZ
  - I²C write address：0x18
  - I²C read address：0x19
- Packaging:
  - WLCSP ， 1.14*0.73m

3. Pin definition

3.1 Pin

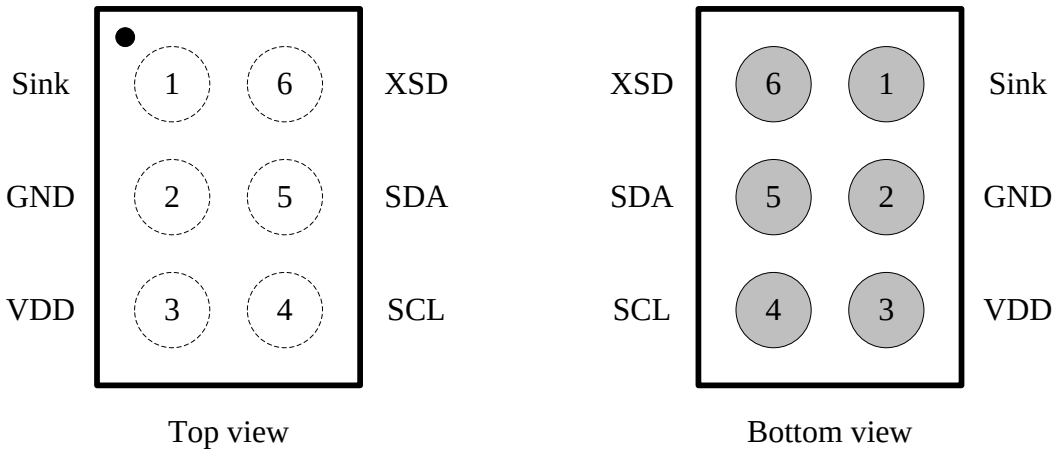


Figure2: Pin Num

3.2 Pin definition

Pin Name	I/O	Description
Sink	O	Output current sink
GND	-	Ground
V_{DD}	-	Power supply
SCL	I	I^2C interface input/output (CLOCK)
SDA	I/O	I^2C interface input (DATA)
XSD（1）	I	Shutdown mode(low active)

Table1: pin definition

Note：（1） XSD

1：normal working， XSD content to high

0：Switch mode, IC cannot work

4. Block map

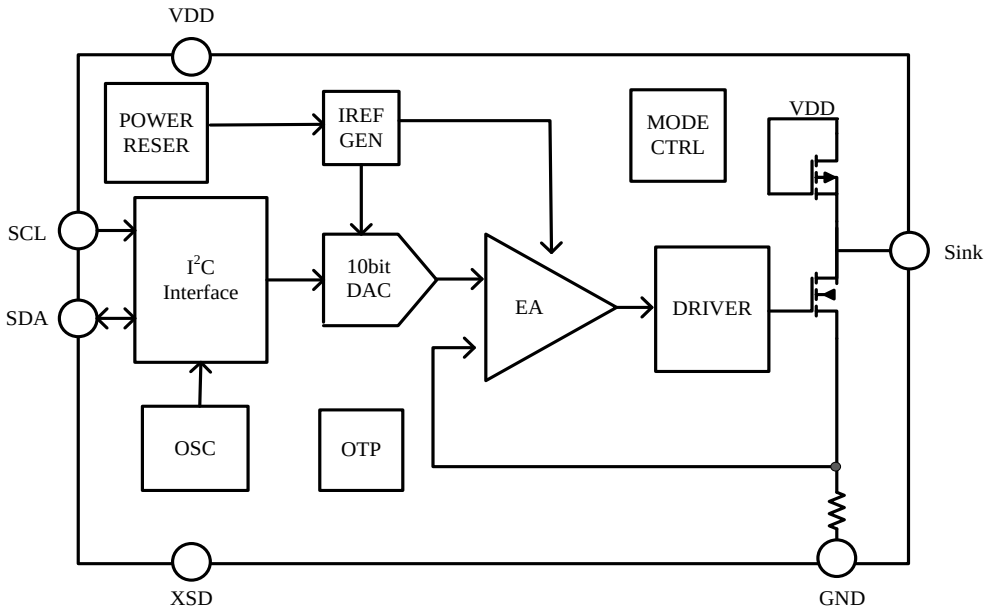


Figure3: Block map

5. Application to scheme

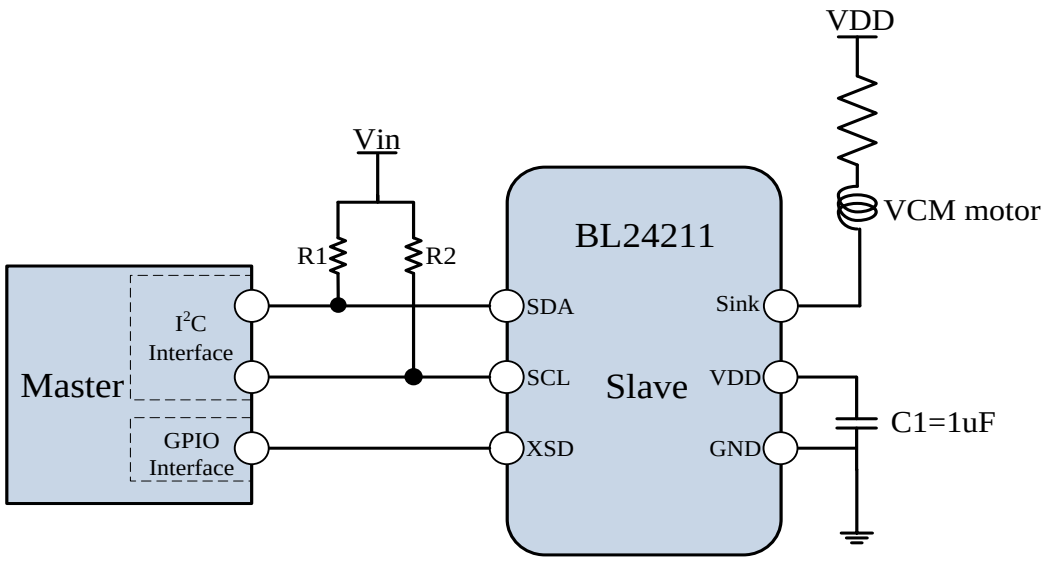


Figure4: Scheme

Explain：（1）BL24211 normal work，XSD pin connect to high of GPIO or VDD to high

（2）R1&R2 value：in Vin2.8V-4.7K Ω，in Vin1.8V-1.3KΩ to 4.7K Ω.

6. Power on sequence

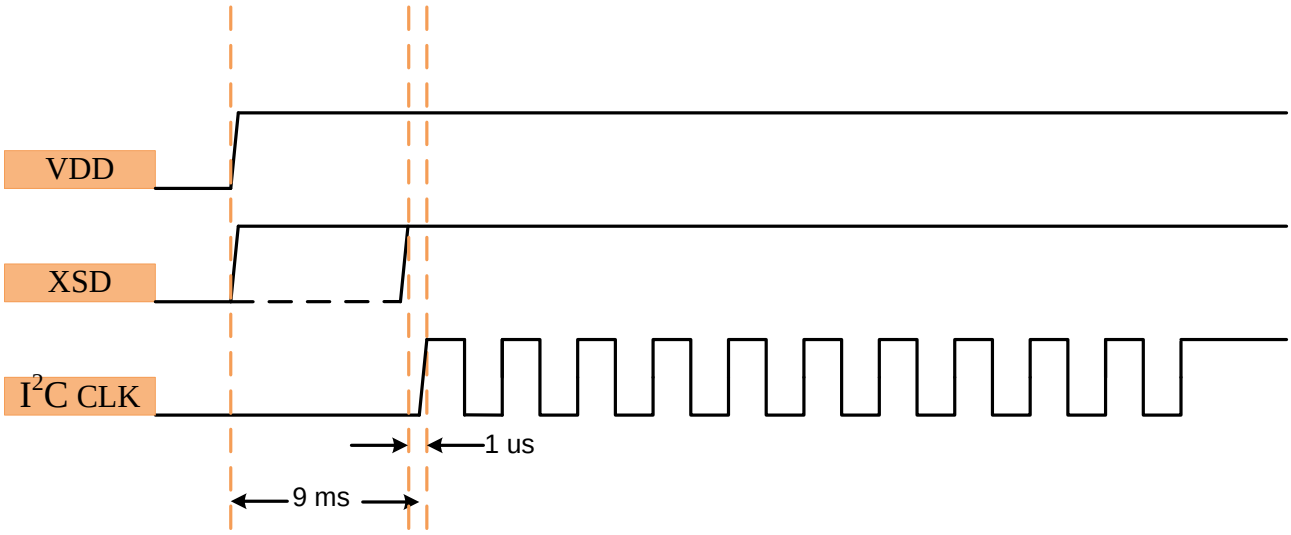


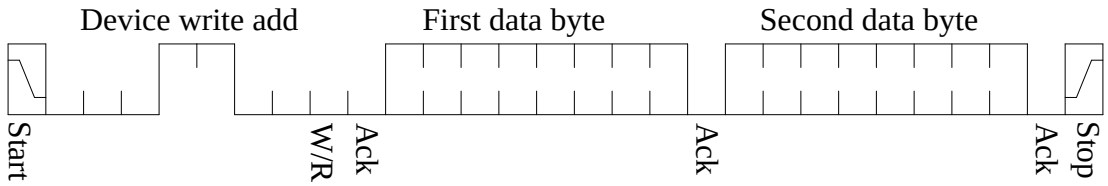
Figure5: Power on time

Note:（1）XSD&VDD together with high or XSD waiting 9ms .

7. The register and application

7.1 I²C communication format:

Write operation



Read operation

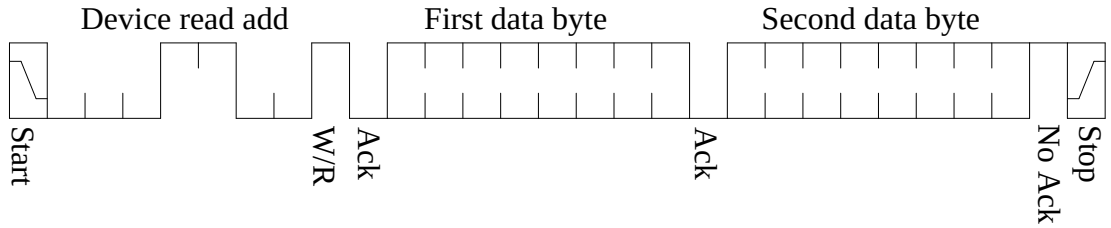


Figure6: I2C Format

7.2 Control table

bit	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
Name	**First byte**								**Second byte**							
DAC Register	PD	Flag	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0
FSC ON	0xEC								0xA3							
Set FSC	0xA1								0	0	0	0	FSC	FSC3	M1	M0
T	0xF2								T5	T4	T3	T2	T1	T0	0	0
FSC OFF	0xDC								0x51							

Table2: Register map

DAC Register	PD	Flag	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	S3	S2	S1	S0

PD bit:

1: Power down

0: Normal work

Flag bit: The bit is reading only. Its value is low of default. When the component working. Flag will keep high until over. In this time, the component cannot response from the master of command.

D<9:0> bit: 10 bit DAC control

Sink current = (D<9:0>/1023) * 100mA

S<3:0> bit: FSC1 control bit. Its value is “0000”. You want to set it. Please refer to table3 and table4

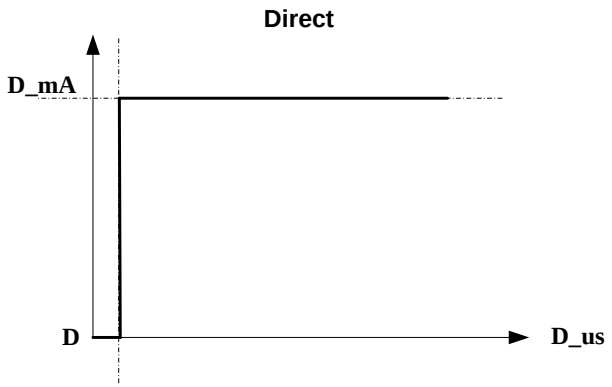


Figure 7

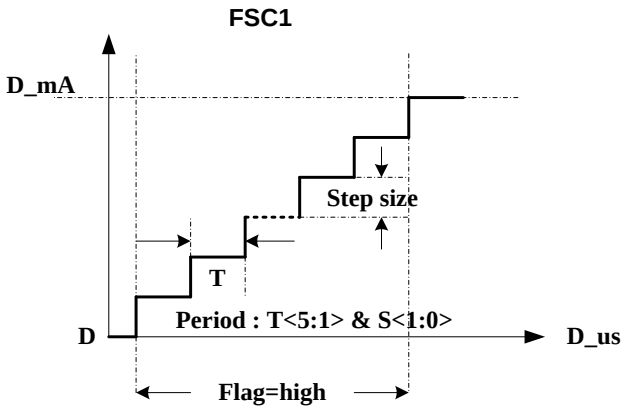


Figure 8

S<3:2>:FSC1 Step size

S[3:2]	Step size
00	0-Direct
01	1
10	2
11	4

Table3

S<1:0>:FSC1 Step time rate

S[1:0]	Step time rate us（1）
00	81
01	162
10	324
11	648

Table4

Note（1）： T5~T1 bit can set other step time rate

7.3 FSC1，FSC2，FSC3 register setting method

FSC ON	0xEC	0xA3

FSC ON：

0xEC and 0xA3 is the head about command, not register. You want to write “Set FSC” before must add to 0xEC and 0xA3 and 0xA1 in command.

.

Set FSC	0xA1	0	0	0	0	FSC	FSC3	M1	M0

FSC: FSC3

- 01 : Set FSC1 mode
- 11 : Set FSC2 mode
- 00 : Set FSC3 mode

M1: M0:

- 00 : double
- 01 : default
- 10 : half
- 11 : quarter

Step time rate is 81us in the FSC1. M1 and M0 can set time for FSC1.

T	0xF2	T5	T4	T3	T2	T1	T0	0	0

T [5:0] = 000000(default)

In FSC1 mode or FSC2 mode, you can set T5~T1 bit

In FSC3 mode, you can set T5~T0 bit

FSC OFF	0xDC	0x51

FSC OFF:

Later the part, 0xDC and 0x51 is the tail about command. You must add to the end in command

You can according to the eighth point that the mode setting process

8. Mode setting process

- –Direct, FSC1/FSC2/FSC3.

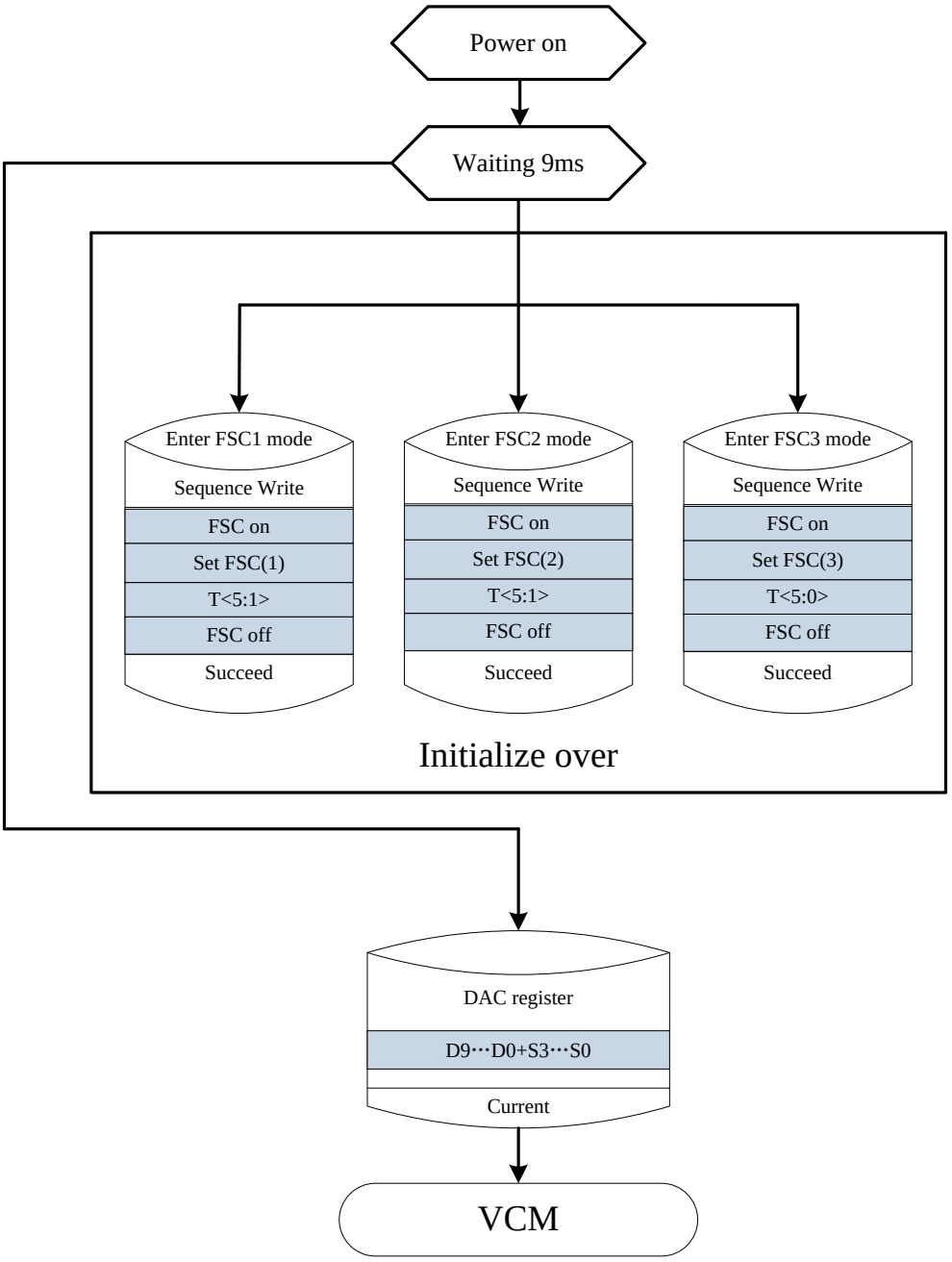


Figure9: Mode set process

- Direct mode is default. The master write D9~D0 to “DAC register” after power on
- When you want to set S3~S0. The component will enter FSC1 mode.

9: FSC data from test

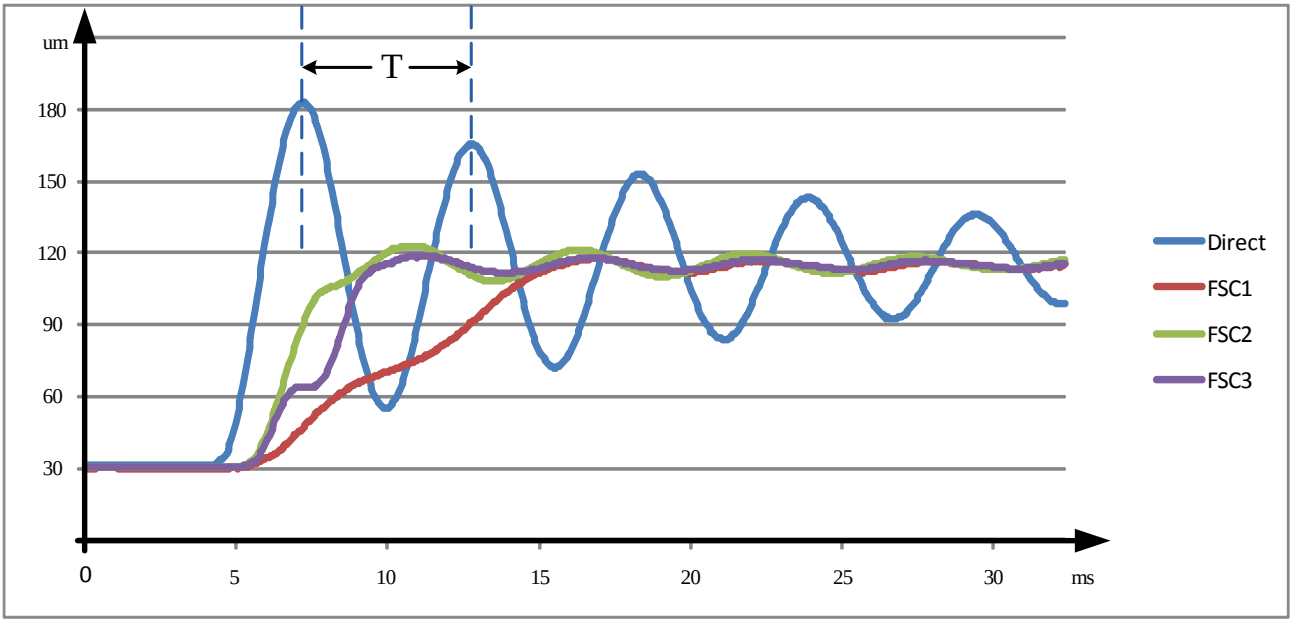


Figure10

- T : VCM Period of oscillation.

10. Recommended Operating condition

名称	参数	Min.	Typ.	Max.	单位
V_{DD}	Power supply voltage	2.3	2.8	3.6	V
V_{in}	Control input voltage	1.8	2.8	V_{DD}	V
SCL	I^2C bus transmission rate			400	kHz

Table6

Absolute maximum ratings: Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (To pr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode when the absolute maximum ratings may be exceeded is anticipated.

11.Electrical Specification

Project	Name	symbol	condition	Min	type	Max	unit
Power	Supply voltage	V_{DD}		2.3		4.2	V
	V_{DD} Pin current	Is	Shutdown mode	-1		1	uA
		I_P	Power down mode	-1		1	uA
		I_Q	Quiescent mode	0.24		0.35	mA
Logic output and input(XSD)	Input current			-1		1	uA
	Low input voltage	V_{IL}				0.54	V
	High input voltage	V_{IH}		1.26			V
Logic output and input (SCL,SDA)	Input current			-1		1	uA
	Low input voltage	V_{IL}				0.54	V
	High input voltage	V_{IH}		1.26			V
	Interference rejection			50			ns
VCM driver	Resolution ratio		97.75uA/LSB		10		bits
	INL	INL		-4		4	LSB
	DNL	DNL		-1		1	LSB
	Zero error code	ZCE	Zero data loaded to DAC	-1		1	mA
	I_{sink} constant voltage		Sink current = 100mA	150			mV
	Max output current	I_{max}			100		mA
	Power on time	T_{PON}			9		ms
Absolute Maximum Ratings	Supply voltage	V_{DD}		-0.3		4.5	V
	Control output voltage	V_{in}		-0.3		V_{DD}+0.3	V
	ESD Human body model	V_{hbm}				2	KV
	ESD Machine model	V_{mm}				200	V
	Work temperature rang	T_{opr}		-35		85	℃
	Junction temperature	T_j				150	℃

Table7: Electricity function

12. I²C Protocol

■ Start and Stop condition

A serial data transfer always begins with a start condition and ends with a stop condition. The SCL and the SDA keep to high. When SDA from high to low change. This is status a start condition, or when the SDA from low to high change. This is status a stop condition. Refer to Figure 11 I2C protocol of start and stop

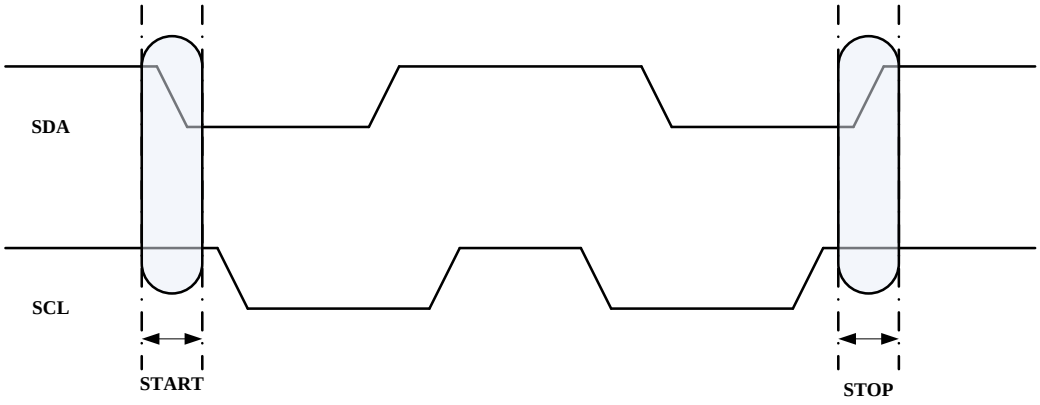


Figure11: I2C protocol of Start and Stop

■ I²C data communication process

The I²C interface initiates a data transfer and generates the clock signal. A serial data transfer always begins with a start condition and ends with a stop condition. The I²C interface is capable of recognizing its own addresses. Data and addresses are transferred as 8-bit bytes, address first. The first bytes following the start condition contain the address. The second bytes and the third bytes is data. A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter. Refer to Figure 12 I2C bus protocol

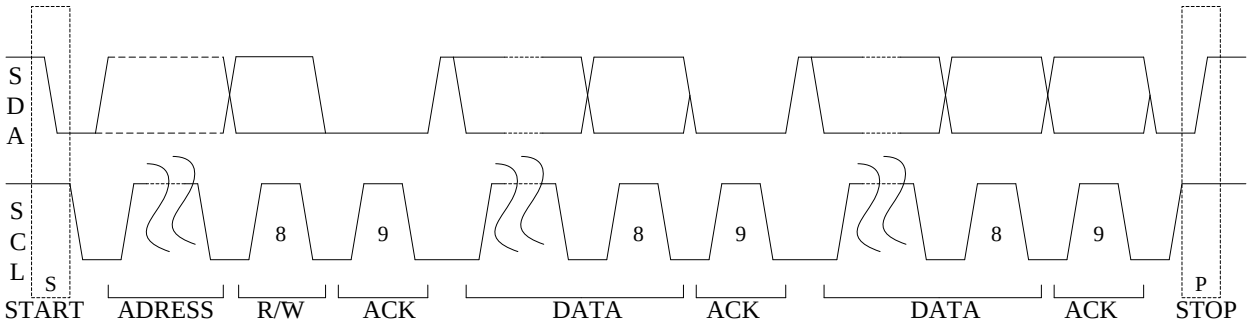


Figure12: I2C bus protocol

■ I2C time

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time after Start,SCL Keep time in the low	$t_{HD;STA}$	0.6	-	us
Low perido of the SCL Clock	t_{LOW}	1.3	-	us
High perido of the SCL Clock	t_{HIGH}	0.6	-	us
Set-up time for a repeated Start condition	$t_{SU;STA}$	-	0.9	us
data hold time	$t_{HD;DAT}$	-	0.9	us
Data Set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1C_b	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1C_b	300	ns
Set-up time for stop condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a stop and start condition	t_{BUF}	1.3	-	us
Capacitive load for each bus line	C_b	-	400	pF
Pulse width of spike suppress	t_{SP}	0	50	ns

Table8: I2C time

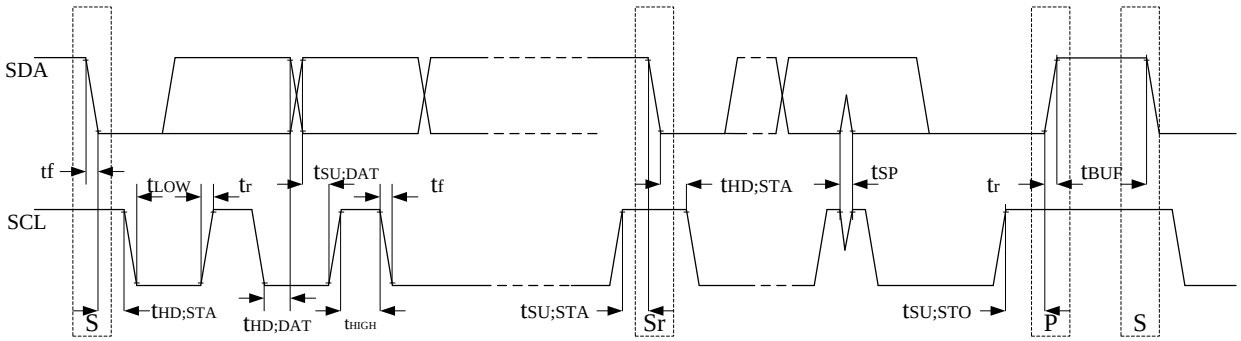


Figure13

13. Package Dimension

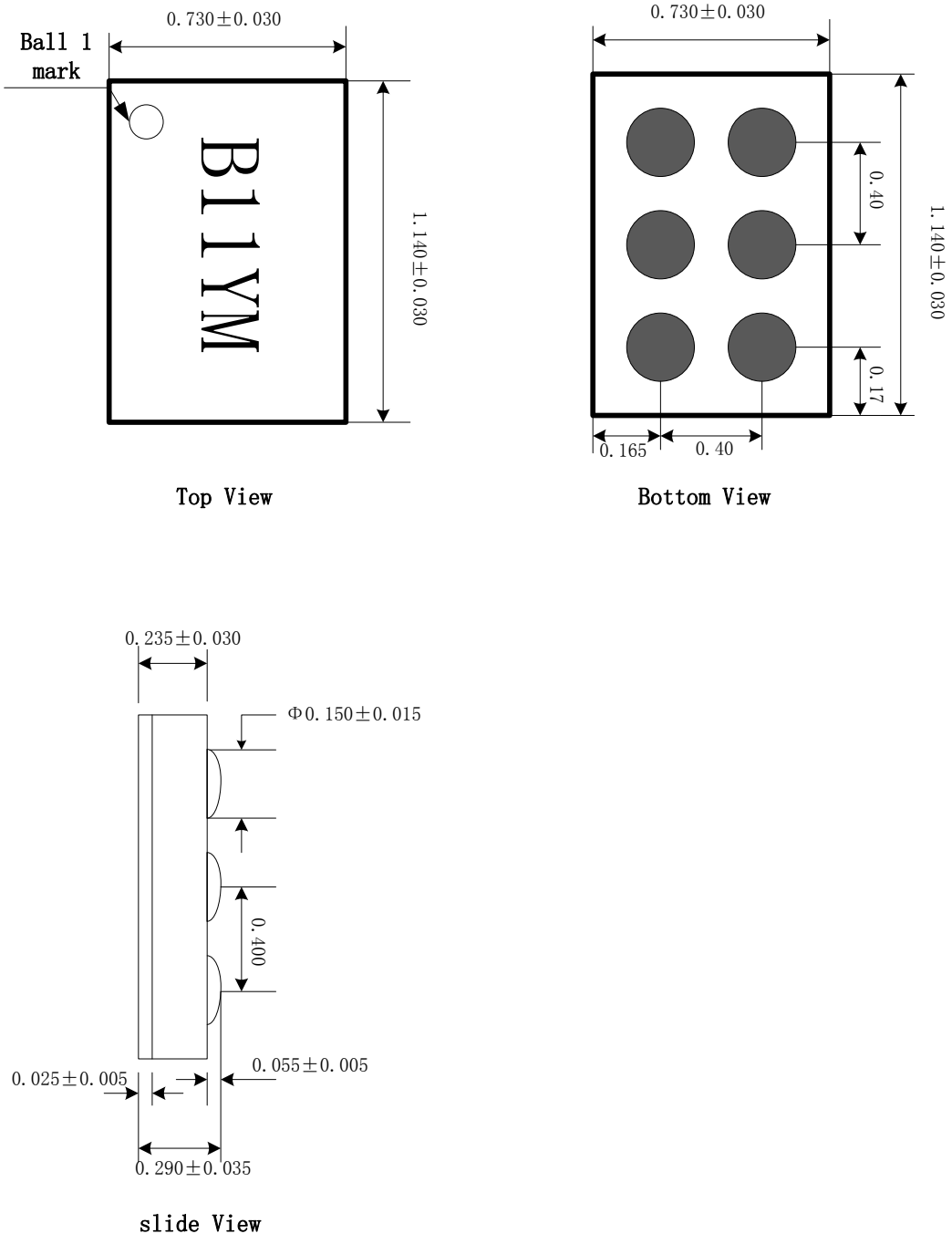


Figure14