BK4813

Analog Two Way Radio IC

Features

- World wide band: 134 ~ 490 MHz
- 12.5/25 kHz channel spacing
- On chip 4 dBm RF PA
- 2.4 V to 3.6 V power supply
- CTCSS tone receiver with up to parallel eight frequency detector
- 23/24 bit programmable DCS code
- Standard DTMF and programmable in-band dual tone
- SELCALL and programmable in-band single tone
- 1.2/2.4 kbps FSK data modem with either F2D or F1W modulation type
- Frequency inversion scrambler
- Voice activated switch (VOX) and time-out timer
- RF Signal strength measurement and signal quality measurement
- TX Audio signal strength indication and RX audio signal strength indication
- 3-wires interface with MCU with maximum 8 Mbps clock rate
- QFN 4x4 24-Pin package

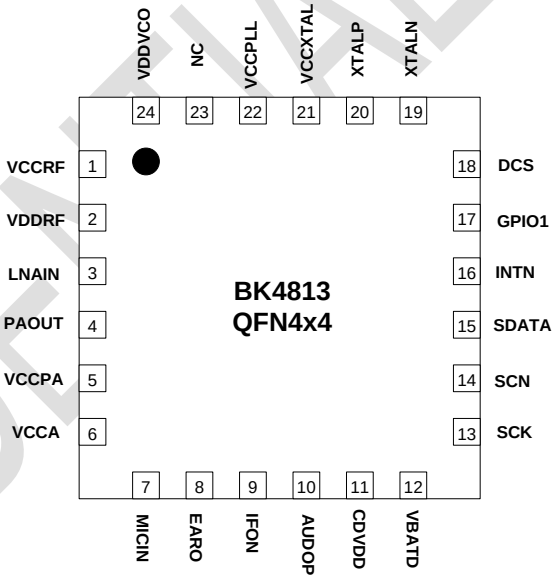
Applications

- Personal Radio Service
- Baby Monitor
- Toys

General Description

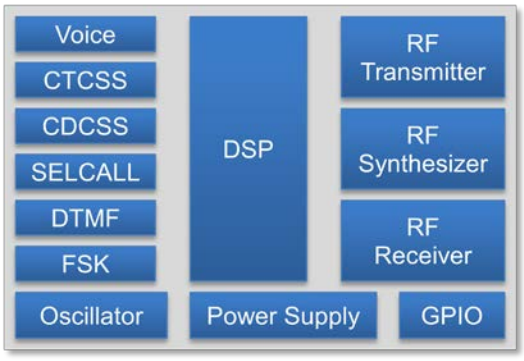
The BK4813 is a half duplex TDD FM transceiver operating from 130 MHz to 490 MHz band for worldwide personal radio. Besides speech communication, the BK4813 on-chip FSK data modem supports F2D and F1W emission to be used in both FRS and DPMR band for text message and GPS information exchange.

The BK4813 is a complete, small form factor solution optimized for low-power, low-cost, and highly integrated mobile and portable consumer electronic devices, requiring only a few external decoupling capacitors and an external inductor for input matching.



QFN 24 Pin Assignments(Top View)

Functional Block Diagram



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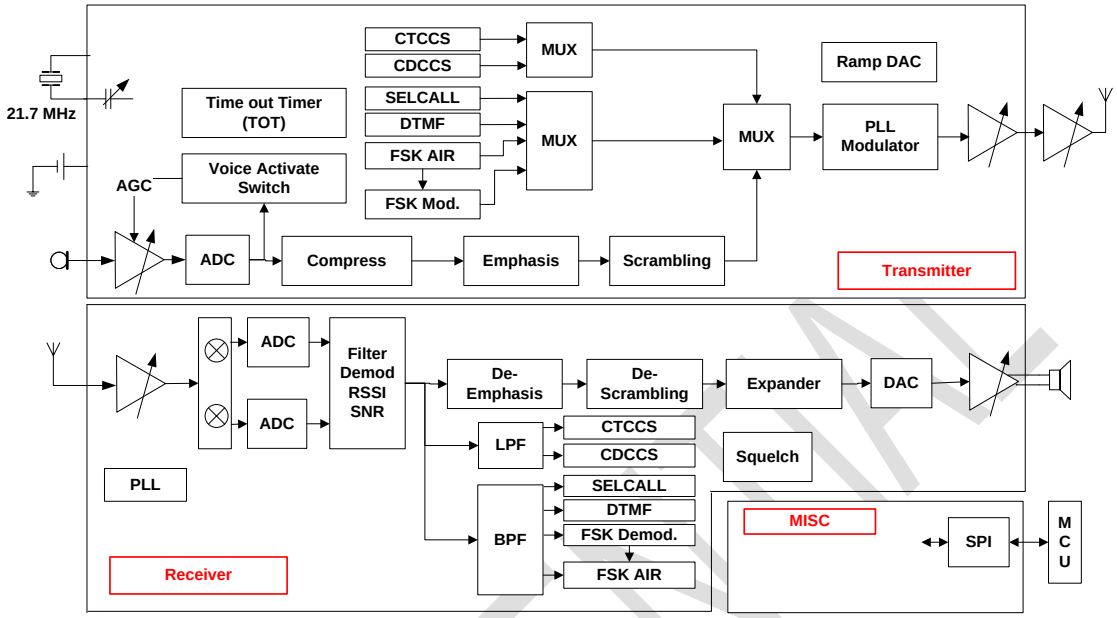

Figure 1. Functional Block Diagram

1.1 Overview

The BK4813 integrates high performance PLL, ADC, DAC, and advanced digital signal processing capability on a single chip. The digital low-IF image rejection architecture enables it to work with a very simple MCU as a two way radio communication system. On-chip flexible and precise continuous and discrete tone generator and detector enable a secure link and digital signaling.

1.2 RF Transceiver

BK4813 includes an integrated RF transceiver which is compliant with the specification most country in the world. The RF transceiver requires the following external components to operate:

1) a 21.7MHz crystal;
2) simple input matching and output matching;
3) several SMD capacitors for decoupling and DC blocking.

1.2.1 FM Receiver

The receiver implements a low-IF image rejection architecture, which is composed with two parts: RF front-end and IF part. The RF front-end comprises a LNA and a quadrature mixer. The IF part comprises a low-pass filter (LPF) for channel filtering, a variable gain amplifier (VGA) and a high precision analog-to-

digital converter(ADC). The block diagram of the FM receiver is shown in Figure 2.

At the RF front-end part, the LNA is a differential low-noise amplifier with single-ended input. The LNA is followed by a quadrature mixer that down-converts the RF signal directly to IF signal. Low-IF image rejection architecture is implemented in order to eliminate the external SAW filters. The value of IF frequency(f_{IF}) can be programmed from 1kHz to 150kHz through 3-wire SPI interface(*REG16*). The RF front-end part can be power up by set *REG7[11]* to 0.

At the IF part, the down-converted in-phase IF signal(IF/I) and quadrature-phase IF signal(IF/Q)are first filtered by the LPF, and then amplified by the VGA. The 3dB bandwidth of the LPF could be set to 100kHz or 200kHz through 3-wire SPI interface(*REG108[7]*).The VGA provides variable gain with 21dB dynamic range, and could be controlled through3-wire SPI interface(*REG108[6:4]*).The Sigma-Delta ADC sample analog IF signal from VGA, and convert it to digital IF signal. Then the digital signal will be send to DSP for second down-conversion and audio processing. The IF part can be power up by set *REG7[10]* to 0.

To avoid serious distortion with high-level input power, AGC function is added to automatically adjust the gain of LNA and the gain of VGA. AGC function can be enabled by set *REG7[6]* and *REG108[15]* to 0.

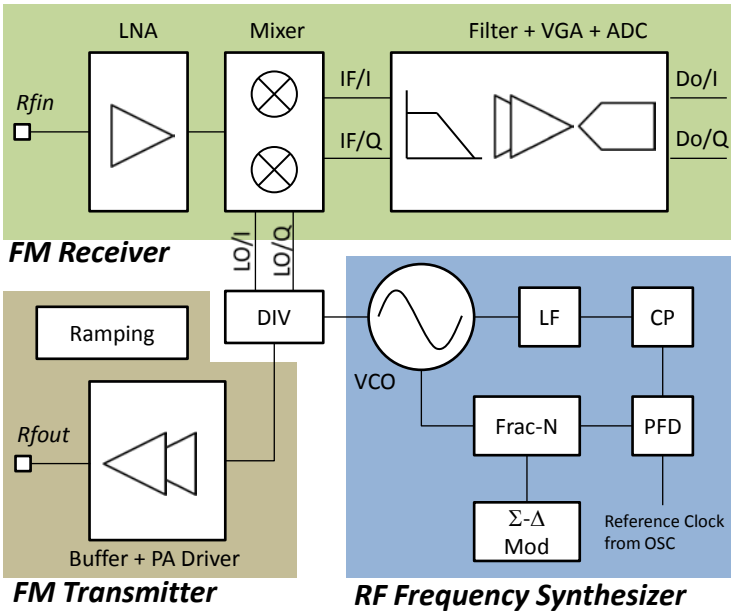

Figure 2. Radio Block Diagram

1.2.2 FM Transmitter

The transmitter is a single-ended amplifier including a buffer, a PA driver and a ramping-control block. The block diagram of the transmitter is shown in Figure 2. Due to FM modulation is of constant envelope, the amplifier works in saturated mode to save current consumption.

A ramping-control block is implemented to avoid unwanted spurious signals when the transmitter is power up. Ramping function can be enabled by set *REG10[8]* to 1. If ramping function is enabled, a ramping table should be filled by writing ramp values into *REG42* in turn. The best ramping curve is raised cosine.

The output power of FM transmitter can be programmed from -60dBm to +7dBm through 3-wire SPI interface(*REG10[7:4]*).

The transmitter can be power up by set *REG7[8]* to 0.

1.2.3 RF Frequency Synthesizer

An RF synthesizer is implemented to generate local oscillator(LO) signals. It includes a voltage controlled oscillator(VCO), a fractional-N divider(frac-N), a phase-frequency detector(PFD), a charge pump(CP) and a loop filter(LF). The RF synthesizer is shared for RX mode and TX mode. The block diagram of the synthesizer is shown in Figure 2.

In RX mode, the RF frequency synthesizer generates unmodulated LO signal. And the unmodulated LO signal is then divided by an integer N_{div} for down-conversion mixer in the FM receiver. In TX mode, FM modulation is realized in the RF frequency synthesizer. Modulated VCO output is divided by an integer N_{div}. The value of N_{div} can be programmed to 8/12/16/20/24 through 3-wire SPI interface(*REG4[15:13]*).

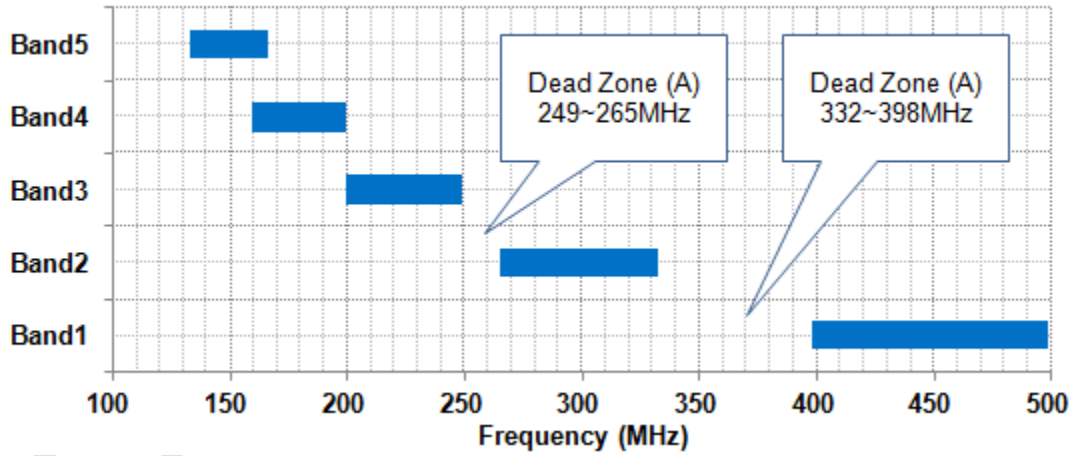

Figure 3. Frequency Cover Range of RF Synthesizer

In RX mode, the locked frequency of the synthesizer is equal to N_{div} x (f_{wanted}-f_{IF}). While in TX mode, the locked frequency of the synthesizer is equal to N_{div} x f_{wanted}.

Channel selection is also implemented by programming the value of fraction-N through 3-wire SPI interface(*REG113/REG114*). On power up or channel reselection, the synthesizer takes less than 0.3msec to settle.

The synthesizer can use external crystals between 21.2MHz and 22.2MHz. For BK4813, the default crystal is 21.7MHz. The frequency tolerance of the crystal should be within ±2.5ppm to keep a reliable communication.

The synthesizer can be power up by set *REG7[12]* to 0.

1.2.4 Input/Output Matching

Since the LNA input and the PA output are of single-ended, external balun is not necessary. Both the input matching and the output matching can be implemented using low-cost discrete inductors and capacitors. The schematic of input/output matching is shown in Figure 4.

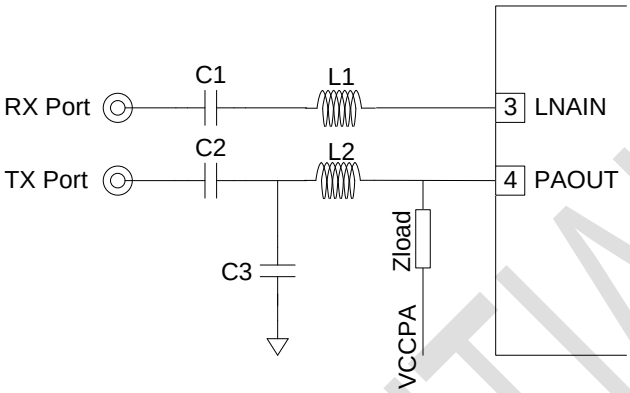

Figure 4. Schematic of Input/Output matching

As for input matching, capacitor C1 is used for DC-blocking. The recommended value of C1 is 100pF. The DC voltage at PIN3 is about 0.47V in RX mode. Inductor L1 is used for impedance transformation. The recommended value of L1 is 47nH for 409.75MHz band, and is 33nH for 446.00625MHz/462.5625MHz band.

As for output matching, capacitor C2 is used for DC-blocking, too. Due to the PA driver in FM transmitter is open-drain, a load device(Zload) should be put between PIN4 and power supply to offer a DC path. The load device(Zload) can be a resistor or a inductor. Inductor L2 and capacitor C3 are used for impedance transformation, and are used as low-pass filter to attenuate harmonics. If an external high-power PA is implemented in the solution, there will be a low-pass network after high-power PA. Then, L2 and C3 can be removed.

1.2.5 Crystal Oscillator

BK4813 integrates a low-power amplitude-regulated 21.7MHz crystal oscillator. The 21.7MHz crystal oscillator not only provides the reference frequency for the RF synthesizer, but also provides clock for digital part. The circuit diagram of the 21.7MHz crystal oscillator is shown in Figure 5.

The 21.7 MHz crystal oscillator is designed for use with an quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal datasheet. Figure 5 on next page shows how the crystal is connected to the 21.7 MHz crystal oscillator. C1 and C2 are ceramic SMD(Surface Mount Device) capacitors connected between each crystal terminal and ground. Cvar is an adjustable capacitor for frequency calibration.

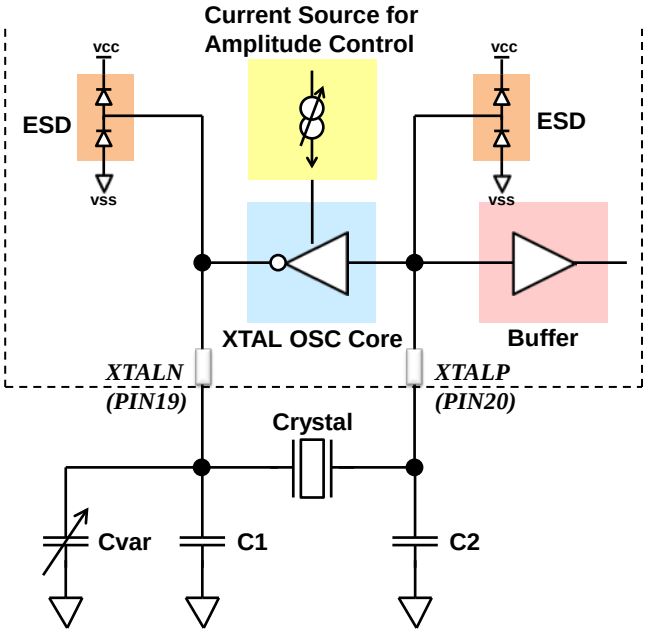

Figure 5. Circuit Diagram of the 21.7MHz Crystal Oscillator

$$C_{load} = \frac{C_1' \times C_2'}{C_1' + C_2'}$$
$$C_1' = C_1 + C_{var} + C_{par}$$
$$C_2' = C_2 + C_{par}$$

in which, Cpar is parasitic capacitance including PCB trace capacitance and pin input capacitance. The value of Cpar is about 1pF.

The 21.7MHz crystal oscillator can be power up by set *REG7[14]* to 0.

1.2.6 On-chip Voltage Regulator Decoupling

BK4813 contains 3 low-dropout regulator(LDO):

1) One LDO for RF part in FM receiver. This LDO needs an external SMD capacitor to reduce noise on power supply for better noise figure. The output voltage of this LDO is about 2.2V, and the typical value of this SMD capacitor is 100nF.
2) One LDO for VCO in RF synthesizer. This LDO needs an external SMD capacitor to reduce noise on power supply for better phase noise performance. The output voltage of this LDO is about 2V, and the value of this SMD capacitor should be no less than 1uF.
3) One LDO for digital part. This LDO needs an external SMD capacitor to reduce spurious signal from digital part. The output voltage of this LDO is about 1.8V, and the value of this SMD capacitor should be no less than 1uF.

The configuration of these 3 LDOs is shown in Figure 6.

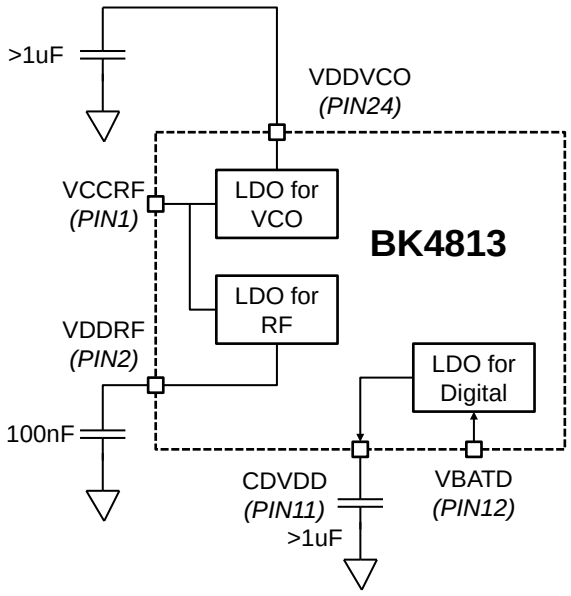

Figure 6. Configuration of Low-dropout Regulators

1.2.7 Power Supply Decoupling

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application.

1.3 TX Baseband

1.3.1 Audio

TX audio path has the following blocks:

1) Digital AGC to automatically adjust microphone gain (REG44, REG45) before ADC;
2) Digital compressor to extent signal dynamic range (REG17);
3) Volume control with 1 dB step from -25 dB to 6 dB (REG18);
4) Optional pre-emphasis filter, 0 dB at 1 kHz and +6 dB per octave (REG18);
5) Audio scrambling with programmable scrambling frequency (REG20);
6) 300 Hz high pass filter to avoid interference to sub-audible signal, which has 30 dB attenuation for frequency below 250 Hz with respect to signal at 1 kHz (REG18);
7) Low pass filter 3 kHz corner for 12.5 kHz/25 kHz channel spacing, the bandwidth is not programmable;
8) Limiter to avoid unwanted out-of-band emission (REG19);
9) Flexible block execution order (REG18).

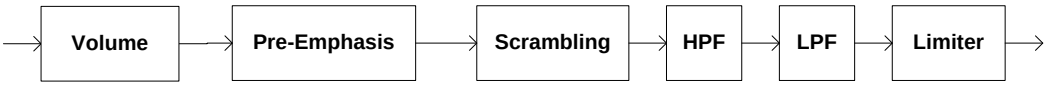

Figure 7. TX Audio Block Diagram

The microphone gain can be control through *REG44* and *REG45*.

When AGC is enabled, the microphone gain is automatically controlled by internal AGC algorithm. At this scenario, the real time microphone gain setting can be read by *REG21[5:0]*. Combined with the real time microphone gain (*REG21 [5:0]*) and the digital detected microphone signal level (*REG21*), the absolute microphone signal level at microphone input can be calculated, but please note the *REG21[15:8]* and *REG21[5:0]* have difference unit.

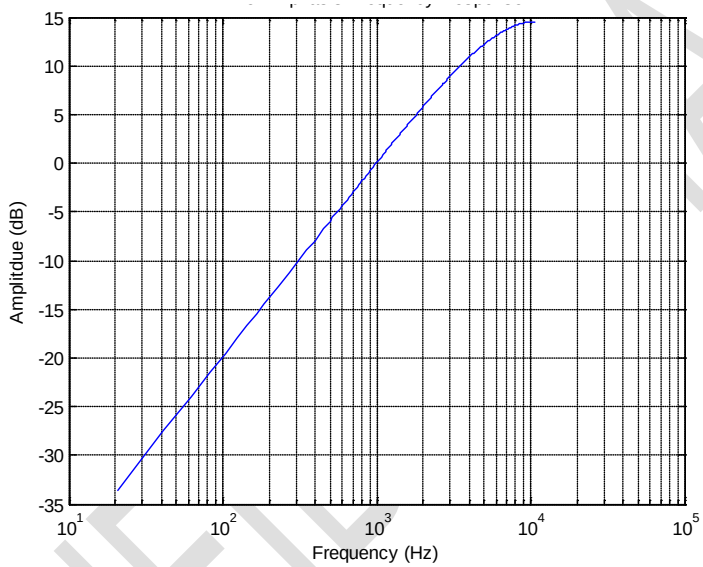

Figure 8. Frequency Response of Pre-emphasis Filter

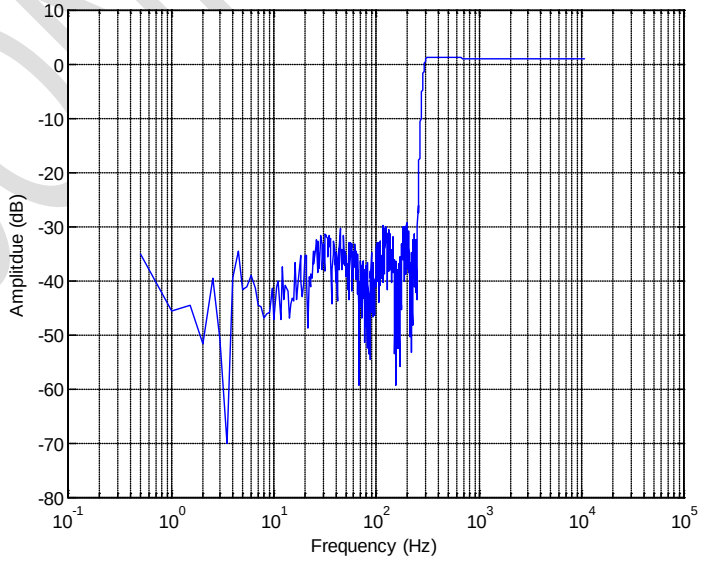

Figure 9. Frequency Response of 300Hz High Pass Filter

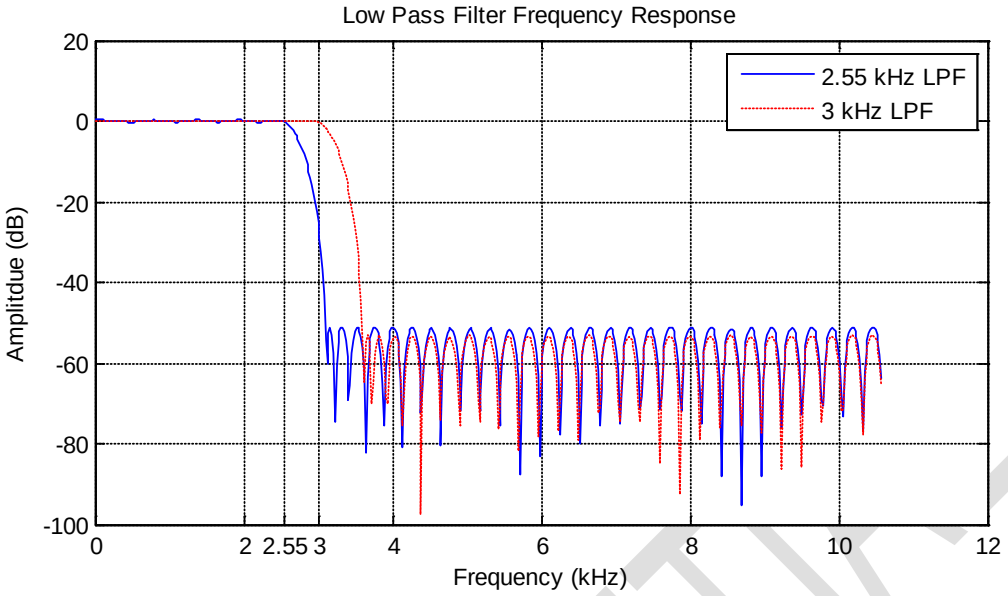

Figure 10. Frequency Response of Low Pass Filter

1.3.2 VOX and TOT

Voice activated switch (VOX) detects the background noise level (REG22[7:0]) and microphone input signal level (REG21[15:8]), when the ratio between the signal level and the background noise level is greater than a programmable threshold (REG23[8:1]) and (REG23 [0] =0) / or (REG23 [0] =1) the signal level is greater than an absolutely threshold (REG23[8:1]), the VOX will output 1 and the VOX interrupt bit will be set (REG116[3]).

VOX works only when receive signal strength (REG68[6:0]) is lower than a programmable threshold (REG67[6:0]).

In TX mode, time-out timer (TOT) detects the VOX output, if it is 0 (no active microphone input signal) for a programmable duration (REG23[14:12]), the TOT interrupt bit will be set (REG116[2]).

User can do its own VOX and TOT control based on the readable microphone signal level (REG21[15:8]) and background noise level (REG22[7:0]).

1.3.3 In-band Signaling

There are three types of in-band signaling: DTMF, SELCALL, and FSK (and FSK_AIR). Together with audio signal, they are total of four kinds of in-band signaling, of which only one can be sent at a time (REG40). The deviation of in-band signaling is programmable (REG40).

1.3.3.1 DTMF

DTMF is a dual tone signaling, it has programmable high band and low band frequency. The high band frequency can be programmable from 1209 Hz to 1633 Hz (REG25). The low band frequency can be programmable from 697

Hz to 941 Hz (REG24). The twist can be programmable from 0 to 15 dB with 1 dB resolution (REG26)). The suggested DTMF tone table is given below.

Table 1. Standard DTMF Table

DTMF Symbol		High Frequency (Hz)			
		1209	1336	1477	1633
Low Frequency (Hz)	697	1	2	3	A
	770	4	5	6	B
	852	7	8	9	C
	941	E	0	F	D

1.3.3.2 FSK

FSK is a high data rate signaling, which supports 1200 bps data mode at 12.5 kHz channel spacing and 2400 bps data mode at 25 kHz channel spacing. The frame structure of the data package is given below.

Pre-amble	Sync Word	Addr	Type	Size	CRC A	Payload	CRCB
16 bit	16 bit	Byte0	Byte1	Byte2	Byte3	0-127 Word	2/4 Byte

Figure 11. Frame Structure of Data Mode

User can write head field including Address/Type/Size/CRCA and the corresponding payload (REG28, REG29, REG30), and it will automatically calculate the CRC and packetize the data. Optional scrambling can be added to Address and subsequent bytes, and the scrambling seed is programmable (REG32).

Data receiver will automatically finish synchronization and data extraction that Address/Type/Size/CRCA and Payload can be read out through MCU interface.

The final over the air data package type can be setting with Type byte.

1) Type 0: Only head, no payload
2) Type 1: Head with payload
3) Type 2: Head with FEC encoded payload
4) Type 3: Head with FEC and interleaved encoded payload
5) Type 4: Free format that no automatic CRC insertion, CRCA is a user writable byte

The payload write is through an 8 words (1 word = 2 bytes) FIFO, if the word number in FIFO is shorter than a threshold that a write operation requires, it will give an interrupt to MCU that MCU must refill the FIFO (REG31).

Note: if use type 3, the number of payload is restricted. The allowed payload number is either odd number less than 8 or even number greater than 9. Payload number 8 and 9 is not allowed for type 3.

The FSK packet can be transmitted either directly through FM modulation (FSK AIR) for DPMR band or with a MSK modulated sub-carrier (FSK modem) then to FM modulation for FRS band.

1.3.3.3 SELCALL

SELCALL is a single tone signaling, the frequency can be programmable from 400 Hz to 3000 Hz (REG34). To get high sensitivity the suggested tone frequency (EIA frequency group) is given below.

Table 2. EIA single tone frequency setting

Tone Number	0	1	2	3	4	5	6	7
Tone Frequency (Hz)	600	741	882	1023	1164	1305	1446	1587
Tone Number	8	9	A	B	C	D	E	F
Tone Frequency (Hz)	1728	1869	2151	2435	2010	2295	495	No Tone

1.3.4 Sub-audible Signaling

Sub-audible signaling includes both CTCSS and CDCSS. For CTCSS, the frequency is programmable with 18 bit resolution, and it can be set to have a 0/120/180 degree phase shift. For CDCSS, it supports both standard CDCSS code with programmable 9 bit raw code and user programmable 23/24 bits CDCSS code, and the transmitted CDCSS code can be inversed.

The CDCSS mode is set by REG38 [15:13]. The CDCSS mode and CDCSS code register are shared by both TX and RX.

Table 3. Reference CTCSS Frequency

Standard CTCSS Tone						
Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
67.0	**85.4**	**103.5**	**127.3**	**156.7**	**192.8**	**241.8**
71.9	**88.5**	**107.2**	**131.8**	**162.2**	**203.5**	**250.3**
74.4	**91.5**	**110.9**	**136.5**	**167.9**	**210.7**	
77.0	**94.8**	**114.8**	**141.3**	**173.8**	**218.1**	
79.7	**97.4**	**118.8**	**146.2**	**179.9**	**225.7**	
82.5	**100.0**	**123.0**	**151.4**	**186.2**	**233.6**	
Non-Standard CTCSS Tone						
Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
62.5	**69.3**	**183.5**	**196.6**	**206.5**		
64.7	**159.8**	**189.9**	**199.5**	**229.1**		

Table 4. Reference CDCSS Raw 9 bit Octal Word

023 025 026 031 032 036 043 047
051 053 054 065 071 072 073 074
114 115 116 122 125 131 132 134
143 145 152 155 156 162 165 172
174 205 212 223 225 226 243 244
245 246 251 252 255 261 263 265
266 271 274 306 311 315 325 331
332 343 346 351 356 364 365 371
411 412 413 423 431 432 445 446
452 454 455 462 464 465 466 503
506 516 523 526 532 546 565 606
612 624 627 631 632 654 662 664
703 712 723 731 732 734 743 754

1.4 RX Baseband

The RX baseband output is the FM demodulator output, whose amplitude can be scaled (REG66), and subsequent filter coefficient is selected according to the in-band signal type (REG66) and sub-audible signal type (REG66).

1.4.1 Audio

Audio path has blocks below.

1) De-emphasis filter, 0 dB at 1 kHz and -6 dB per octave (REG72);
2) Audio de-scrambling with programmable scrambling frequency (REG74);
3) Low pass filter with 2.55 kHz corner for 12.5 kHz channel spacing and 3.1 kHz corner for 25 kHz channel spacing (REG72);
4) 45 dB volume control range with 3 dB per step (REG73);
5) Hard mute or soft mute control based on receive signal quality (REG73);
6) Flexible block execution order (REG72);
7) Expander to extent signal dynamic range (REG17).

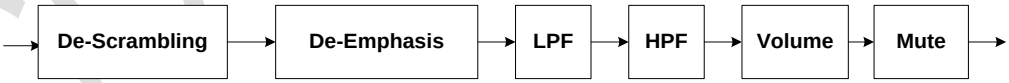

Figure 12. TX Audio Block Diagram

The RX signal strength before volume control module can be read out through REG74.

1.4.2 In-band Signaling

1.4.2.1 DTMF

DTMF decoder can detect up to 16 DTMF symbols simultaneously (REG78). High band tone frequency and low band tone frequency of each symbol can be programmed individually (REG77). When the decoder finds a symbol

match, it will set corresponding bit and the found symbol address (REG78), and an interrupt will be issued.

User can trade off detection sensitivity with response time by selection different match condition and their detection margin (REG75, REG76).

There are two symbol match conditions; the first (match condition 1) is the tone frequency variance less than a programmable margin DTMF_MARGIN2, and the second (match condition 2) is the tone frequency stay inside a deviation (DTMF_MARGIN1) from reference frequency for a programmable duration (DTMF_MARGIN3). User can enable either one of them or both of them for DTMF symbol match. SELCALL and CTCSS have the same match algorithm.

1.4.2.2 FSK

In FSK AIR mode, the slicer output of FM demodulator will be FSK symbol. In FSK mode, the FM demodulator output is taken as a sub-carrier, and will be demodulated with a FSK demodulator.

FSK receiver will search the sync word to establish synchronization with FSK transmitter. When it is synchronized and CRCA check is passed, a FSK head received interrupt (REG116) will be issued and it will continue to receive the payload. The payload data will be written to an 8 words FIFO, and when the data word number in FIFO is greater than a threshold that the FIFO needs to read out, it will issue an interrupt (REG116) and MCU should read out all data bytes in FIFO immediately (REG82, REG83). After all payload of one packet is received, the CRCB check result will be set (REG83) and a receive-finished interrupt will be issued to MCU that MCU should check this bit to know whether the read out payload is valid or invalid that should be discarded.

Note: With free format type (type 4), the “ FSK head received interrupt” will be given out immediately when it found the sync word , thus, this interrupt is earlier than that in other mode.

1.4.2.3 SELCALL

SELCALL decoder can detect up to 16 SELCALL symbols simultaneously (REG87). Frequency of each symbol can be programmed individually (REG86). When the decoder find a symbol match, it will set corresponding bit and the found symbol address (REG87), and an interrupt will be issued.

User can trade off detection sensitivity with response time by selection different match condition and their detection margin (REG84, REG85).

There is an optional high pass filter to filter out signal below 400 Hz (REG87), and user can bypass this filter to receive SELCALL symbol with frequency below 400 Hz.

1.4.3 Sub-audible Signaling

CTCSS decoder can detect up to 8 CTCSS symbols simultaneously (REG92). Frequency of each symbol can be programmed individually (REG91). When the decoder find a symbol match, it will set corresponding bit and the found symbol address (REG92), and an interrupt will be issued.

User can trade off CTCSS detection sensitivity with response time by selection different match condition and their detection margin (REG89, REG90). For example, setting REG89 [15:4] to 0xFF8 can improve the sensitivity and stability, at the cost of much longer response time. In practical use, initiallyuser can set the REG89 [15:4] small to improve the response time, and after the CTCSS is found, user can change it to be larger to avoid link lose. It applies same for the REG90 where user can set the margin smaller initially and set them larger after the tone is found.

CTCSS decoder has an optional high pass filter to filter out DC signal (REG92), which can be used to get better RF frequency offset and low frequency noise immunity.

The CTCSS can detect 120/180 degree phase shift (REG93).

CDCSS decoder uses the same setting as CDCSS encoder, and has also an optional DC block filter (REG94). It can recognize the CDCSS code is exactly same or inversed (REG93).

CTCSS and CDCSS receiver can works simultaneously by set both REG94 [11] =1 and REG94 [10] = 1.

1.5 SPI Interface

The BK4813 has one SPI hardware integrate inside chip with 3-wires. These 3 wires are SCK(PIN13), $\overline{\text{SCN}}$(PIN14), SDATA(PIN15) for data exchange. SCK and $\overline{\text{SCN}}$ are input pins, while SDATA is bi-direction pin.

BK4813 always latch data at the SCK rising edge and output its data at SCK falling edge.

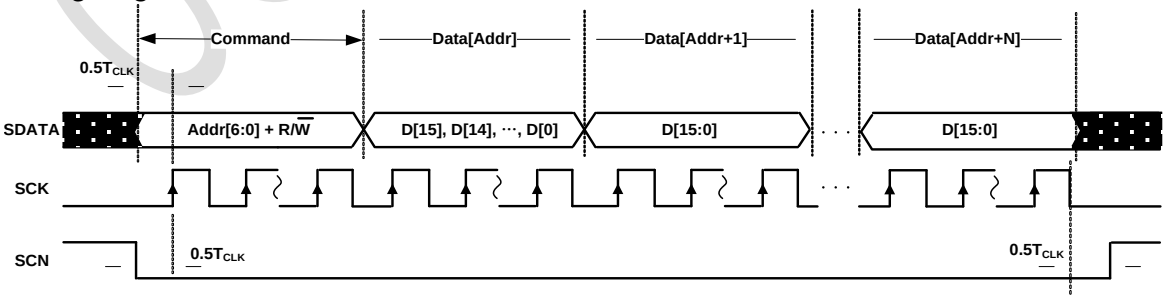

Figure 13. Three-wires Interface Timing

1.6 Power Management

Table 5. Power Control for Different Operational States

Blocks	Control Register	TX	RX	Idle
AGC	REG7[6]	1	0	1
TX Audio	REG7[7]	0	1	1
TX RF	REG7[8]	0	1	1
RX Audio	REG7[9]	1	0	1
RX IF	REG7[10]	1	0	1
RX RF	REG7[11]]	1	0	1
RF Synthesizer	REG7[12]	0	0	1
Central Bias	REG7[13]	0	0	1
Crystal Oscillator	REG7[14]	0	0	1
Digital LDO	REG7[15]	1	1	0
PA Ramping Up	REG43[15]	1	0	0
PA Ramping Down	REG43[14]	0	1	1
Digital State	REG112[14]	1	0	X
Digital Power Up	REG112[15]	1	1	0
Current		33 mA	56 mA	8 uA

When switching from TX or RX mode to idle mode, register should be update in order of REG7, REG43, and REG112. When back from idle to active mode, register should be update in order of REG7, REG2, REG3, REG4 , REG5, REG6, REG43, REG112, where REG2 to REG6 must be re-filled here as their content is lost at idle mode. Please refer to the application note for detailed operation.

2 Electrical Specifications

2.1 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which BK4813 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect BK4813's reliability. Table 6 specifies the absolute maximum ratings for BK4813.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	-0.3	—	+3.6	V
I/O pin voltage	V_{IO}	-0.3	—	V_{DD}+0.3	V
Storage Temperature	T_S	–20	25	85	°C

2.2 Recommended Operating Conditions

The operating conditions are the physical parameters that BK4813 can operate within. The operating conditions for BK4813 are defined in Table 7.

Table 7. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	2.6	—	3.6	V
Operating Temperature	T_O	–10	25	60	°C

Notes:
All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD}=3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.
For QFN4x4 24pin package, VDD range is 2.6-3.6V.
The range of operating temperature mainly depends on the specification of the crystal. The frequency tolerance of the crystal should be within +/-2.5ppm during all operating conditions.

2.3 Power Consumption Specification

Table 8. Power Consumption Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current (RX Mode)	I_{RX}	REG7=0x81BF REG112=0xA000	—	56	58	mA
Supply Current (TX Mode)	I_{TX}	REG7=0x8E7F REG112=0xE000	—	33	36	mA
Power Down Current	I_{PD}	REG7=0x7FFF REG112[15]=0	—	8	12	μA

2.4 Receiver Characteristics

Table 9. Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Frequency	F_{OP}	1	134	—	249	MHz
		2	265	—	332	
		3	398	—	498	
Sensitivity	RXSENS	4, 8	-125	-124	-123	dBm
Adjacent Channel Selectivity	ACS	5	61	62	64	dB
Blocking	BLK	6	81	82	86	dB
Inter-modulation	IMD	7	60	61	62	dB
Audio						
Earpiece output level	EARO	8		146		mVrms
SINAD	ASNR	8,9		50		dB
Amplitude response	ARES		-3		3	dB
Audio noise floor	ANF			-81		dBm
CTCSS						
CTCSS sensitivity	CTSEN			-123		dBm
CTCSS response time	CTRES		75		125	ms
Frequency range	SAF		62.5		250.3	Hz
DCS						
CDCSS sensitivity	CDSEN			-122		
CDCSS response time	CDRES			171		ms
Code length	CLEN		23		24	Bit
Bit rate	BRATE			134.4		Hz
SELCALL						
SELCALL sensitivity	SELSEN			-122		dBm
SELCALL response time	SELRES			30		ms
Frequency range	IBSF		400		3000	Hz
DTMF						
DTMF sensitivity	DTSEN			-122		dBm
DTMF response time	DTRES			20		ms
High band frequency range	FH		1209		1633	Hz
Low band frequency range	FL		697		941	Hz
FSK data modem (F3E and F2D)						
FSK sensitivity (1E-3 BER)	FSKSEN			-122		dBm
FSK Best PER (32 bytes payload)	FSKBEST			0.1	1	%
Over the air data rate	BAUD		1200		2400	bps

Test Condition:
1. Band 3, Band 4, Band 5
2. Band 2
3. Band 1
4. 12 dB SINAD
5. 1st adjacent channel (±12.5kHz)
6. Frequency offset > 1MHz
7. According to TIA standard (TIA-603-B)
8. 1kHz tone, 1.5kHz deviation
9. -50dBm input power

2.5 Transmitter Characteristics

Table 10. Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Frequency	F_{OP}	1	134	—	249	MHz
		2	265	—	332	
		3	398	—	498	
Output Power	POUT	4	-60	-1	7	dBm
Adjacent Channel Power Rejection	ACPR			67		dBc
Microphone Sensitivity	MICSENS	5		8		mV
SINAD	TSINAD	6		47		dB

Test Condition:
1. Band 3, Band 4, Band 5
2. Band 2
3. Band 1
4. Depend on output matching and register settings
5. 1.5kHz deviation
6. At sensitivity level

2.6 SPI Control Interface Characteristics

Table 11. SPI Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	8	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, SEN to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
SEN Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, SEN, SDIO, Rise/Fall Time	t_R , t_F		—	—	10	ns

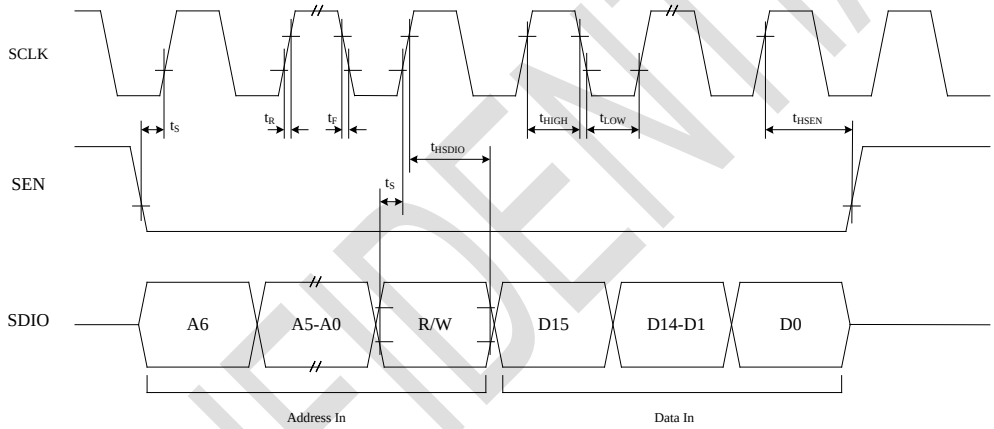

Figure 14. 3-Wire Control Interface Write Timing Diagram

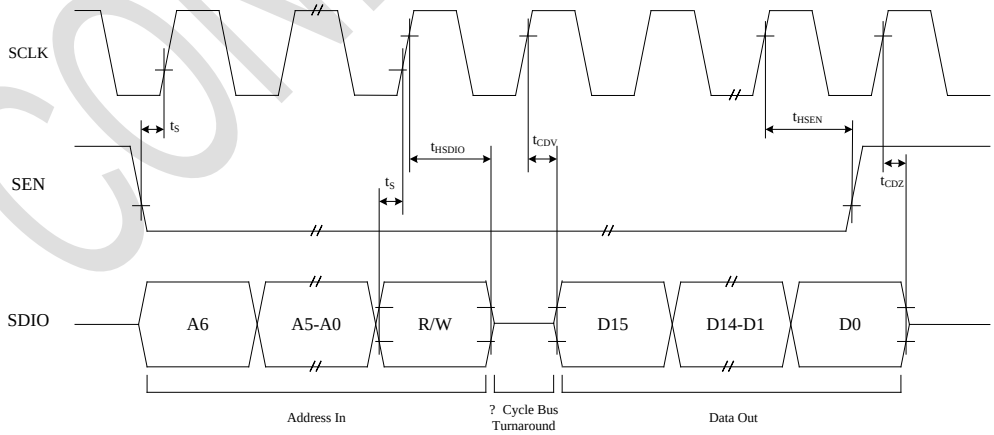

Figure 15. 3-Wire Control Interface Read Timing Diagram

3 Register Definition

Table 12. Interface Register Definition

(Default setting for 446.00625 MHz and 8 mV microphone sensitivity, IF = 137 kHz)

Address（DEC）	R/W	Default Setting	Sub-module	Description	
0	R	0xAx00	Common	15:08	Device ID, read only
1	W/R	0x00000	Common	15	Channel spacing. 0: 12.5 kHz 1: 25 kHz
				14	FSK_AIR data rate. 0:1.2kbps 1:2.4kbps
02 – 15	RF/Analog				
2	W	0x003C			
3	W	0x003C			
4	W	0x1000		15:13	VCO to LO divider number 0: 8; 1: 12; 2: 16; 3: 20; 4: 24
5	W	0x1C80			
6	W	0xFFC0			
7	W	0x7FFF (Idle) 0x8E7C (TX) 0x81BC (RX)		15	TX/RX digital low-drop regulator. 1: Enable0: Disable
				14	TX/RX crystal oscillator. 1: Power down0: Power up
				13	TX/RX central bias. 1: Power down 0: Power up
				12	TX/RX RF synthesizer. 1: Power down 0: Power up
				11	RX RF. 1: Power down 0: Power up
				10	RX IF. 1: Power down 0: Power up
				9	RX Audio. 1: Power down 0: Power up
				8	TX RF. 1: Power down 0: Power up
				7	TX Audio. 1: Power down 0: Power up
				6	RX AGC. 1: Power down 0: Power up
8	W	0xDDDD			
9	W	0x0F00			
10	W	0x2468			
11	W	0x0008			
12	W	0x080F			
13	W	0xC0D5			
16	W/R	0x54DF		Used for IF = 137 kHz at narrow band mode	

17 – 63			Digital Transmitter		
17	W/R	0x1800	AUDIO	11	0: Enable digital compander 1: Disable digital compander
18	W/R	0xC160	AUDIO	15	Bypass Pre-emphasis (1)
				14	Bypass Frequency Inversion (1)
				11:09	PRE-emphasis/scrambling/ HPF order 3'd0: PRE->SCR->HPF 3'd1: PRE->HPF->SCR 3'd2: SCR->PRE->HPF 3'd3: SCR->HPF->PRE 3'd4: HPF->PRE->SCR 3'd5: HPF->SCR->PRE Others are not valid inputs
				8	Soft Limiter (1) or hard limiter (0)
				6:02	Volume: -25 dB (0) to 6 dB (31)
19	W/R	0x0870	AUDIO	12:0	Audio limiter value. -val ~ +val
20	W/R	0x0000	AUDIO	15:13	Inversion frequency 3'd0: 2700, 3'd1: 2800 3'd2: 2900, 3'd3: 3000 3'd4: 3100, 3'd5: 3200 3'd6: 3300, 3'd7: 3400
21	R(15:8) W/R(7:0)	0x0020	AUDIO	15:08	Microphone signal level, scalar
				5:0	Real time microphone gain, same unit as REG44[5:0]
22	W/R(15:8) R(7:0)	0x3200	VOX	15	Enable VOX (1)
				14	Background noise detection speed 0: 1/65536, 1: 1/32768
				13	Speech detection speed 0: 1/512, 1: 1/256
				12:10	THD 3'd0: 2, 3'd1: 3, 3'd2: 4 3'd3: 6, 3'd4: 8, 3'd5: 12 3'd6: 16, 3'd7: 24
				9:08	VOX_DELAY 2'd0:100 ms, 2'd1:200 ms 2'd2:400 ms, 2'd3:800 ms
				7:00	Back ground noise level BACK_LEVEL

23	W/R	0x2000	TOT	15	Enable TOT 1: Enable 0: Disable
				14:12	TOT time out timer (Unit: second) 3'd0: 0.5, 3'd1: 1, 3'd2: 2 3'd3: 4, 3'd4: 8, 3'd5: 16 3'd6: 32, 3'd7: 64
				8:1	Microphone Energy Threshold for VOX
				0	1:vox_thrd_0(sin wave can trigger)
24	W/R	0x086C	DTMF	15:00	Low frequency; Unit: 0.3234 Hz
25	W/R	0x13BA	DTMF	15:00	High frequency; Unit: 0.3234 Hz
26	W/R	0x0000	DTMF	15:12	Twist (Unit: dB); 4'd0: 0, 4'd1: 1 1 dB per step, 4'd15: 15
27	W/R	0x0000	FSK	15:00	Sync Word (Only be used in free frame type)
28	W/R	0x0000	FSK	15:08	Address
				7:00	Type 8'd0: Type 0, 8'd1: Type 1 8'd2: Type 2, 8'd3: Type 3 8'd4: Type 4 Others are not valid
29	W/R	0x0000	FSK	15:09	Size
				7:00	CRCA (Only be used in free frame type)
30	W	0x0000	FSK	15:00	Payload FIFO
31	W/R	0x8000	FSK	15:13	FIFO Threshold
				12	FIFO needs refilling 1: Needs refilling 0: No needs refilling
				3:00	Total words in write FIFO
32	WR	0x0000	FSK	15	Enable scrambling (1)
				14:08	Scrambling initial value
34	W/R	0x0740	SELCALL	15:00	SELCALL tone Frequency Unit: 0.3234 Hz

36	W/R	0x8000	CTCSS	15	CTCSS mode 0: Use internal frequency table (Not supported yet) 1: Frequency set by user
				14:13	The high 2 bits of CTCSS frequency
				1:00	Phase change (Unit: Degree) 0: 0, 1: 120, 2: 180. 3: 240
37	W/R	0x04D5	CTCSS	15:00	The low 16 bits of CTCSS frequency Unit: 0.0808 Hz
38	W/R	0xE000	CDCSS	15	0: CDCSS is set by register 1: CDCSS symbol generated internal by low 9 bit of CDCSS code Shared by both TX and RX
				14	0: CDCSS not inversed 1: CDCSS inversed Shared by both TX and RX
				13	0: 23 bits CDCSS 1: 24 bits CDCSS Shared by both TX and RX
				11:00	High 12 bits of CDCSS if it has 24 bits or high 11 bits of CDCSS if it has 23 bits Shared by both TX and RX
39	W/R	0x0013	CDCSS	11:00	Low 12 bits of CDCSS Shared by both TX and RX
40	W/R	0x9020	Transmitter	15	1: In-band signal exists 0: No in-band signal
				14:13	In-band signal type 00: Audio 01: DTMF 10: FSK 11: SELCALL
				12:09	In-band signal deviation 0.2~1.9 (8 is about 1.5 kHz deviation by default)
				7	1: Sub-audible signal exists 0: No sub-audible
				6	Sub-audible signal type 0: CTCSS 1: CDCSS
				5:02	Sub-audible signal deviation 0.08~ 0.38 (8 is about 300 Hz deviation by default)
				1:00	TX deviation expand factor 0:1 1:1.5 2:2 3:2.5

42	W/R	0x0000	RAMP	15:10	RAMP memory address
				9:00	RAMP data
				RAMP TABLE, should be written to address from 0 to 63, with linear up data	
43	W/R	0x403F (Idle) 0x803F (TX) 0x403F (RX)	RAMP	15	RAMP up enable 1: Enable 0: Disable
				14	RAMP down enable 1: Enable 0: Disable
				5:03	RAMP up speed 3'd0: 0.16 ms 3'd1: 0.16*2 ms … 3'd6: 0.16*2^6 ms 3'd7: 0.16*2^7 ms
				2:00	RAMP down speed, same as ramp up speed definition
44	W/R	0xAA3C	AUD_AGC	15	Audio AGC Enable (1) When AGC is enabled, gain will be set internally by AGC, else can be set through bit 5:0 of this register
				14:12	AGC target level 0: -3, 1: -6, 2: -9, 3: -12, 4: -15, 5: -18, 6: -21 (Default), 7: -24 dBFS
				11	AGC gain change mode 1 (Default): fast mode 0: slow mode
				5:00	Audio AGC set value, 0.5 db each step
				Microphone AGC	

45	W/R	0x1F00	AUD_AGC	15:14	Time taken by the output signal decrease to the target level when the input signal is greater than the target level + HYS 0: 12.5 ms, 1: 25 ms, 2: 50ms (Default), 3: 100 ms (Step Mode 0) 0: 1.25 ms, 1: 2.5 ms, 2: 5 ms (Default), 3: 10 ms (Step Mode 1)
				13:12	Time taken by the output signal increase to the target level when the input signal is smaller than the target level 0: 250, 1: 500 (Default), 2: 1000, 3: 2000 (Unit: ms, Step Mode 0) 0: 5, 1: 10 (Default), 2: 20 , 3: 40 (Unit: ms, Step Mode 1)
				11:06	Maximum value of AGC gain, 0..63, Default is 63
				5:00	Minimum value of AGC gain, 0..63, Default is 32
64 – 111			Digital Receiver		
64	W/R	0x0000			
65	W/R	0x0000		15:14	CS Filter Configuration: 2'b11 Narrow Band, 2'b10 Wide Band, 2'b0x Auto Selection

66	W/R	0xD083	FM_DEM	15:14	Demodulator output amplitude 12.5 kHz space: 0: 1/2, 1: 1, 2: 2, 3: 4 25 kHz space: 0: 1/4, 1: 1/2, 2: 1, 3: 2
				12	Parallel Audio enable
				11	Parallel DTMF enable
				10	Parallel FSK enable (can't be set to 1 with FSK air enable at the same time)
				9	Parallel SELCALL enable
				8	Parallel FSK air enable (can't be set to 1 with FSK enable at the same time)
				7	1: Enable in-band signal receive 0: Disable in-band signal receive
				4	1: Enable sub-audible signal receive 0: Disable sub-audible signal receiver
				3	Sub-audible signal type 0: CTCSS, 1: CDCSS
				2	Is in-band signaling FSK_AIR mode 1: Yes 0: No, determined by [6:5]
67	W/R	0xDA1D	RSSISNR	15:14	SNR/RSSI update period 11: 12.5 ms; 10: 25 ms 01: 50 ms; 00: 100 ms
				13:08	SNR threshold for auto soft mute
				6:00	RSSI threshold for auto soft mute
68	R	Ready Only	RSSISNR	15	CS Filter Fir3 band Selection(Read back Value)
				14	SNR invalid 1: SNR result is invalid 0: SNR result is valid
				13:08	SNR indicator, 1 dB per step, 0 is minimum
				7	LNA RSSI 1: LNA gain should be set to 1 0: LNA gain should be set to 0
				6:00	RSSI indicator, 1 dB per step, 0 is minimum
69	W/R	0x07FF	AFC	15	1: Disable AFC 0: Enable AFC
				14:13	AFC control gain 0: 1/8, 1: 1/4, 2: 1/2, 3: 1
				12:00	AFC threshold (Unit: Hz)

70	R	0x0000	AFC	5	AFC rail 1: AFC indicator > AFC threshold 0: Else
				14	Link state 1: Link is active 0: Link is lost
				13:00	AFC residue frequency offset (Hz)
71	W/R	0x1E20		13:08	SNR threshold for AFC
				7	AFC Direction. 1: Inversed mode, 0: Normal mode
				6:00	RSSI threshold for AFC
72	W/R	0x2006	BB_FLT	13	1: Bypass Frequency Inversion 0: Not Bypass
				12	1: Bypass De-emphasis 0: Not Bypass De-emphasis
				9:07	HPF/ de-scrambling /de-emphasis execution order 3'b000: HPF->SCR->EMP 3'b001: HPF->EMP->SCR 3'b010: SCR->HPF->EMP 3'b011: SCR->EMP->HPF 3'b100: EMP->HPF->SCR 3'b101: EMP-> SCR->HPF
				2:00	RX volume control before DAC
73	W/R	0x270D	AUDIO	15	1: Hard Mute (Only affect when REG73[10]=0)
				10	Volume change speed 0: Normal, change to lower volume will be in slowly ramping down curve 1: Immediately
				3:00	Volume 4'd0: -39dB, 4'd1: -36dB 3 dB per step 4'd15: 6 dB
74	W/R	0x0000	AUDIO	15:13	Inversion frequency (Unit: Hz) 3'd0: 2700, 3'd1: 2800 3'd2: 2900, 3'd3: 3000 3'd4: 3100, 3'd5: 3200 3'd6: 3300, 3'd7: 3400
				7:00	RX_AUDIO_LEVEL (Read only)

75	W/R	0x7A80	DTMF	15:05	DTMF detection speed Suggest value: 1960
				2	DTMF_MARGIN1 mode 0: 0-6.3% 1: 0-63 Hz
				1	DTMF_MARGIN2 mode 0: 0-6.3% 1: 0-63 Hz
				0	DTMF_MARGIN3, 0: 5 ms; 1:10 ms
76	W/R	0xE204	DTMF	15:10	DTMF_MARGIN1 0: 0% or 0 Hz 0.1% or 1 Hz per step 63: 6.3% or 63 Hz
				9:04	DTMF_MARGIN2 Same definition as DTMF_MARGIN1
				2	1: Use match condition 1
				1	1: Use match condition 2
				0	0: Use set frequency as reference 1: Use detected frequency as reference
77	W	0x0000	DTMF	DTMF_TABLE	
				15:12	DTMF symbol address
				11	DTMF Symbol frequency band 0: low band, 1: high band
				10:00	DTMF symbol low band or high band tone frequency Unit: 1.0347 Hz
78	W/R	0x800F	DTMF	15	0: DTMF symbol frequency uses internal table (Not supported yet) 1: DTMF symbol frequency is set by user
				7:04	Address of found DTMF symbol
				3:00	DTMF symbol numbers in search table
79	R	0x0000	FSK	15:08	Address
				7:00	Type
80	R	0x0000	FSK	15:09	Size
				7:00	CRCA (Only used in free frame type)
81	W/R	0xB200	FSK	15:05	Symbol detection speed Suggest value: 1424
82	R	0x0000	FSK	15:00	Payload FIFO

83	W/R	0x8000	FSK	15:13	FIFO Threshold
				12	FIFO needs reading out
				5	Free format type
				4	CRCB_OK 1: No error in payload 0: Error in payload, will be automatically updated at the end of new RX packet
				3:00	Total words in read FIFO
84	W/R	0xFC40	SELCALL	15:05	SELCALL detection speed Suggest value: 2018
				2	MARGIN 1 mode 0: 0-6.3% 1: 0-63 Hz
				1	MARGIN2 mode 0: 0-6.3% 1: 0-63 Hz
				0	MARGIN3 0: 5 ms, 1: 10 ms
85	W/R	0x70A6	SELCALL	15:10	MARGIN1
				9:04	MARGIN2
				2	1: Use match condition 1
				1	1: Use match condition 2
				0	0: Use set frequency as reference 1: Use detected frequency as reference
86	W	0x03A0	SELCALL	15:12	SELCALL Symbol Address
				11:00	SELCALL symbol frequency Unit: 0.6467 Hz
87	W/R	0x800F	SELCALL	15	0: SELCAL symbol frequency uses internal table (Not supported yet) 1: SELCALL symbol frequency is set by user
				14	HPF_BYPASS 0: No bypass 1: Bypass
				13	1: Found symbol is lost
				7:04	The address of found SELCALL symbol
				3:00	SELCALL symbol numbers in search table

89	W/R	0xFF81	CTCSS	15:04	CTCSS detection speed, for example: 0xFF8 for high sensitivity and >1 second response time 0xF7A for normal sensitivity and <100 ms response time
				2	MARGIN 1 mode 0: 0-6.3% 1: 0-63 (Unit: 0.1616 Hz)
				1	MARGIN2 mode 0: 0-6.3% 1: 0-63 (Unit: 0.0404 Hz)
				0	MARGIN3 0: 20 ms, 1: 40 ms
90	W/R	0x7D26	CTCSS	15:10	MARGIN1
				9:04	MARGIN2
				2	1: Use match condition 1
				1	1: Use match condition 2
				0	0: Use set frequency as reference 1: Use detected frequency as reference
91	W	0x0000	CTCSS	CTCSS TABLE	
				15:13	CTCSSS symbol address
				12:00	CTCSSS symbol frequency Unit: 0.0404 Hz
92	W/R	0x8000	CTCSS	15	0: CTCSS symbol frequency uses internal table (Not supported yet) 1: CTCSS symbol frequency is set by user
				14	1: Bypass HPF
				13	1: Found CTCSS symbol is lost
				7:04	The address of found CTCSS symbol
				2:00	CTCSS symbol numbers in search table
93	W/R	0x0000	CTCSS CDCSS	8	CDCSS detected phase, 0: Normal 1: Invert phase
				1:00	CTCSS detect phase change 0: 0° 1:120° 2:180° 3: Reserved
94	W/R	0x8C00	CDCSS	15	1: Bypass HPF
				11	Parallel CTCSS receive enable (1)
				10	Parallel CDCSS receive enable (1)
				1	1: CDCSS code lost match
				0	1: CDCSS code is matched

101	R	Read Only	RF AGC	15:08	AGC_H; IF RSSI high level indicator
				7:00	AGC_L; IF RSSI low level indicator
102	R	Read Only	Ex-band Noise	12:00	Baseband out-of-band noise level
103	R	Read Only	Ex-band Noise	12:0	Ex-Band Noise Average Level
106	W/R	0x0000		13	Link-Loss interrupt select(REG116[6]) 1 : Ex-Noise 0: RSSI_SNR
				12:0	Ex-Band Noise Average High threshold
108	W/R	0x01F0	RF AGC	15	RF AGC disable 0: Enable RF AGC 1: Use manually set value
				8	LNA gain manually set value 1: High gain, 0: low gain
				7	IF filter bandwidth
				6:04	PGA manually set value, valid from 0 to 0x7, 3 dB per step
110	W/R	0x0022	RF AGC	RF AGC gain compensation	
112-119	W/R		Control and Interrupt		
112	W/R	0xA000 (Idle) 0xE000 (TX) 0xA000 (RX)	Operation Control	15	Power up digital section (1), Power down digital section (0)
				14	Digital logic operation mode 1: TX mode, 0: RX mode
				13	1: Normal work, 0: Software reset, it will not reset interface registers
				4:00	Should be set to 0 always
113	W/R	0x553D	Frequency control	15:00	High 16 bits of First Channel Frequency 137 kHz IF for 462.5625 MHz narrow band(0x4553D)
114	W/R	0x5E82	Frequency control	15:00	Low 16 bits of First Channel Frequency 137 kHz IF for 462.5625 MHz narrow band(0x5EDE)

115	W/R	0x0000	Interrupt MASK	15	1: Enable interrupt 0: Disable all interrupt
				14	Enable FSK transmit success interrupt
				13	Enable FSK transmitter FIFO need fill interrupt
				12	Enable FSK head receive success interrupt
				11	Enable FSK receiver FIFO need read interrupt
				10	Enable DTMF receive interrupt
				9	Enable SELCALL receive interrupt
				8	Enable CTCSS receive interrupt
				7	Enable CTCSS tone loss interrupt
				6	Enable link lost interrupt (RSSI and SNR are less than their threshold)
				5	Enable CDCSS receive interrupt
				4	Enable CDCSS code lost match interrupt
				3	Enable VOX voice detected interrupt
				2	Enable TOT time out interrupt
				1	Enable FSK receive complete interrupt
				0	CTCSS phase change interrupt enable
116	W/R	0x0000	Interrupt flags (Active high) Set by hardware and reset by software (write 1 will clear interrupt bit to 0)	15	1: Reset all flags to zeros
				14	FSK transmit success interrupt
				13	FSK transmitter FIFO need fill interrupt
				12	FSK head receive success interrupt
				11	FSK receiver FIFO need read interrupt
				10	DTMF receive interrupt
				9	SELCALL receive interrupt
				8	CTCSS receive interrupt
				7	CTCSS tone loss interrupt
				6	Link lose interrupt
				5	CDCSS receive interrupt
				4	CDCSS code lost match interrupt
				3	VOX voice detected interrupt (Can only be cleared in TX mode)
				2	TOT time out interrupt (Can only be cleared in RX mode)
				1	FSK receive complete interrupt
				0	CTCSS phase change interrupt

117	W/R	0x0000	GPIO	12	1: Loop TX in-band signal to RX audio path
				10	0: Normal IF, low side injection 1: Opposite IF, high side injection
				5:04	GPIO2 mode control 00: as input 01: output low 10: output high 11: reserved
				3:02	GPIO1 mode control, as GPIO2
				1:00	GPIO0 mode control, as GPIO2
118	R	0x0000	GPIO	2	GPIO2 input value
				1	GPIO1 input value
				0	GPIO0 input value
122	W/R	0x46A3	FSK	FSK bit rate setting = reference_clock/bit_rate Default is: 21.7e6/1200	
123	W/R	0x0002	CDCSS	MSB 2 bits of CDCSS bit rate setting = referenc_clock/bit_rate Default is: 21.7e6/134.4	
124	W/R	0x76B2	CDCSS	LSB 16 bits of CDCSS bit rate setting = referenc_clock/bit_rate Default is: 21.7e6/134.4	
125	W/R	0x0000	Squelch	8	Threshold for glitch pulse 1: 3/4pi, 0: pi/2
				7:00	Glitch counter (ready only)
126	W/R	0x0048	Frequency control	4	IF constant, different for each operation band
				3:00	TX deviation gain control 0: 1/8; 1: 2/8; 15: 2
127	W/R	0xA9BF	Frequency control	IF constant, different for each operation band For 88 kHz IF and 409.75 MHz narrow band(0x6D08)	

4 Pin Assignment

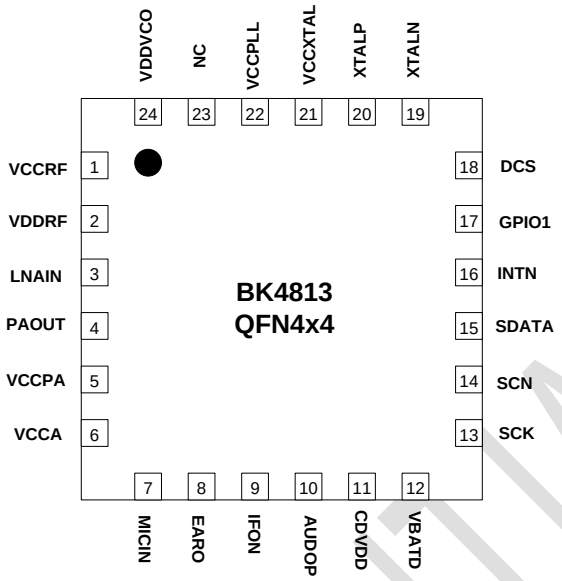

Figure 16. BK4813 Pin Assignment (Top View)

Table 13. BK4813 4mmx4mm 24-Pin Definition

Pin #	Name	Direction	Function
1	VCCRF	Input	Power Supply, 2.4 V~ 3.6 V
2	VDDRF	Input	LNA regulator output, with decoupling capacitor to ground.
3	LNAIN	Input	LNA input
4	PAOUT	Output	PA output
5	VCCPA	Input	Power supply to PA regulator, 2.4 V~ 3.6 V
6	VCCA	Input	Power supply to audio regulator, 2.4 V~ 3.6 V
7	MICIN	Input	Microphone input
8	EARO	Output	Earpiece output
9	IFON	Output	Test pin. Should be floating
10	AUDOP	Output	Output of TX audio PGA
11	CDVDD	Output	Digital regulator output, with decoupling capacitor to ground
12	VBATD	Input	Power supply, 2.4 V to 3.6 V
13	SCK	Input	SPI clock
14	SCN	Input	SPI enable
15	SDATA	I/O	SPI data
16	INTN	Output	Interrupt Signal to MCU
17	GPIO1	I/O	GPIO1
18	DCS	Output	DCS output, for software DCS decoding
19	XTALN	Output	Crystal oscillator port, output
20	XTALP	Input	Crystal oscillator port, input
21	VCCXTAL	Input	Power Supply, 2.4 V~ 3.6 V
22	VCCPLL	Input	Power Supply, 2.4 V~ 3.6 V
23	NC		
24	VDDVCO	Output	VCO regulator output, with decoupling capacitor to ground.

5 Typical Application Schematic

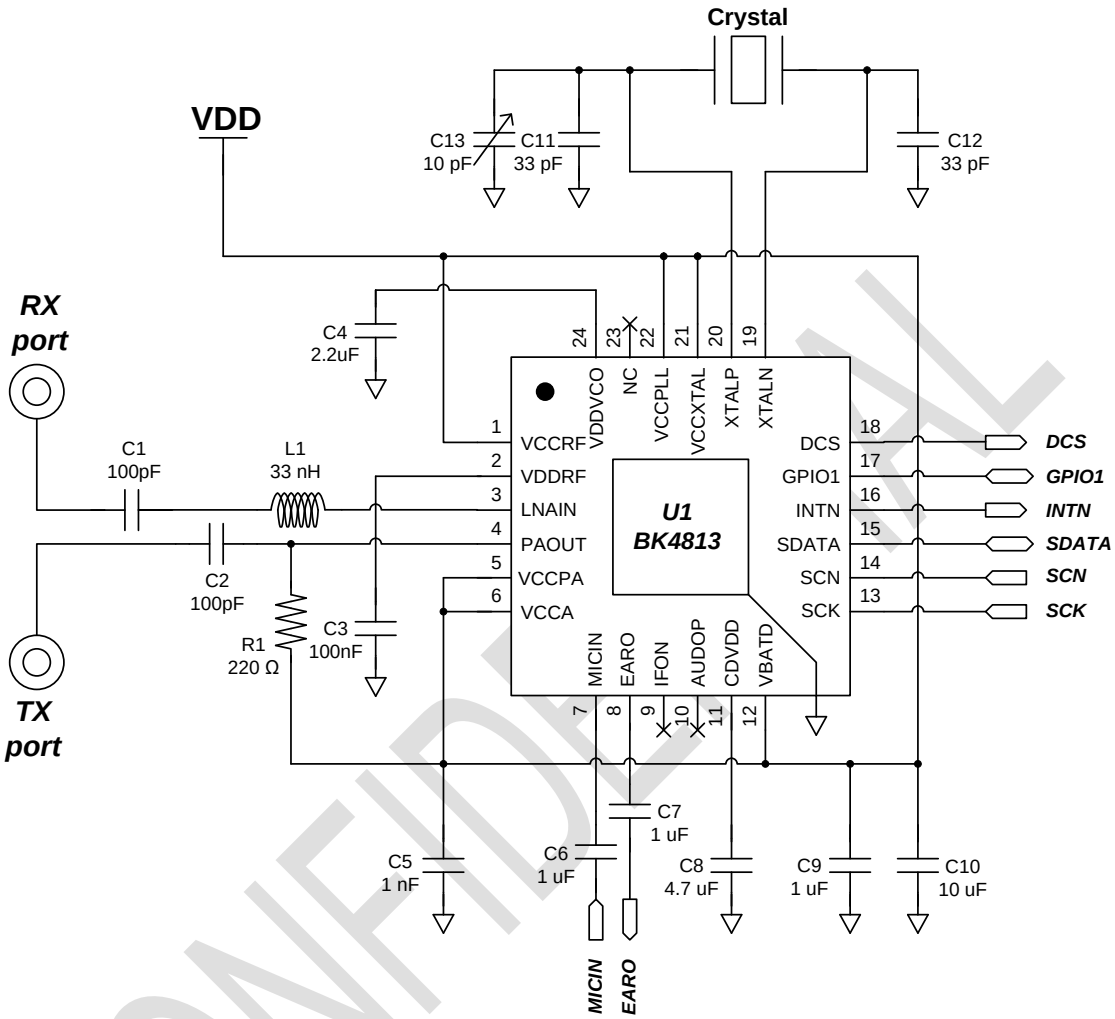

Figure 17. BK4813 Application

6 Package Information

QFN4x4 24pinpackageis available for BK4813. Detail information of the package follows:

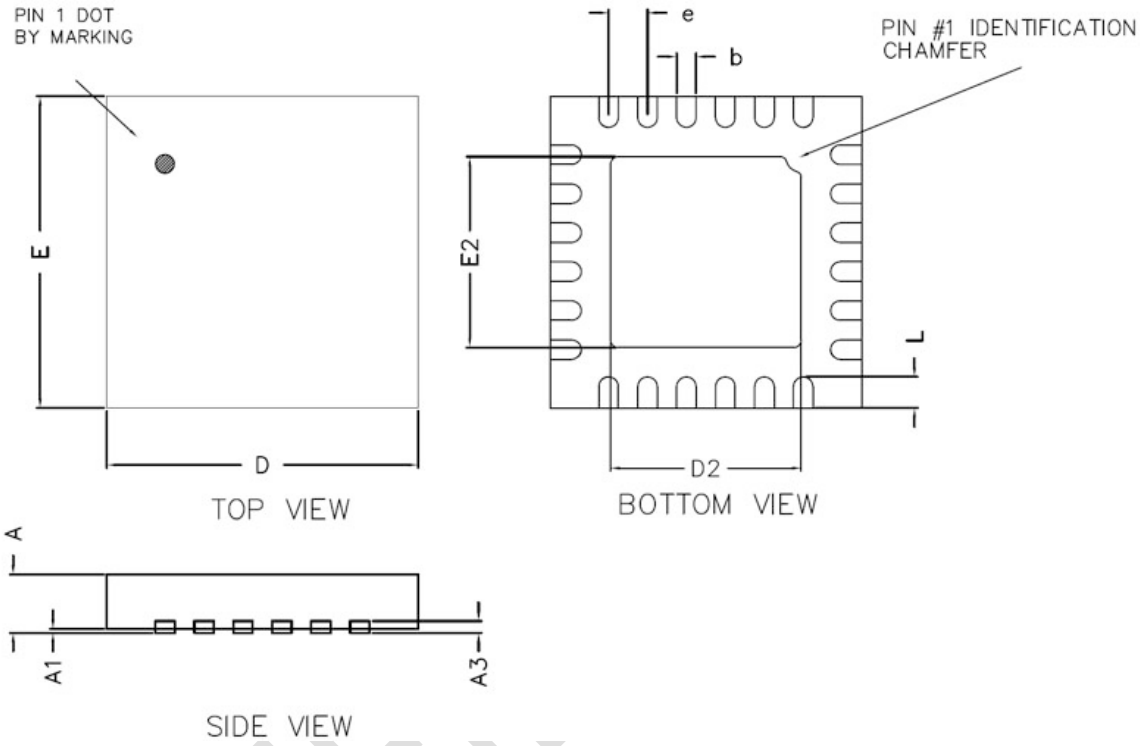

Figure 18. QFN 4x4 24 Pin Package diagram

Table 14. QFN 4x4 24 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	-	0.05	mm
A3		0.20 REF		mm
D	3.95	4.00	4.05	mm
E	3.95	4.00	4.05	mm
b	0.20	0.25	0.30	mm
L	0.35	0.40	0.45	mm
D2	2.30	2.45	2.55	mm
E2	2.30	2.45	2.55	mm
e		0.50 REF		mm

Soldering layer content

Content	width	unit
Ni	0.5-2.0	um
Pd	0.02-0.15	um
Au	0.003-0.015	um

Storage Caution

1. Calculated shelf life in vacuum sealed bag 12 months at<40℃ and 90% relative humidity(RH).
2. Peak package body temperature 260℃.
3. After vacuum sealed bag is opened ,devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within 168 hours of factory conditions<40℃/60%.
   b) Stored at 10% RH.

7 Tape and Reel Information

All dimensions are in millimeters by default.

7.1 Tape Information

The figure below shows the dimensions of the tape for the BK4813 QFN.

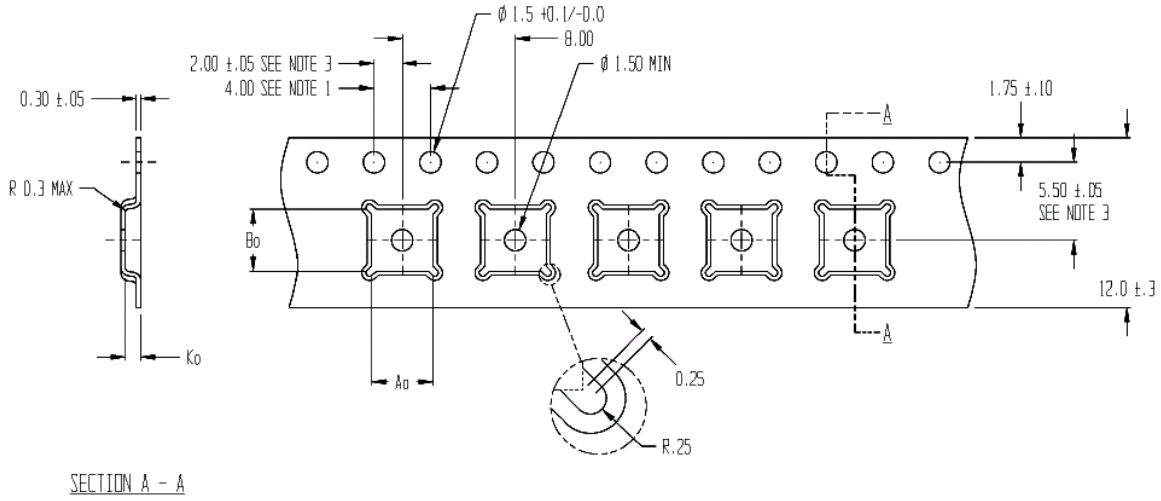

Figure 19. Tape Dimensions

A_0	B_0	K_0	Unit	Notes
4.35	4.35	1.1	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2. 2. Camber in compliance with EIA 481. 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

7.2 Cover Information

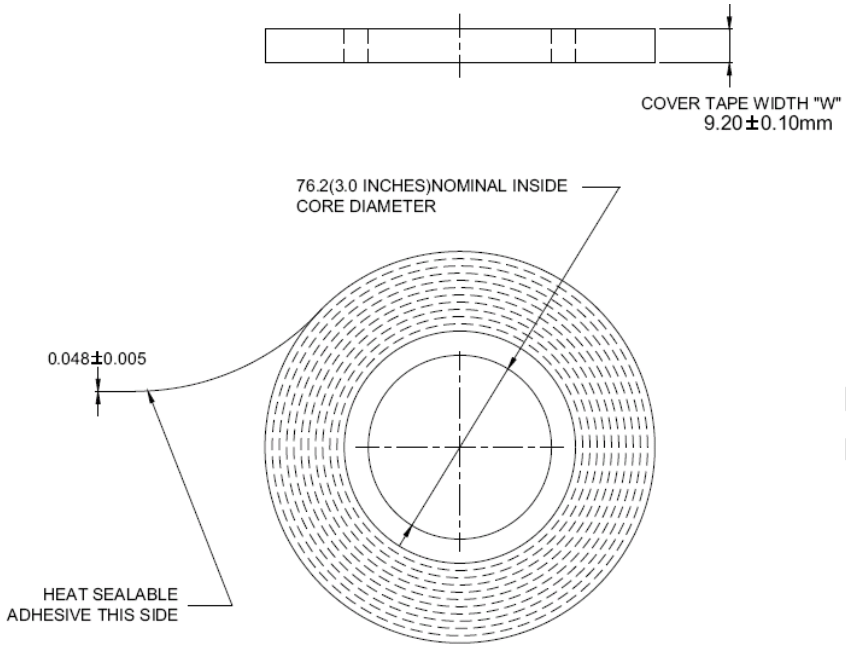

Figure 20. Cover Dimensions

Note:

1. Reel to contain 300 meters of splice free material.
2. Material: Polyester film with antistatic coating and adhesive coating.
3. Color: Transparent, natural

7.3 Reel Information

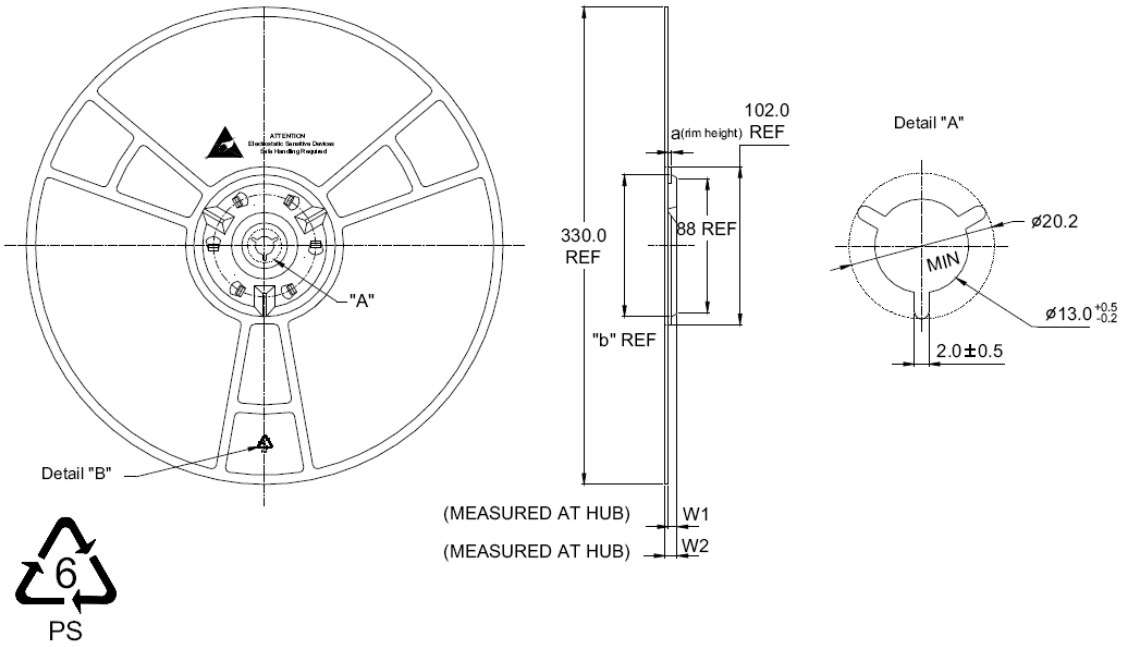

Figure 21. Reel Dimensions

Nominal Hub Width	W1 +0.6mm -0.4mm	W2 MAX	a	b	Unit
12	12.8	18.2	1.5	96.5	mm

8 Solder Reflow Profile

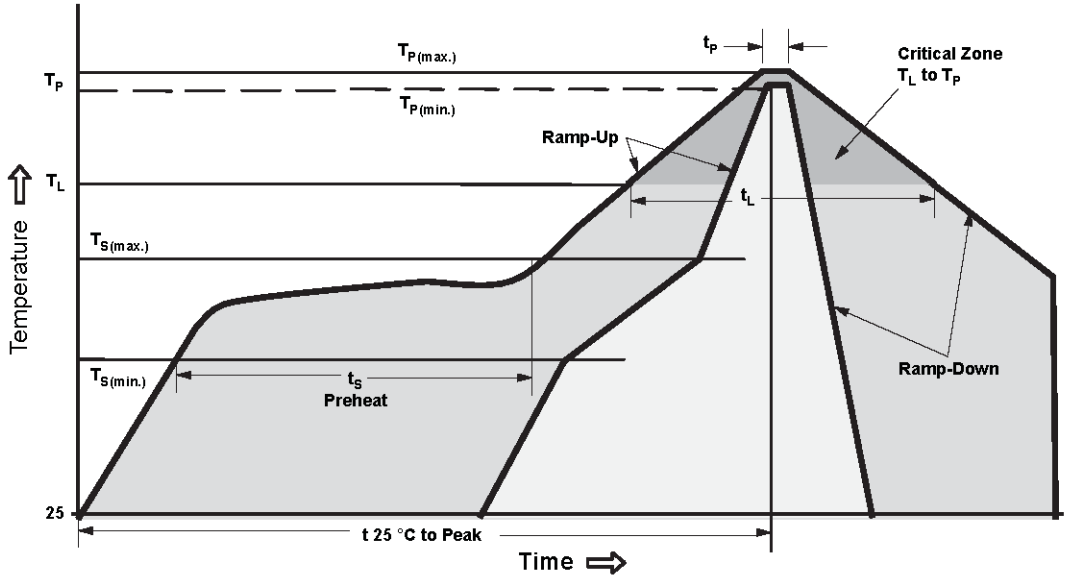

Figure 22. Classification Reflow Profile

Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3°C/second max.
Pre_heat	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217°C
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate 6		6°C/second max.
Time 25°C to Peak Temperature 8		8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

9 Order Information

Part number	Package	Packing	MOQ (ea)
BK4813QB	QFN	Tape Reel	3 k

Remark:
MOQ: Minimum Order Quantity

10 Additional Reference Resources

- User Guide
- Application Notes
- Programming Guide

11 Revision History

Version	Change Summary	Date	Author
Rev.0.1	Initial draft	2013/11/01	PH
Rev.0.2	Modify *Electrical Specification* according to the test results.	2014/01/01	PH
Rev 0.3	Updated register setting about TX audio.	2014/02/17	PH
Rev 1.0	Formal release.	2014/02/21	PH
Rev 1.1	Add the figure illustration about pre-emphasis, high-pass filter and low-pass filter in TX baseband.	2014/03/11	PH
Rev 1.2	Modify *Contact Information* in section 12.	2014/12/04	PH
Rev 1.3	Add detailed register description about TX audio part	2015/02/09	PH
Rev 1.4	Update PIN assignment Update the frequency coverage of the synthesizer	2015/03/20	PH

12 Contact Information

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