BK3296 Datasheet

DS-BK3296-E03 V0.9

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Contents

1. Features

Bluetooth

- Bluetooth 5.2 compliant
- Supports Basic Rate (BR), Enhanced Data Rate (EDR) 2 Mbps and 3 Mbps, and Low Energy (LE) 1 Mbps
- TX power up to +8 dBm
- RX sensitivity -95 dBm
- Bluetooth profiles: A2DP, AVRCP, HFP, HID, AVCTP, AVDTP, and SPP
- True wireless stereo and two active links
- Fast link setup and fast role switch

Core and Memory

- 32-bit MCU at up to 120 MHz
- Flash
- 128 KB RAM
- 256 KB ROM
- 64 KB Cache
- 32-bit eFuse
- UART for debugging and downloading
- Charging port communication supported

Clock Management

- External oscillator: 26 MHz crystal oscillator (X26M)
- Internal oscillator: 32 kHz ring oscillator (ROSC)
- 120 MHz PLL

Power Management

- 2.8 to 4.35 V VCC4BAT supply
- 4.75 to 5.75 V VCC5USB supply
- On-chip power-on reset (POR) and brown-out detector (BOD)
- Embedded buck (DC-DC) converter and LDO regulators
- Low power consumption:
  - A2DP: 2.8 mA

- Shutdown: TBD

Peripherals

- GPIOs: 11 in QFN32 (BK3296QN323), 6 in QFN20 (BK3296QN223), 7 in QFN20 (BK3296QN213)
- 1x SPI (only BK3296QN323)
- 2x UART: 2 with hardware flow control, 1 with flash download support
- 1x I2C
- Up to 6x 32-bit PWM
- 120 mA battery charge controller
- 1x I2S (only BK3296QN323)
- 2x audio ADC
- 2x audio DAC
- Four-band digital hardware equalizer
- FFT/FIR/SBC accelerator
- 12-bit SAR ADC, up to 4 channels
- 6x general-purpose 32-bit timer/counter
- 1x Watchdog timer
- 1x low-power timer
- 1x IrDA decoder interface
- 1x temperature sensor
- Up to 6x touch sensor

Packaging

- QFN32 package, 4 x 4 mm
- QFN20 package, 3 x 3 mm
- Operating temperature range: -20 to +85 ℃

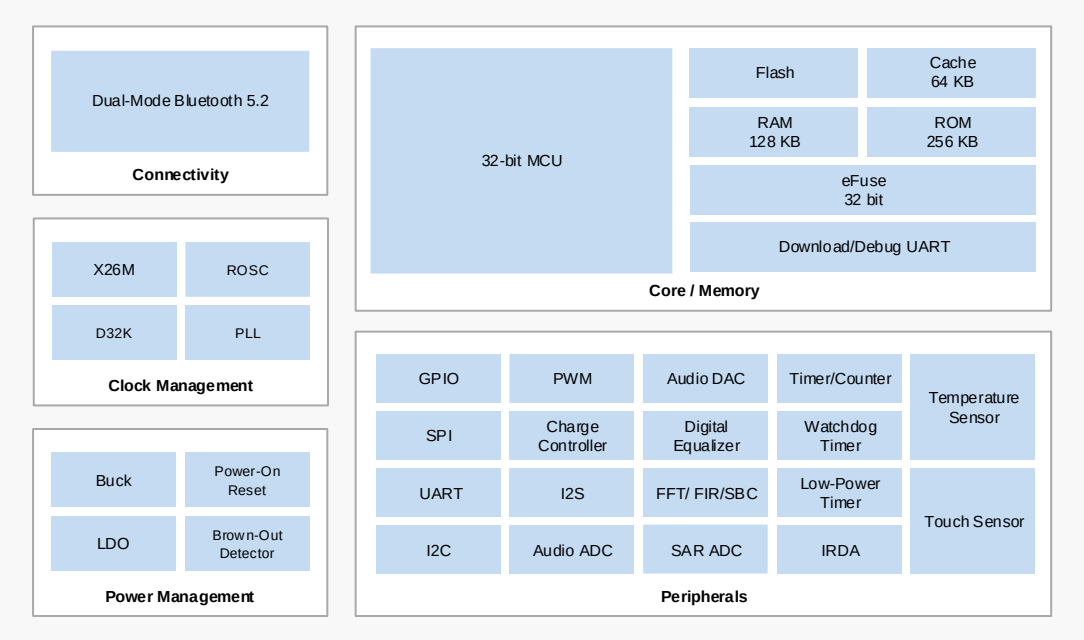
2. Overview

The BK3296 is a highly-integrated single-chip Bluetooth 5.2 audio system-on-chip (SoC) which supports Bluetooth LE, BR and EDR. It integrates a high-performance Bluetooth RF transceiver, a feature-rich baseband processor, a memory controller, multiple analog and digital peripherals, and Bluetooth protocol stacks including the audio, voice, and SPP profiles.

Using advanced design techniques and ultra-low-power process technology, BK3296 delivers advanced audio processing and minimal power consumption for audio applications including TWS earbuds, wireless headsets, control and multimedia hybrid applications, etc.

Figure 2-1 shows the general block diagram of BK3296.

Figure 2-1 BK3296 Block Diagram



BK3296 devices are offered in several packages. The set of included peripherals varies depending on package. Table 2-1 shows the list of peripherals available on each part number.

Table 2-1 Device Options and Features

Feature		BK3296QN323	BK3296QN223	BK3296QN213
Flash		Yes	Yes	Yes
GPIO		11	6	7
SPI	Master/Slave	1	-	-
UART		2	1	1

Feature		BK3296QN323	BK3296QN223	BK3296QN213
I2C	Master/Slave	1	1	1
PWM	PWM0 ~ 5	6	2	3
Charge controller		Yes	Yes	Yes
I2S	Master/Slave	1	-	-
Audio ADC		2	1	1
Audio DAC		Stereo	Stereo	Mono
Digital equalizer		Yes	Yes	Yes
FFT/FIR/SBC accelerator		Yes	Yes	Yes
SAR ADC	12 bits	1	1	1
	Number of channels	4	1	2
Timer	General-purpose timer/counter	6	6	6
	Watchdog timer	1	1	1
	Low-Power timer	1	1	1
IrDA		1	1	1
Temperature sensor		1	1	1
Touch sensor	TS0 ~ 5	6	2	3
Package		4 x 4 mm QFN32	3 x 3 mm QFN20	3 x 3 mm QFN20
Operating voltage		2.8 to 4.35 V		
Operating temperature		-20 to +85 ℃		

3. Pin Description

BK3296 provides Bluetooth functionality in several packages ranging from 20 pins to 32 pins.

3.1 BK3296QN323 Pin Description

Figure 3-1 shows the pin assignments of the 4 x 4 mm, 32-pin QFN package for BK3296QN323.

Figure 3-1 QFN32 Pin Assignments of BK3296QN323

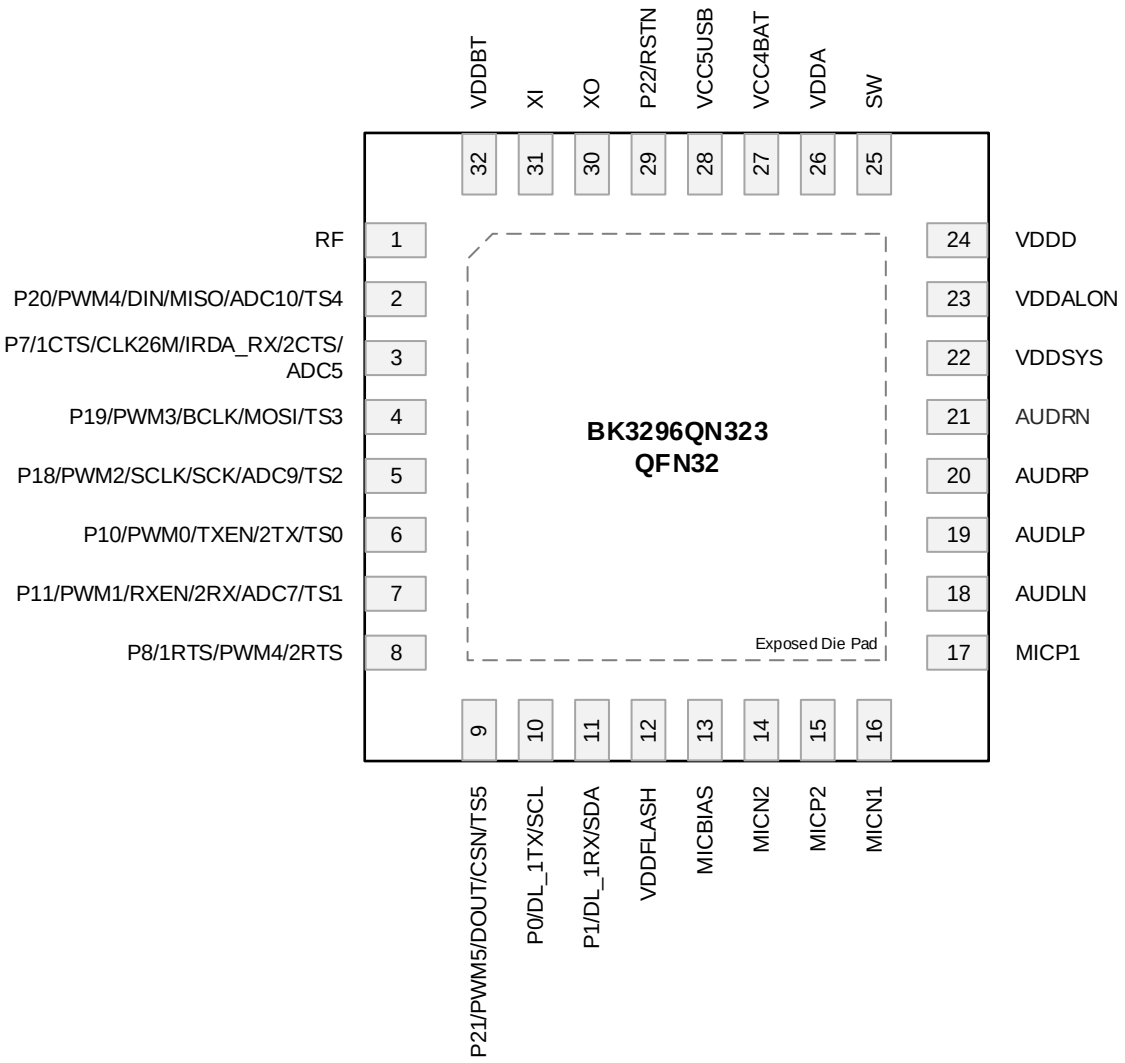


Table 3-1 shows the pin descriptions of BK3296QN323.

Table 3-1 QFN32 Pin Descriptions of BK3296QN323

Pin #	Name	I/O	Type	Description
1	RF	-	RF	2.4 GHz RF signal port
2	P20/PWM4/DIN/MISO/ADC10/ TS4	I/O	Digital/Analog	• GPIO20 • PWM4 (differential with PWM5) • I2S: DIN • SPI: MISO • ADC10 • Touch sensor 4
3	P7/1CTS/CLK26M/IRDA_RX/ 2CTS/ADC5	I/O	Digital/Analog	• GPIO7 • UART1: CTS • 26 MHz clock output (divide by 2/4/8/16/32) • IRDA RX • UART2: CTS • ADC5
4	P19/PWM3/BCLK/MOSI/TS3	I/O	Digital/Analog	• GPIO19 • PWM3 (differential with PWM2) • I2S: BCLK • SPI: MOSI • Touch sensor 3
5	P18/PWM2/SCLK/SCK/ADC9/ TS2	I/O	Digital/Analog	• GPIO18 • PWM2 (differential with PWM3) • I2S: SCLK • SPI: SCK • ADC9 • Touch sensor 2
6	P10/PWM0/TXEN/2TX/TS0	I/O	Digital/Analog	• GPIO10 • PWM0 (differential with PWM1) • TX enable • UART2: TX • Touch sensor 0
7	P11/PWM1/RXEN/2RX/ADC7/ TS1	I/O	Digital/Analog	• GPIO11 • PWM1 (differential with PWM0) • RX enable

Pin #	Name	I/O	Type	Description
				• UART2: RX • ADC7 • Touch sensor 1
8	P8/1RTS/PWM4/2RTS	I/O	Digital	• GPIO8 • UART1: RTS • PWM4 (differential with PWM5) • UART2: RTS
9	P21/PWM5/DOUT/CSN/TS5	I/O	Digital/Analog	• GPIO21 • PWM5 (differential with PWM4) • I2S: DOUT • SPI: CSN • Touch sensor 5
10	P0/DL_1TX/SCL	I/O	Digital	• GPIO0 • UART1: TX (Flash Download support) • I2C: SCL
11	P1/DL_1RX/SDA	I/O	Digital	• GPIO1 • UART1: RX (Flash Download support) • I2C: SDA
12	VDDFLASH	-	Analog output	Flash voltage output, can be shut down in idle state, connected to VDDSYS
13	MICBIAS	-	Analog output	Microphone bias output
14	MICN2	-	Analog input	Microphone 2 negative input
15	MICP2	-	Analog input	Microphone 2 positive input
16	MICN1	-	Analog input	Microphone 1 negative input
17	MICP1	-	Analog input	Microphone 1 positive input
18	AUDLN	-	Analog output	Audio left channel negative output
19	AUDLP	-	Analog output	Audio left channel positive output
20	AUDRP	-	Analog output	Audio right channel positive output
21	AUDRN	-	Analog output	Audio right channel negative output
22	VDDSYS	-	Analog output	System LDO output

Pin #	Name	I/O	Type	Description
23	VDDALON	-	Analog output	Always on LDO output
24	VDDD	-	Analog output	Digital LDO output
25	SW	-	BUCK output	BUCK switch output
26	VDDA	-	Analog output	Analog LDO output
27	VCC4BAT	-	Power	Battery input, up to 4.35 V
28	VCC5USB	-	Power/Digital/ Analog	USB 5.0 V input or DLP or 3.3 V Reset input
29	P22/RSTN	I/O	Digital/Analog	• GPIO22 • Reset input, active-low
30	XO	-	Analog output	26 MHz crystal output
31	XI	-	Analog input	26 MHz crystal input
32	VDDBT	-	Analog output	Bluetooth radio LDO output
Die pad	GND_SLUG	-	GND	Ground

3.2 BK3296QN223 Pin Description

Figure 3-2 shows the pin assignments of the 3 x 3 mm, 20-pin QFN package for BK3296QN223.

Figure 3-2 QFN20 Pin Assignments of BK3296QN223

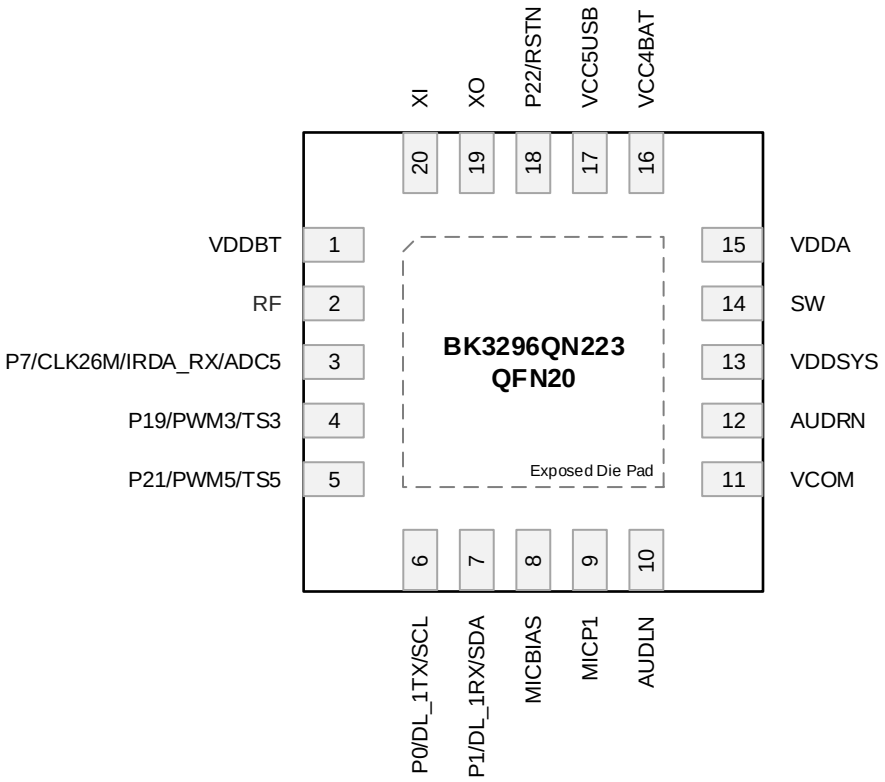


Table 3-2 shows the pin descriptions of BK3296QN223.

Table 3-2 QFN20 Pin Descriptions of BK3296QN223

Pin #	Name	I/O	Type	Description
1	VDDBT	-	Analog output	Bluetooth radio LDO output
2	RF	-	RF	2.4 GHz RF signal port
3	P7/CLK26M/IRDA_RX/ADC5	I/O	Digital/Analog	• GPIO7 • 26 MHz clock output (divide by 2/4/8/16/32) • IRDA RX • ADC5
4	P19/PWM3/TS3	I/O	Digital/Analog	• GPIO19 • PWM3 • Touch sensor 3
5	P21/PWM5/TS5	I/O	Digital/Analog	• GPIO21 • PWM5

Pin #	Name	I/O	Type	Description
				• Touch sensor 5
6	P0/DL_1TX/SCL	I/O	Digital	• GPIO0 • UART1: TX (Flash Download support) • I2C: SCL
7	P1/DL_1RX/SDA	I/O	Digital	• GPIO1 • UART1: RX (Flash Download support) • I2C: SDA
8	MICBIAS	-	Analog output	Microphone bias output
9	MICP1	-	Analog input	Microphone 1 positive input
10	AUDLN	-	Analog output	Audio left channel negative output
11	VCOM	-	Analog output	Common mode output
12	AUDRN	-	Analog output	Audio right channel negative output
13	VDDSYS	-	Analog output	System LDO output
14	SW	-	BUCK output	BUCK switch output
15	VDDA	-	Analog output	Analog LDO output
16	VCC4BAT	-	Power	Battery input, up to 4.35 V
17	VCC5USB	-	Power/Digital/ Analog	USB 5.0 V input or DLP or 3.3 V Reset input
18	P22/RSTN	I/O	Digital/Analog	• GPIO22 • Reset input, active-low
19	XO	-	Analog output	26 MHz crystal output
20	XI	-	Analog input	26 MHz crystal input
Die pad	GND_SLUG	-	GND	Ground

3.3 BK3296QN213 Pin Description

Figure 3-3 shows the pin assignments of the 3 x 3 mm, 20-pin QFN package for BK3296QN213.

Figure 3-3 QFN20 Pin Assignments of BK3296QN213

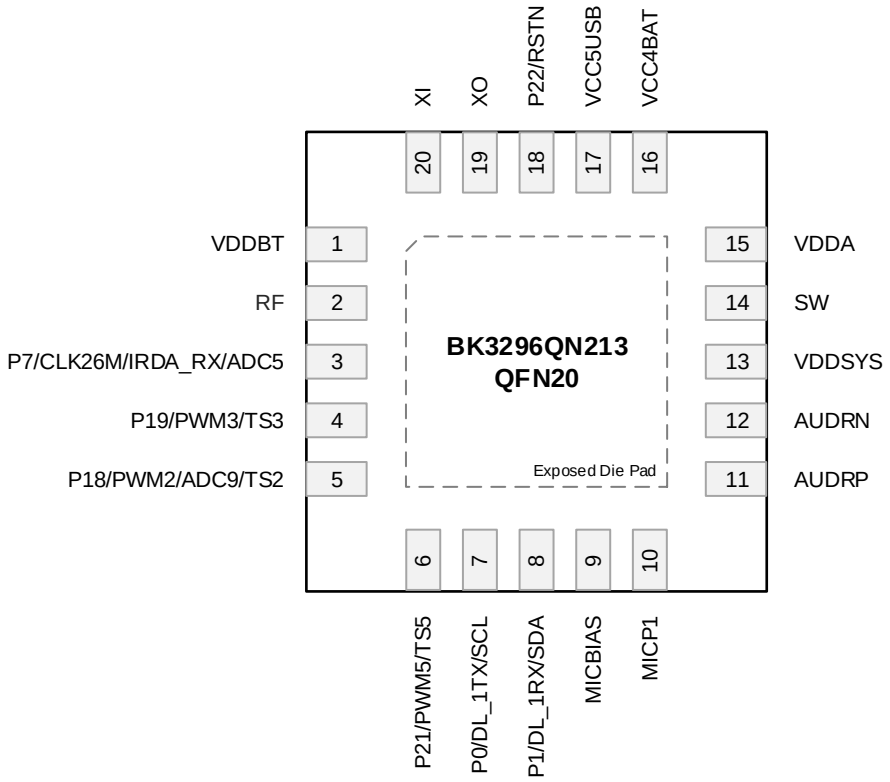


Table 3-3 shows the pin descriptions of BK3296QN213.

Table 3-3 QFN20 Pin Descriptions of BK3296QN213

Pin #	Name	I/O	Type	Description
1	VDDBT	-	Analog output	Bluetooth radio LDO output
2	RF	-	RF	2.4 GHz RF signal port
3	P7/CLK26M/IRDA_RX/ADC5	I/O	Digital/Analog	• GPIO7 • 26 MHz clock output (divide by 2/4/8/16/32) • IRDA RX • ADC5
4	P19/PWM3/TS3	I/O	Digital/Analog	• GPIO19 • PWM3 (differential with PWM2) • Touch sensor 3
5	P18/PWM2/ADC9/TS2	I/O	Digital/Analog	• GPIO18 • PWM2 (differential with PWM3)

Pin #	Name	I/O	Type	Description
				• ADC9 • Touch sensor 2
6	P21/PWM5/TS5	I/O	Digital/Analog	• GPIO21 • PWM5 • Touch sensor 5
7	P0/DL_1TX/SCL	I/O	Digital	• GPIO0 • UART1: TX (Flash Download support) • I2C: SCL
8	P1/DL_1RX/SDA	I/O	Digital	• GPIO1 • UART1: RX (Flash Download support) • I2C: SDA
9	MICBIAS	-	Analog output	Microphone bias output
10	MICP1	-	Analog input	Microphone 1 positive input
11	AUDRP	-	Analog output	Audio right channel positive output
12	AUDRN	-	Analog output	Audio right channel negative output
13	VDDSYS	-	Analog output	System LDO output
14	SW	-	BUCK output	BUCK switch output
15	VDDA	-	Analog output	Analog LDO output
16	VCC4BAT	-	Power	Battery input, up to 4.35 V
17	VCC5USB	-	Power/Digital/ Analog	USB 5.0 V input or DLP or 3.3 V Reset input
18	P22/RSTN	I/O	Digital/Analog	• GPIO22 • Reset input, active-low
19	XO	-	Analog output	26 MHz crystal output
20	XI	-	Analog input	26 MHz crystal input
Die pad	GND_SLUG	-	GND	Ground

4. Functional Description

4.1 Modes of Operation

The general operation of BK3296 is as follows. After system reset, BK3296 enters deep sleep mode waiting for external circuitry via the GPIO interface to wake up the device. Once the device is woken up, it will establish a connection with other Bluetooth devices by using the Inquire and Paging states.

Shutdown – In this mode, all circuits are powered down. Software can bring the system into this mode by writing special registers and the system can only be woken up by active level applied on GPIOs.

Deep Sleep – In this mode, all circuits are powered down except GPIOs and the always on logic. Any GPIO edge transition or low-power timer time-out event can wake up the system again. The retention registers can keep their contents at this mode.

Active – In this mode, BK3296 and the other connected Bluetooth device are actively receiving and transmitting data on the channel. This data can be high fidelity audio, voice, or control commands depending on the application.

Test – BK3296 provides a test mode to test the internal RAM memory BIST and other blocks. The test mode is normally not used.

4.2 RF Transceiver

BK3296 integrates a high-performance Bluetooth transceiver and frequency synthesizer. The transceiver is fully differential and incorporates an on-chip balun which transforms the single-ended RF signal from the antenna via pin RF into an internal differential balanced signal for the low noise amplifier (LNA). On the transmit side, the differential outputs of the power amplifier (PA) are combined and transformed to a single-ended output using the same on-chip balun thus enabling only one RF pin connection to the antenna for both transmit and receive operations. The device is able to output +8 dBm of transmit output power, allowing users to develop a class 2 (+4 dBm) device with small printed circuit board (PCB) antennas. The frequency synthesizer is fully integrated and does not require any external components.

4.3 Bluetooth Baseband

BK3296 Bluetooth baseband implements the Bluetooth 5.2 Enhanced Data Rate (EDR) modem, providing Basic Rate (BR) 1 Mbps and Low Energy (LE) 1 Mbps as well as the enhanced 2 Mbps, and 3 Mbps data rates.

Table 4-1 Bluetooth Modulation Formats

Data Rate	Modulation	Bits/Symbol
BR/LE: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4-DQPSK	2
EDR: 3 Mbps	8-DPSK	3

The Bluetooth baseband utilizes a combination of both hardware blocks and firmware for the frequency hopping sequence generator, access code generation, detection, and correlation, encryption and decryption for security, forward error correction, 16-bit CRC, packet construction, and Bluetooth clocks and timers to optimize for power consumption and user programmability.

4.4 Beken Bluetooth Stack

BK3296 comes with Bluetooth 5.2 dual mode compliant protocol stacks which run on the internal 32-bit RISC MCU. The SoC also runs the application program removing the need for an external host controller. An external host can be connected via the UART interface for debugging purposes, but is not required to run the application. Beken provides a development kit that customers can use to configure their applications. The development kit includes a software configuration tool and reference software code for stereo-mode Bluetooth speakers and hands-free operation. Interested readers are encouraged to contact their local Beken representative for more information.

4.5 Crystal Oscillator

BK3296 contains an integrated crystal oscillator driver circuit to drive an external 26 MHz crystal. The 26 MHz crystal frequency provides the reference frequency for the frequency synthesizer and can also be selected as the reference clock for the internal PLL.

If an external reference clock is used, the clock input should be applied to the XI pin. Care must be taken not to overdrive the XI input with a voltage above 1.05 V.

There is tunable load capacitance from 6 to 18 pF (Both side have this capacitance) with 64 steps to tune the crystal frequency, that no external capacitance is needed. The startup time of the clock signal is about one milliseconds.

4.6 Clock

The system has several root clock signals: X26M, D32K, ROSC, and PLL.

- X26M: 26 MHz crystal oscillator.
- D32K: 32 kHz clock signal divided from X26M
- ROSC: 32 kHz internal low frequency ring oscillator
- PLL: High speed 120 MHz PLL clock

The clock selection options for MCU and peripherals are listed as follows.

Table 4-2 Clock Selection

MCU and Peripherals	X26M	ROSC	D32K	PLL
MCU	√			√
FLASH Controller	√			√
FFT/FIR	√			√
SBC	√			√
SPI	√			
UART	√			
I2C	√			
PWM	√		√	
I2S	√			√
Audio ADC	√			
Audio DAC	√			
SAR ADC	√			
Timer0	√			
Timer1		√	√	
Watchdog timer			√	
Low-power timer		√	√	
IrDA	√			

The system also has clock output capability to output clock signals to external components.

- The X26M clock can be output to GPIO7 for general purpose.

4.7 Reset

A reset can be triggered by the following sources: Power-on reset, brown-out reset, watchdog reset, low level on RSTN pin (external reset), software reset, and wakeup from shutdown mode or deep sleep mode.

System power on, digital power on and watchdog reset have the same reset effect one major blocks except always on logic, that any reset will reset the whole chip to initial status. The always on logic has one 32-bit timer and 16-bit retention registers, which can only be reset to initial value by system power on reset.

Wakeup from either shutdown mode or deep sleep mode will power on digital from power down mode, which triggers the whole system reset procedure.

4.8 Power Management

The power management system on BK3296 includes a battery charger, a buck regulator which can be configured as a low–drop out (LDO) regulator and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

BK3296 can be powered directly from a 2.8 V to 4.35 V external battery via the VCC4BAT pin or a 4.75 V to 5.75 V USB power supply via the VCC5USB pin. When only an external battery is available, the SYS LDO regulator is powered by it via the VCC4BAT pin; when only a USB power supply is available, the SYS LDO regulator is powered by it via the VCC5USB pin. When both the battery and USB power supply are available, the SYS LDO regulator is powered by the USB power via the VCC5USB pin if the battery is below 3.0 V, and by the battery via the VCC4BAT pin if the battery is above 3.0 V.

BK3296 can operate in BUCK mode or LDO mode. When operating in BUCK mode, most of the modules are powered by the buck regulator; in LDO mode, all modules are powered by the SYS LDO regulator. Outputs from the buck and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the BK3296 EVB User Guide and application note for more details about choosing the proper bypass capacitors.

BK3296 can enter deep sleep mode when there is no active connection. BK3296 can be woken from deep sleep mode by any GPIO signal or by applying the USB power supply.

4.9 GPIO

BK3296 has up to 11 GPIOs. Each can be configured as either input or output. Each GPIO has alternate functions.

All GPIO pins can wake up the internal MCU from deep sleep mode. In deep sleep mode, any level change on the set GPIO will trigger the wakeup procedure.

In shutdown mode, the system can be woken up on a low level on GPIO22 or any other GPIOs configured as wakeup sources. Two of any other GPIOs except GPIO22 can be configured as wakeup sources at the same time.

4.10 SPI

BK3296 integrates a SPI interface that can operate in master or slave mode with up to 26 MHz clock speed. The SPI 4-wire master/slave interface consists of four signals: SCK, CSN, MOSI and MISO.

The receive data can be latched on either rising edge or falling edge of clock signal. The transmit data can be set by MSB or LSB first.

4.11 UART

BK3296 includes two Universal Asynchronous Receiver/Transmitter (UART) interfaces, UART1 and UART2, which offer full-duplex, asynchronous serial communication at a baud rate up to 3.25 Mbps. They support 5/6/7/8 bits data, and even, odd or none parity check. The stop bit can be either 1 bit or 2 bits.

Both UART1 and UART2 support hardware flow control with RTS and CTS signal. UART1 also supports Flash download.

4.12 I2C

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). BK3296 embeds a I2C interface, which could act as Master mode or Slave mode. The I2C supports standard (up to 100 kbps) and fast (up to 400 kbps) modes with 7-bit addressing. If low level on SCL or bus idle duration is greater than a programmable threshold, it will generate interrupt to MCU.

4.13 PWM

BK3296 has up to six 32-bit PWM channels, labeled PWM0 ~ 5 (Timer mode supported). Each PWM channel has three modes: Timer mode, PWM mode, and Capture mode. Each mode of each channel is multiplexed with 32-bit counting. The PWM running clock can be either high speed clock or low power clock. Each PWM runs independently with its own duty cycle.

The main features of the PWM module are listed here:

- Fixed PWM base frequency with programmable 1 ~ 256 prescaler
- The counter increases in one direction and continues counting from 0 automatically when it overflows to the maximum value.
- Each channel can be individually enabled, and the mode of each channel can be individually configured.
- Capable of continuous counting between two rising edges, two falling edges or dual edges in Capture mode
- Configurable PWM period and duty-cycle for each PWM channel

- Real-time count value can be read in Timer mode.

4.13.1 Timer Mode

In Timer mode, the counter is enabled and incrementally counted, and an interrupt is generated when the specified cycle value is reached. Counting restarts from 0.

If the software refreshes the count cycle value during the counting process, the new count cycle value is used as the count cycle. If the current count value exceeds the new count cycle value, it immediately goes back to 0 and starts counting again.

The counter resets to 0 immediately if Enable = 0. If Stop = 1, the counter stops incrementing and remains its current state, and continues counting after Stop = 0.

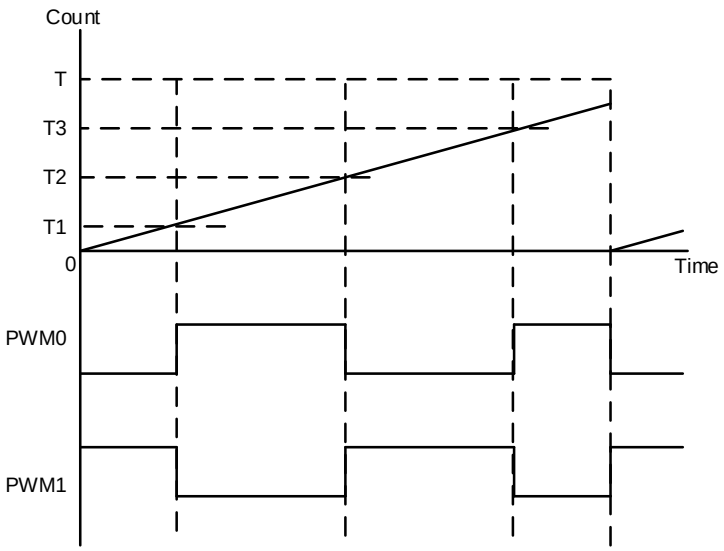
The current count value of the counter can be read in real time.

4.13.2 PWM Mode

In PWM mode, the PWM waveform start level can be configured as 0 or 1. The waveform timing is configured with four parameters.

- Waveform period T (1~2^32)
- The first level inversion time T1 (0~2^32-1, 0 - no inversion)
- The second level inversion time T2 (0~2^32-1, 0 - no inversion)
- The third level inversion time T3 (0~2^32-1, 0 - no inversion)

The six PWM channels can be configured as three pairs, and their start up time is aligned when the adjacent two channels are in paired mode (At this point, the waveform period must be configured to the same value).



As shown in the above figure, PWM0 and PWM1 have opposite start levels, share same waveform parameters, and are in paired mode.

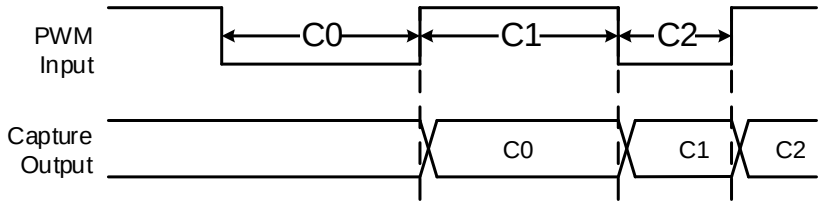
In PWM mode, no interrupts are generated.

During operation, any updates to the configuration parameters will take no effect until the next time the counter starts from 0 again.

4.13.3 Capture Mode

Capture mode, which uses the operating clock to count the time between input signal edges, has the following three modes of edges:

- Rising edge: between two rising edges
- Falling edge: between two falling edges
- Dual edge: between any two edges



The figure above shows the Capture result between dual edges.

Each time there is an update to the Capture output, an interrupt is generated. The software must read out the Capture result before the next update, otherwise the Capture result will be overwritten by the new result.

4.14 Charge Controller

The charge controller supports 120 mA constant charge current. The charge current can be programmed at 1 mA step. After the battery reached an expected voltage threshold, the charge controller will switch to constant voltage charging mode.

4.15 I2S

BK3296 integrates a I2S interface. The I2S interface supports both master and slave mode with sample rates from 8 kHz to 384 kHz.

4.16 Audio Peripherals

BK3296 comes with a rich set of audio peripherals to enhance the Bluetooth listening experience. The chip includes a four-band digital equalizer, two analog-to-digital converters (ADC) and two digital-to-analog converters (DAC).

4.16.1 Four-Band Digital Equalizer

A dedicated four-band digital equalizer is implemented prior to digital-to-analog conversion to give users the option of customizing the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption. The four-band equalizer can be easily configured using the BK3296 software configuration tool kit. For more information, please refer to the BK3296 Software Configuration Tool User Guide.

4.16.2 Audio ADC and DAC

BK3296 contains two high fidelity ADCs with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates high fidelity stereo DACs with sample rates of 8 kHz, 16 kHz, 44.1 kHz or 48 kHz.

4.16.3 Microphone Input Amplifier and Bias

BK3296 contains a fully differential analog microphone input amplifier and a low-noise microphone bias generator. Expensive external components are not needed as the microphone amplifier and active bias circuitry are integrated into the chip, allowing the microphone to interface with passive resistors and capacitors.

The microphone signal can be amplified with gain from 0 to 32 dB with 2 dB step.

4.16.4 Audio Output

BK3296 provides high fidelity stereo audio L/R outputs capable of driving 16 Ω speakers with up to 30 pF of load capacitance.

4.17 General Purpose SAR ADC

BK3296 embeds a 12-bit general-purpose SAR ADC with programmable sampling rates ranging from 5 kHz up to 13 MHz and is used to measure DC and low frequency voltages. The input voltage range for the ADC is from 0 V to 3.6 V.

Table 4-3 SAR ADC Input Channel

Channel Number	Detected Voltage	Description
2	VCC4BAT	Monitor battery voltage (0.25* VCC4BAT)
3	Temperature sensor	Temperature sensor output voltage
4	VCC5USB	Monitor USB voltage (0.5*VCC5USB)
5	GPIO7	GPIO7 voltage
7	GPIO11	GPIO11 voltage
9	GPIO18	GPIO18 voltage
10	GPIO20	GPIO20 voltage

4.18 Timer

BK3296 includes six general-purpose timers, a watchdog timer and a low-power timer.

There are two groups of general-purpose timers, Timer0 and Timer1, and each group has three 32-bit timers. Timer0 (fast) uses 1 MHz clock as the main clock, and Timer1 (slow) uses a 32 kHz clock divided from X26M or derived from ROSC as main clock. Each group has three 16-bit counters with 4-bit pre-divider.

The watchdog timer runs on a 32 kHz clock divided from ROSC and has a maximum programmable period of up to 32.8 (2^16/32 kHz * 16) seconds.

The low-power timer runs on a 125 Hz clock derived from X26M or ROSC. It is used for low-power timing and it can keep running even when the MCU is powered off.

4.19 IrDA Interface

BK3296 embeds a hardware IrDA decoder interface to decode the signal. In addition, the interface has the capture timer capability to allow software decoding of the input signal.

4.20 Temperature Sensor

BK3296 integrates an on-chip temperature sensor. The temperature sensor can measure on-chip temperature over -40 to +125 ℃ with an accuracy of ±3 ℃. The digital results can be read by the ADC.

Usually the software initiates calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce the transmit power or suspend operation at high temperatures.

4.21 Touch Sensor

BK3296 has up to six capacitive-sensing GPIOs, labeled TS0 ~ 5, which detect capacitance changes induced by touch or proximity of objects immediately.

5. Electrical Characteristics

Note: Values currently listed in this section are preliminary measurements and are subject to change.

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VCC4BAT	Battery regulator supply voltage	-0.3	4.5	V
VCC5USB	USB power supply voltage	-0.3	5.75	V
VDDBT	BT transceiver LDO output voltage	-0.3	1.5	V
VDDD	Digital Core LDO output voltage	-0.3	1.05	V
VDDA	Analog LDO output voltage	-0.3	1.5	V
VDDSYS	IO LDO output voltage	-0.3	3.6	V
VDDALON	Always on LDO output voltage	-0.3	1.05	V
VDDFLASH	Power supply of Flash	-0.3	3.6	V
VBATCHG	Charger output	-0.3	4.5	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-40	150	℃

5.2 Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VCC4BAT	Battery regulator supply voltage	2.8	-	4.35	V
VCC5USB	USB power supply voltage	4.75	5.0	5.75	V
VDDBT	BT transceiver supply voltage	1.1	1.2	1.25	V
VDDD	Digital Core LDO output voltage	0.6	0.8	0.95	V
VDDA	Analog LDO output voltage	1.2	1.3	1.5	V
VDDSYS	IO LDO output voltage	2.8	3	3.6	V

Parameter	Description	Min.	Typ.	Max.	Unit
VDDALON	Always on LDO output voltage	0.6	0.8	0.95	V
VDDFLASH	Power supply of Flash	2.8	3.0	3.6	V
VBATCHG	Charger output	2.8	-	4.5	V
MICBIAS	Microphone bias output	1.8	-	2.4	V
T_{OPR}	Operating temperature range	-20	-	85	℃

5.3 Battery Charge

Parameter	Description	Min.	Typ.	Max.	Unit
VCC5USB	Charger input voltage	4.75	5.0	5.75	V
I_trickle	Charge current at trickle mode as percent of fast charge mode	-	10	20	%
I_fast	Charge current at fast charge mode	1	-	120	mA
V_end (Calibrated)	VCC4BAT voltage when charge ends	-	4.2	-	V

5.4 BUCK

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	BUCK output voltage	1.2	1.3	1.5	V
Load current	-	-	-	150	mA
Switching frequency	BUCK modulation frequency	0.5	1	2	MHz

5.5 System LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VCC4BAT	Battery input voltage	2.8	-	4.35	V
VDDSYS	LDO output voltage	2.8	3.0	3.6	V
Load current	-	-	-	150	mA

5.6 Analog LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog LDO output voltage	1.2	1.3	1.5	V
Load current	-	-	-	100	mA

5.7 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital Core LDO output voltage	0.6	0.8	0.95	V
Load current	-	-	-	40	mA

5.8 Crystal and Reference Clock

Parameter	Description	Min.	Typ.	Max.	Unit
Frequency	Crystal and reference frequency	-	26	-	MHz
Tolerance	Crystal and reference frequency tolerance	-10	-	+10	ppm
XI Pin	Input voltage range for reference clock input	-0.3	-	1.05	V

5.9 Current Consumption

Measured with T = 25 ℃, VCC4BAT = 4.0 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
Shutdown	-	-	TBD	-	μA
Deep Sleep	-	-	14	-	μA
Active (A2DP)	2DH5	-	2.8	-	mA
Active (HFP)	HV1	-	TBD	-	mA

5.10 RF Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Frequency range	-	2400	-	2527	MHz
RX Sensitivity	GFSK, 0.1% BER, 1 Mbps	-	-93	-	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	-	-95	-	dBm
	8-DPSK, 0.01% BER, 3 Mbps	-	TBD	-	dBm
Maximum received signal	0.1% BER	-	0	-	dBm
Maximum TX power	GFSK	-	8	-	dBm
	π/4-DQPSK	-	8	-	dBm
	8-DPSK	-	TBD	-	dBm
RF power control range	-	-	60	-	dB

5.11 Audio Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
DAC Diff. Output	With 600 Ohm loading	-	1	-	Vrms
	With 16 Ohm loading	-	0.8	-	Vrms
DAC Diff. Output THD	With 1 Vrms @ 600 Ohm loading	-	-75	-	dB
	With 0.8 Vrms @ 16 Ohm loading	-	TBD	-	dB
DAC output SNR	1 kHz sine wave	-	104	-	dB
DAC Sample Rate	-	8	-	48	kHz
ADC SNR	1 kHz sine wave	-	TBD	-	dB
ADC Sample Rate	-	8	-	48	kHz

6. Package Information

6.1 QFN32 4 x 4 mm Package

Figure 6-1 QFN32 4 x 4 mm Package Outline

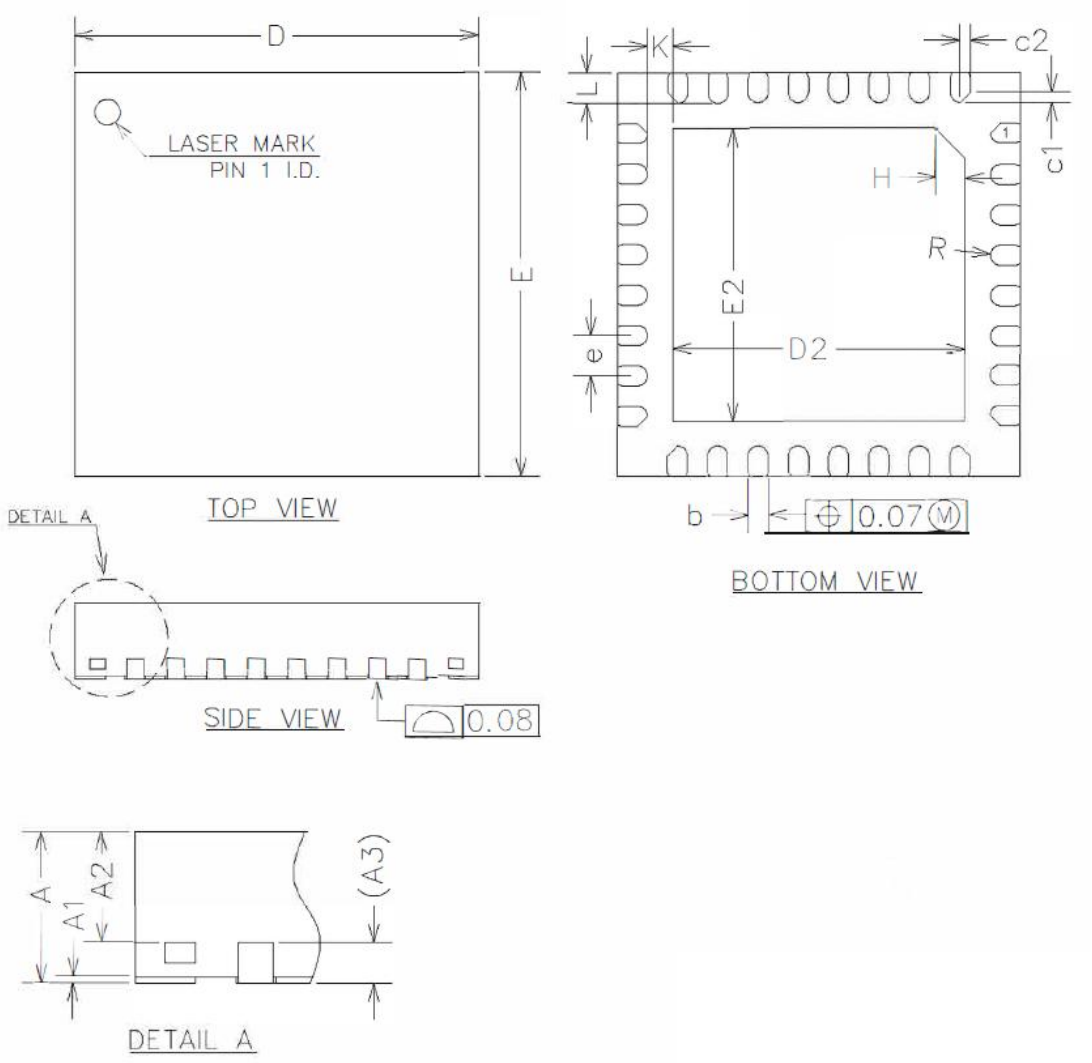


Table 6-1 QFN32 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A2	0.50	0.55	0.60
A3	0.20 REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30 REF		
K	0.25 REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

6.2 QFN20 3 x 3 mm Package

Figure 6-2 QFN20 3 x 3 mm Package Outline

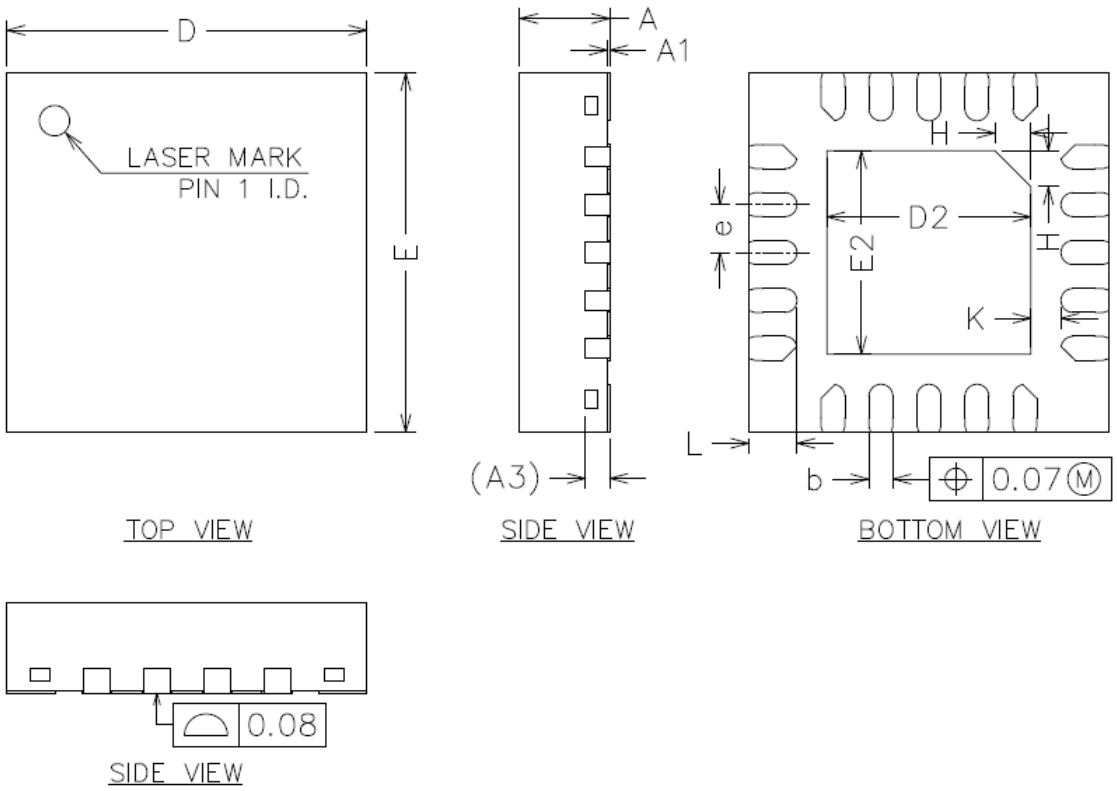


Table 6-2 QFN20 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
e	0.30	0.40	0.50
H	0.30 REF		
K	0.15	-	-
L	0.35	0.40	0.45

7. Ordering Information

Table 7-1 Ordering Information

Part Number	Package	Flash	Operating Temp	Packing	Minimum Ordering Qty (MOQ)
BK3296QN323	4 mm x 4 mm QFN32	Yes	-20 to +85 ℃	Tape and Reel	3000
BK3296QN223	3 mm x 3 mm QFN20	Yes	-20 to +85 ℃	Tape and Reel	3000
BK3296QN213	3 mm x 3 mm QFN20	Yes	-20 to +85 ℃	Tape and Reel	3000

Revision History

Version	Date	Description
0.7	2021/6/7	Initial release. First version of the preliminary specification.
0.8	2021/12/17	• Removed Bluetooth LE 2 Mbps support, added eFuse, updated the maximum operating voltage (VCC4BAT), and updated peripherals in Chapter 1 Features • Updated Chapter 2 Overview • Updated pin assignments and pin descriptions for three packages in Chapter 3 Pin Description • Added clock selection for I2S to Table 4-2 in Section 4.6 Clock • Updated the maximum operating voltage (VCC4BAT) in Section 4.8 Power Management • Updated the description and maximum clock speed for SPI in Section 4.10 SPI • Added Section 4.15 I2S • Corrected the five-band digital equalizer to four-band digital equalizer in Section 4.16 Audio Peripherals and added Section 4.16.3 Microphone Input Amplifier and Bias and Section 4.16.4 Audio Output • Updated the maximum operating voltage (VCC4BAT) in Section 5.2 Recommended Operating Conditions and Section 5.5 System LDO
0.9	2021/12/27	• Updated the description of Bluetooth profiles in Chapter 1 Features • Updated GPIO numbering of 9 GPIOs except for GPIO0 and GPIO1 • Updated the description of ADC and DAC in Section 4.16.2 Audio ADC and DAC

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