



BK1081

FM STEREO TRANSMITTER

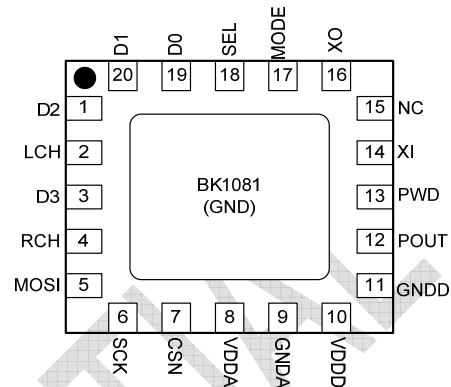
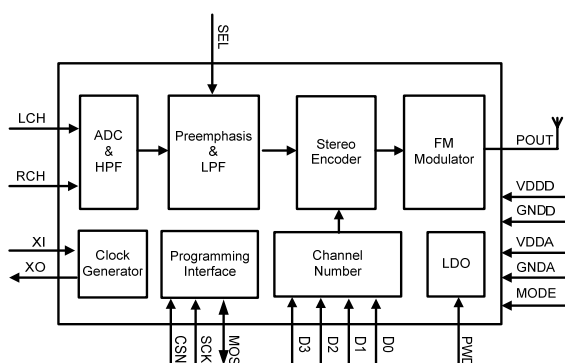
Features

- Support 64~125 MHz band
- Fully integrated PLL
- Digital FM stereo encoder
- 50us/75us pre-emphasis
- Max output power 10dBm
- Output power programmable
- 2.5 ~ 3.6 V supply voltage
- Active current 15 mA
- Wide range reference clock support
- 3-wireSPI or 2-wire I2C interface
- 3x3 mm 20-pin QFN package ,16-pin TSSOP package or 10-pin SSOP

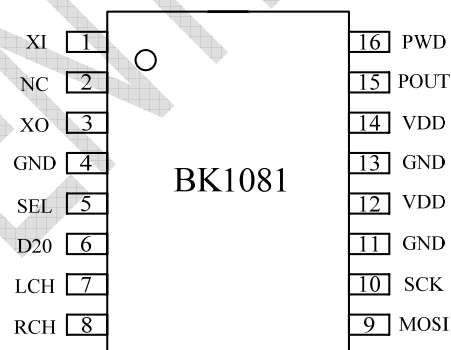
Applications

- MP3 Player
- Wireless Speaker
- Toys

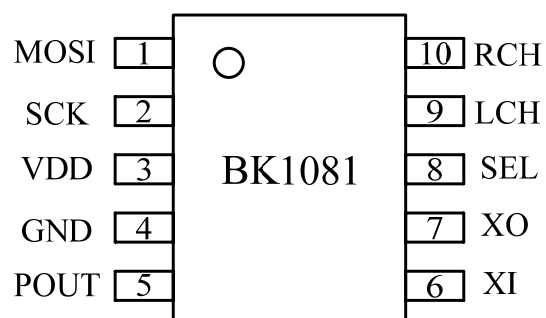
Functional Block Diagram



QFN 20 Pin Assignments (Top View)



TSSOP 16 Pin Assignments (Top View)



SSOP 10 Pin Assignments (Top View)

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2 Functional Description

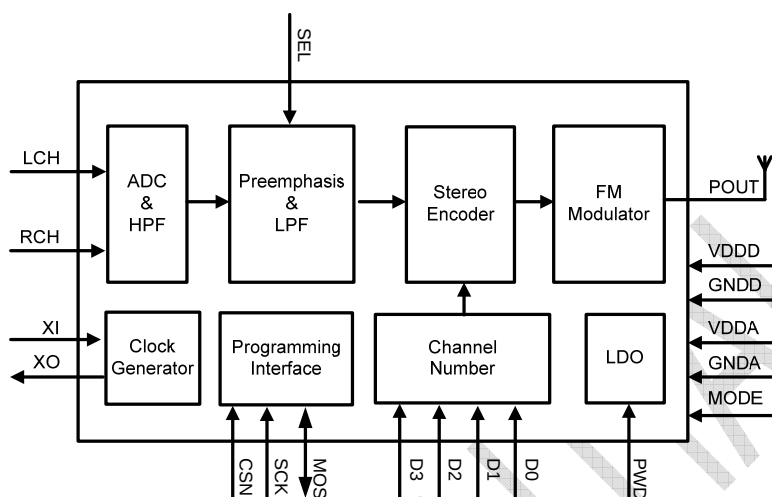


Figure1. Functional Block Diagram

2.1 Power Supply

The BK1081 integrated a regulator which supplies power to the chip. The external supply voltage range is 2.5- 3.6 V.

2.2 Power Down and Reset

BK1081 has already integrated the power on reset circuit inside. The chip power on/down is controlled by programming or pin PWD.

2.3 Pre-emphasis

Pre-emphasis time constant: 50us/75us, it can be selected through SEL pin (0: 50 us, 1: 75 us).

2.4 Stereo Encoder

The stereo encoder is based on signal processing to encode analog stereo audio input signal and generate a composite FM signal with main, sub and pilot signal from the reference clock.

2.5 Channel Number

The BK1081 can select different channel frequency through setting the high level or low level of the channel selection pins. This function is only full available for QFN package chips.

Table 1 [D3, D2, D1, D0] mapping to channel frequency

Channel selection bits	Channel Frequency (MHz)	Channel selection bits	Channel Frequency (MHz)
0	87.7	8	106.7
1	87.9	9	106.9
2	88.1	10	107.1
3	88.3	11	107.3
4	88.5	12	107.5
5	88.7	13	107.7
6	88.9	14	107.9
7	From register	15	From register

2.6 FM modulator

The FM transmitter uses direct frequency synthesis to radiate FM wave to the air by modulating the carrier signal with the composite signal.

2.7 Reference Clock

The BK1081 accepts wide range, from 32.768 kHz to 38.4 MHz, reference clock input to the XI pin. For frequency less than 4 MHz, it must be multiplier of 32.768 KHz. The BK1081 also support crystal oscillator, using XI and XO pins. .

2.8 Programming Interface

The BK1081 supports both 2-wire I2C (MODE=0) and 3-wire SPI (MODE=1) programming interface. Interface clock rate can be up to 20MHz.

BK1081 always latches data at the SCK rising edge and outputs its data at SCK falling edge. For MCU, data should be always written at the falling edge of SCK, and read out at the rising edge of SCK.

2.8.1 3-wire bus mode

When selecting 3-wire mode, user must set MODE = 1.

3-wire bus mode uses SCK, MOSI and CSN pins. A transaction begins when user drives CSN low. Next, user drives an 8-bit command serially on MOSI, which is captured by BK1081 on rising edges of SCK. The command consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

2.8.2 I2C bus mode

When selecting I2C mode, user must set MODE = 0.

I2C bus mode only uses SCK and MOSI pins. A transaction begins with the start condition, which occurs when MOSI falls while SCK is high. Next, user drives an 8-bit device ID serially on MOSI, which is captured by BK1081 at the rising edge of SCK. The device ID of BK1081 is 0x1D.

After driving the device ID, user drives an 8-bit control word on MOSI. The control word consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

For I2C host reading, the host must give an ACK to BK1081 after each byte access, and should give a NACK to BK1081 after last byte read out.

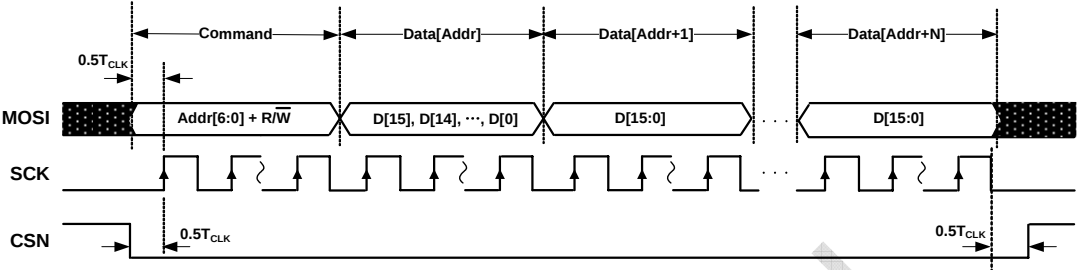


Figure 2 3-wire control interface timing diagram

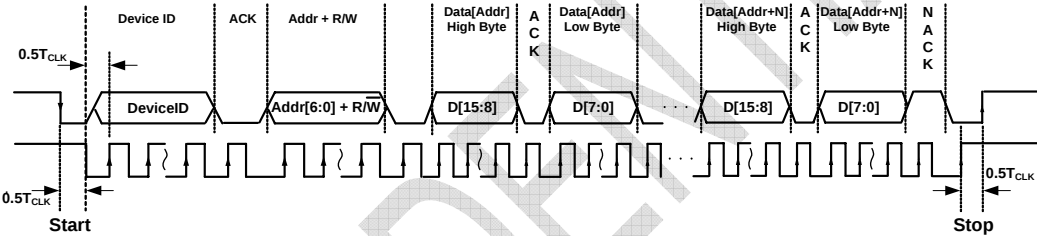


Figure 3 2-wire control interface timing diagram

3 Design Specification

3.1 Recommended Operating Conditions

Table 2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage	V _A	2.5	3.3	3.6	V
Digital Supply Voltage ¹	V _D	2.5	3.3	3.6	V
Interface Voltage Range	V _{IO}	2.5		3.6	V
Supply Current	I _A	-	15	-	mA
Audio input level	V _{IN-A}	-	-	-10	dBV
Audio input frequency range	f _{IN-A}	200	-	15k	Hz
Ambient Temperature	T _{amb}	-40	27	85	°C

3.2 DC Electrical Specification

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V _{IN}	-	-	7	V
Ambient Temperature	T _{amb}	-55	-	125	°C

3.3 Transmitter Characteristics

Table 4 Transmitter Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		64	-	125	MHz
Output power		-16	-	10 ¹	dBm
Pre-emphasis time constant	50us, 75us		50,75		us
Audio SINAD	Mono 22.5 kHz Deviation	-	58	-	dB
Stereo separation		-	36	-	dB
L/R channel balance		-	+/- 0.5	-	dB
Notes:					
1: Measured at 50 ohm loading ,and high output power configuration					

4 Register definition^{1,5}

Register 00h. ChanLSB (WR)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	FL[15:0]	0x86db	LSB 16 bits of frequency setting Frequency = {FH, FL} * 3.8/2 ²¹ Default frequency is 87.7 MHz

Register 01h. ChanMSB (WR)

BIT	NAME	DEFAULT	DESCRIPTION
[15:0]	FH[15:0]	0x02e2	MSB 16 bits of frequency setting Used together with FL to program channel

Register 02h. Configuration1 (WR)

BIT	NAME	DEFAULT	DESCRIPTION
[15:13]	GAIN[2:0]	1	Digital Gain Control 1 to 1.875 , 0.125/step
[12]	BYP_EM	0	Bypass Pre-emphasis Filter 0: Enable filter 1: Bypass filter
[11]	RESERVED	0	Reserved Do not write anyway
[10]	MONO	0	Mono or Stereo Selection 0: Stereo 1: Mono
[9:4]	AUD_DEV[5:0]	2e	Audio Deviation Adjust Default is 75kHz ²
[3:0]	PILOT_DEV[3:0]	3	Pilot Deviation Adjust Default is 7.5kHz

Register 03h. Configuration2 (WR)

BIT	NAME	DEFAULT	DESCRIPTION
[15:4]	RESERVED	0	Reserved Do not write anyway
[3:0]	POUT[3:0]	7	Output Power Control ^{3,4} 0: -16 dBm; 1: -10 dBm; 3: -5 dBm; 7: 0 dBm

Register 04h/05h. Configuration3 (W)

BIT	NAME	DEFAULT	DESCRIPTION
[31:28]	PA_LOAD[3:0]	0x8	PA Load Adjust
[27:26]	RESERVED	0	Reserved Do not write anyway
[25]	PWD_PLL	0	Power down PLL 0 : Power on; 1: Power down
[24]	PWD_PA	0	Power down PA 0: Power on; 1: Power down
[23]	RESERVED	0	Reserved Do not write anyway
[22:20]	MICGAIN[2:0]		Microphone Gain Control 0: 0dB 1: 2dB 2: 4dB 3: 6dB 4: 8 dB 5: 10dB 6: 12 dB 7: 14dB
[19:10]	RESERVED	0x384	Reserved. Do not write anyway
[9]	RESERVED	0	Reserved. Do not write anyway
[8:6]	RESERVED	0x3	Reserved. Do not write anyway
[5]	PWD_AUD	0	Power Down Audio 0: Power on; 1: Power down
[4]	PWD_ADC	0	Power Down ADC 0: Power on; 1: Power down
[3:2]	RESERVED	0	Reserved Do not write anyway
[1]	PWD_G	0	Global Power Down 0: Power on; 1: Power down
[0]	PWD_CB	0	Power Down Central Bias 0: Power on; 1: Power down

Register 06h/07h. Configuration4 (W)

BIT	NAME	DEFAULT	DESCRIPTION
[31:18]	RESERVED	0x08e6	Reserved Do not write anyway
[3:0]	XTAL_SEL[17:0]	0x039fc	Reference Clock Programming XTAL_SEL[17:0] = HEX Ref Frequency/512+0.5 Default reference is 7.6MHz

Notes

1. Don't write or read any register not listed in above table such as register which address is greater than 5; Do not try to write the reserved bits listed in the table;
2. -10 dBv single channel audio input, with default digital gain
3. Measured at low output power configuration mode
4. For high power output configuration, refer to "BK1081 Application Notes"
5. Registers with address equal or greater than 4 must be wrote with continuous 32 bit (MSB to LSB) at once R/W access

5 Pin Descriptions

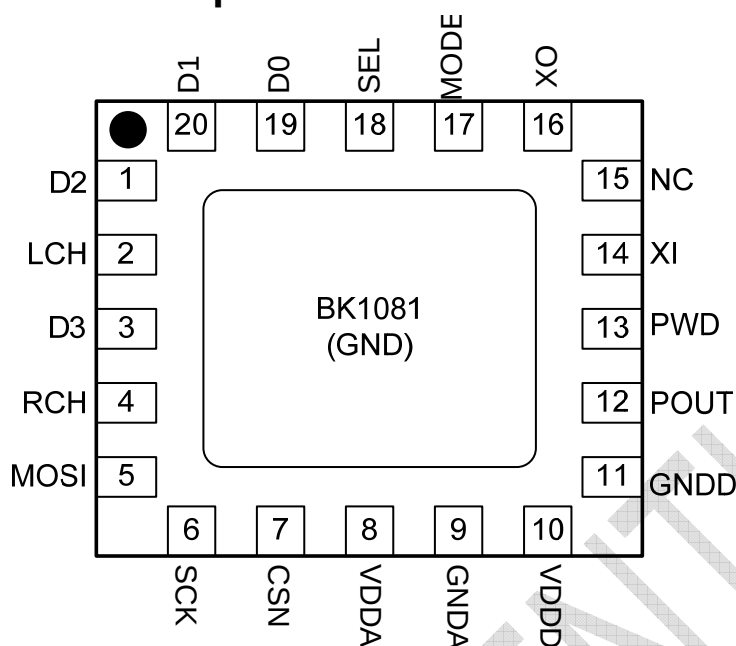


Figure 4 Pin Assignment for BK1081 QFN20 3x3 mm package (top view)

Table 5 BK1081 QFN20 pin assignment

Pin Number(s)	Name	Type	Description
1	D2	I	Channel selection bit
2	LCH	I	Left channel input
3	D3	I	Channel selection bit
4	RCH	I	Right channel input
5	MOSI	IO	SPI data input or I2C data IO, selected by MODE pin
6	SCK	I	SPI clock input or I2C clock input, selected by MODE pin
7	CSN	I	SPI enable
8	VDDA	P	Power for analog
9	GNDA	G	Ground for analog
10	VDDD	P	Power for digital
11	GNDD	G	Ground for digital
12	POUT	RF	RF output
13	PWD	I	Power down enable
14	XI	I	Crystal input
15	RST	I	Reset, active low
16	XO	O	Crystal output
18	MODE	I	I2C or SPI interface selection
19	D0	I	Channel selection bit
20	D1	I	Channel selection bit

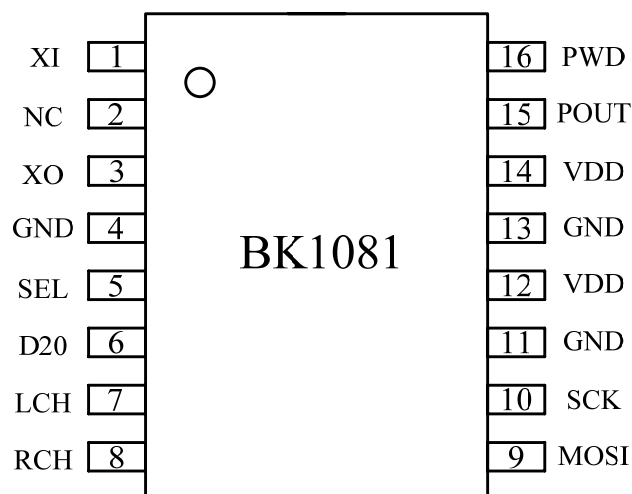


Figure 5 Pin Assignment for BK1081 TSSOP16 package (top view)

Table 6 BK1081 TSSOP16 pin assignment

Pin Number(s)	Name	Type	Description
1	XI	I	Crystal input
2	RST	I	Reset, active low
3	XO	O	Crystal output
4	GND	G	Ground
5	SEL	I	Pre-emphasis time constant selection
6	D20 ¹	I	Channel selection bit
7	LCH	I	Left channel input
8	RCH	I	Right channel input
9	MOSI ²	IO	I2C data IO
10	SCK	I	I2C clock input
11	GND	G	Ground
12	VDD	P	Power
13	GND	G	Ground
14	VDD	P	Power
15	POUT	RF	RF output
16	PWD	I	Power down enable

Notes:

1. Pin D2, D1, D0 of QFN20 is bond together and named D20 at TSSOP16. Pin D3 of QFN20 is bond to ground.
2. Only I2C mode is supported by TSSOP16 package.

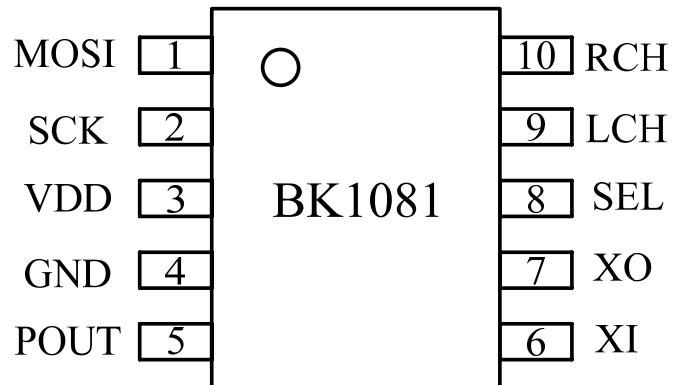


Figure6 Pin Assignment for BK1081 SSOP16 package (top view)

Table 7 BK1081 SSOP10 pin assignment

Pin Number(s)	Name	Type	Description
1	MOSI	IO	I2C data IO
2	SCK	I	I2C clock input
3	VDD	P	Power
4	GND	G	Ground
5	POUT	RF	RF output
6	XI	I	Crystal input
7	XO	O	Crystal output
8	SEL	I	Pre-emphasis time constant selection
9	LCH	I	Left channel input
10	RCH	I	Right channel input

Notes:

1. Only I2C mode is supported by SSOP10 package.
2. Channel setting and power down can only be access by programming.

6 Typical Application Schematic

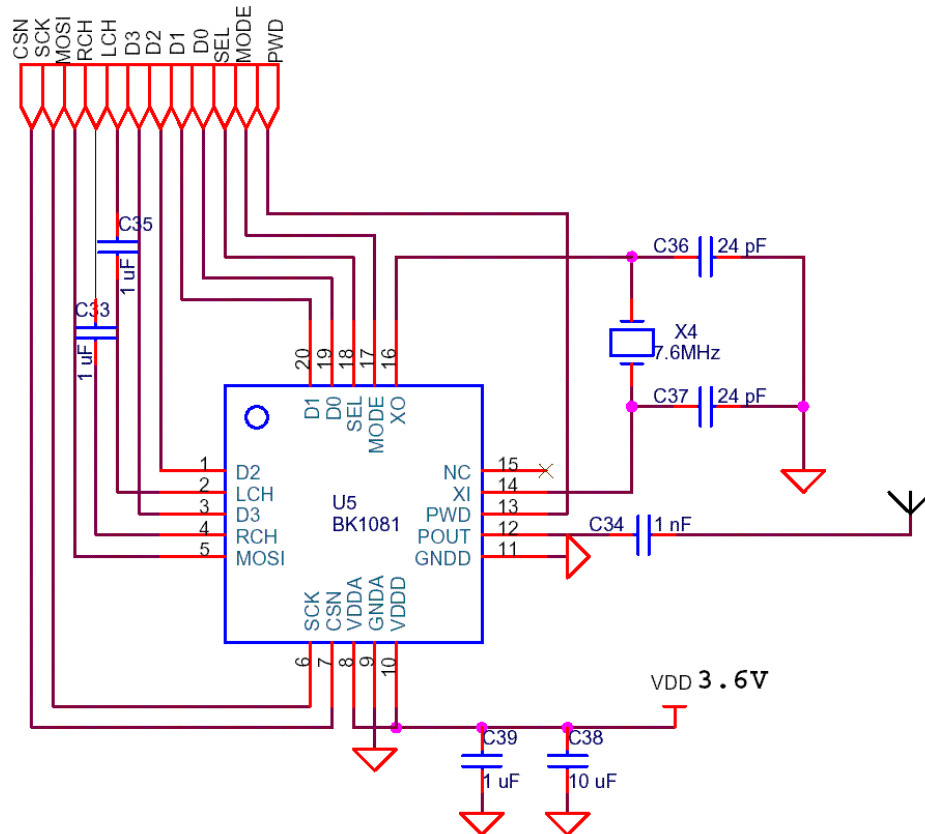


Figure 7. BK1081 QFN20 Typical Application Schematic

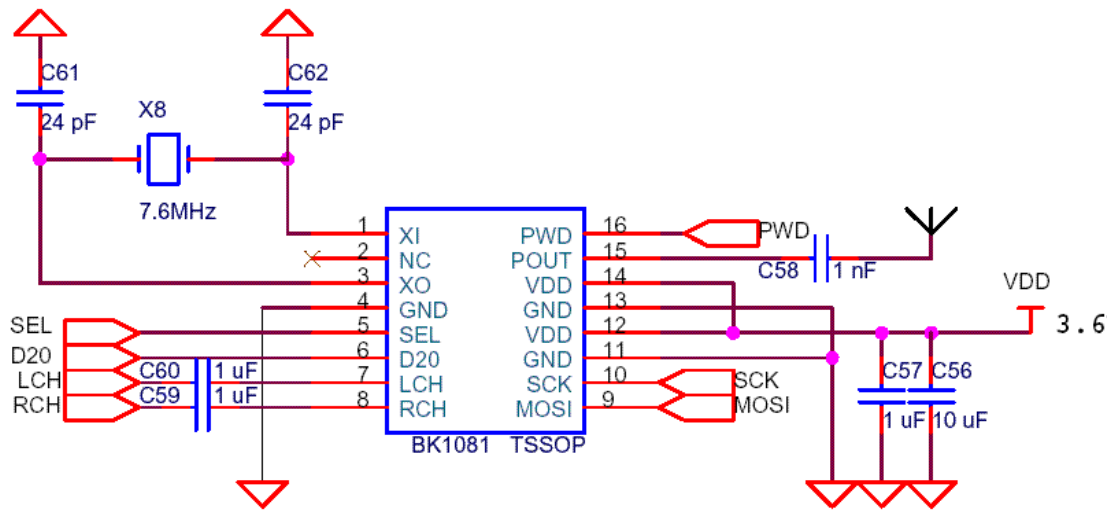


Figure 8. BK1081 TSSOP16 Typical Application Schematic

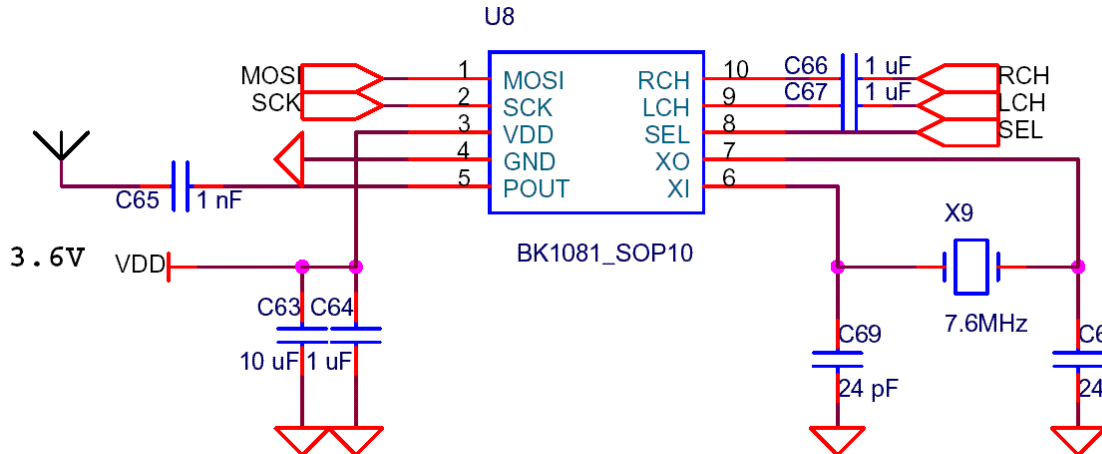


Figure 9. BK1081 SSOP10 Typical Application Schematic

Note: More application schematic, refer to "BK1081 Application Notes"

7 Package Information

QFN 3x3 20pin , TSSOP 16 pin and SSOP 10 pin packages are available for BK1081.
Detail information of the package follows:

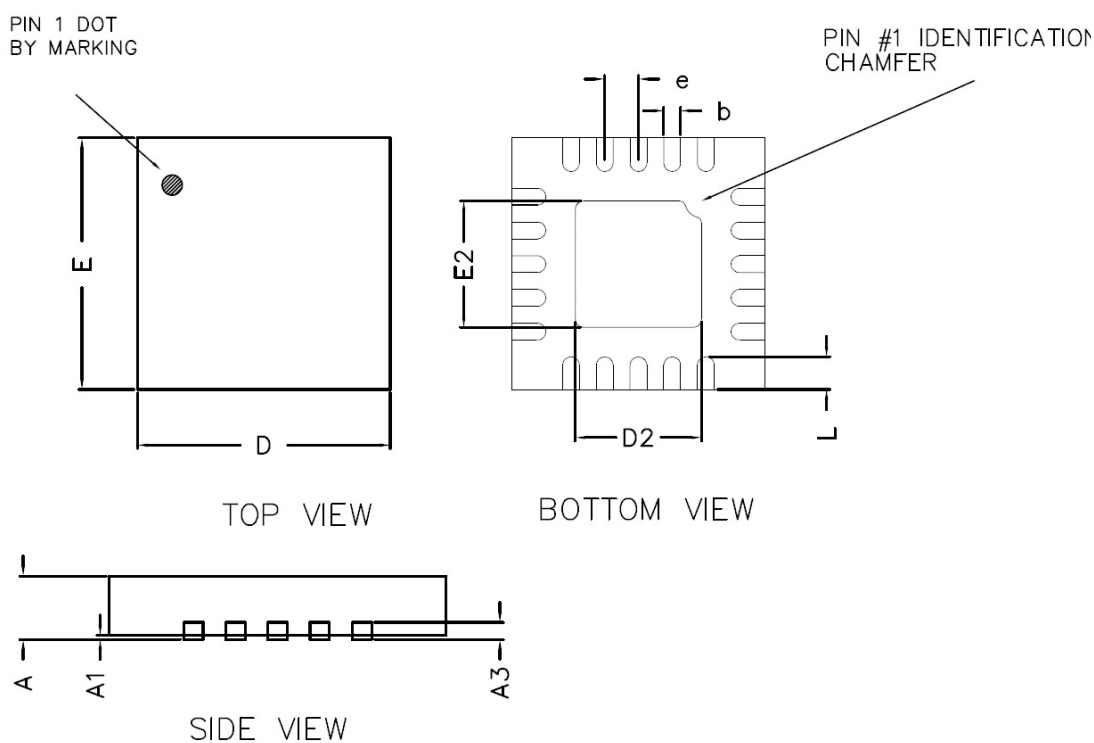


Figure10 QFN20 Pin Package diagram

Table 8 QFN 3x3 20 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	-	0.05	mm
A3	0.20 REF			mm
D	2.95	3.00	3.05	mm
E	2.95	3.00	3.05	mm
b	0.15	0.20	0.25	mm
L	0.30	0.40	0.50	mm
D2	1.35	1.50	1.60	mm
E2	1.35	1.50	1.60	mm
e	0.40 REF			mm

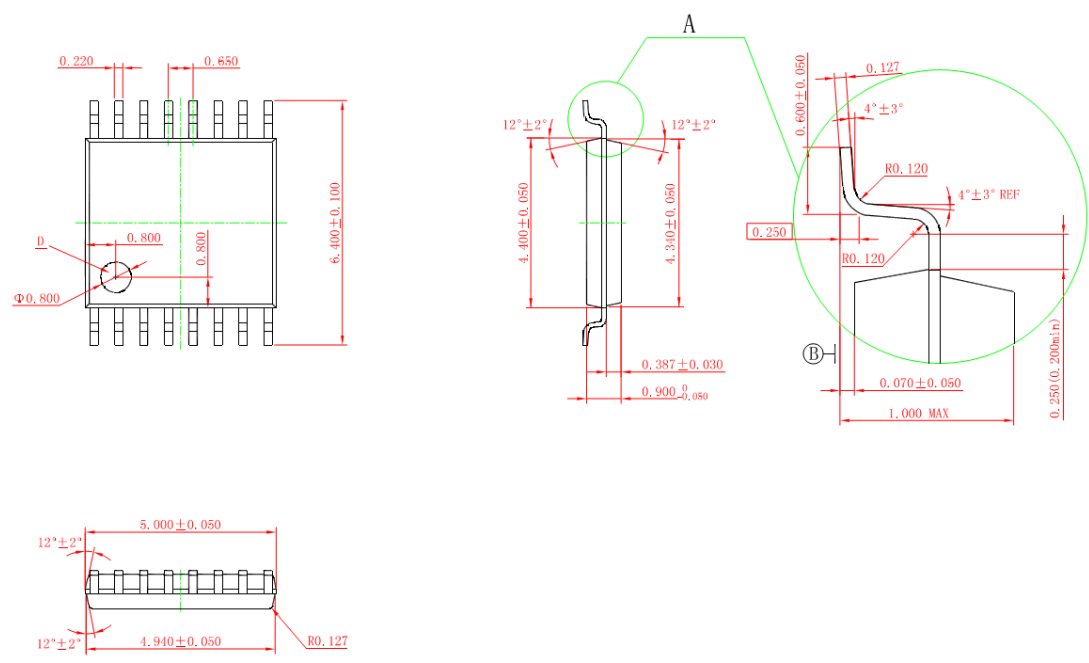


Figure 11 TSSOP 16 Pin Package diagram

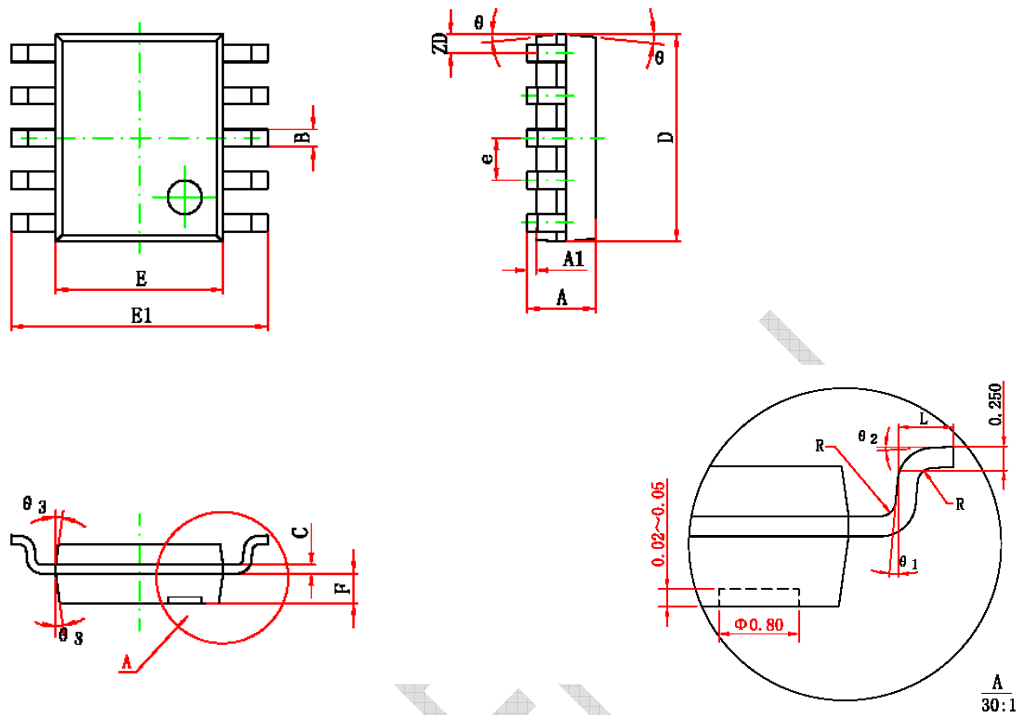


Figure 12 SSOP 10 Pin Package diagram

Table 9 SSOP 10 Pin Package dimensions

Parameter	Min	Typ	Max	Unit
A	1.570	1.650	1.730	mm
A1	0.150	0.200	0.250	mm
B		0.350		mm
C		0.203		mm
E	3.890	3.940	3.990	mm
E1	5.960	6.040	6.120	mm
F	0.750	0.7	0.750	mm
L	0.550	0.600	0.650	mm
R		0.150		mm
D	4.800	4.900	5.000	mm
ZD		0.450		mm
e		1.000		mm
θ		7°		
θ 1		7°		
θ 2	0°		8°	
θ 3		7°		

8 Order Information

Table 10 BK1081 order information

Part number	Package	Packing	MOQ (ea)
BK1081TB	TSSOP16	Tape Reel	3k
BK1081QB	QFN3*3 20L	Tape Reel	3k
BK1081SB	SSOP10	Tape Reel	3k

Remark:

MOQ: Minimum Order Quantity

9 Additional Reference Resource

- BK1081 Application Notes

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10 Revision History

Version	Change Summary	Data	Author
Rev.0.1	Initial draft	23-12-2009	JW

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