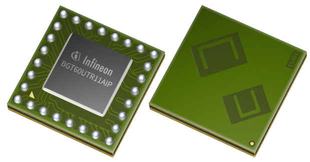
BGT 60UTR11AIP
60 GHz radar sensor with antennas in package



RoHS
Halogen-free

Features

- Integrated state machine for low-power and real time operation
- Broadcast mode to trigger and configure multiple devices
- Single 50 MHz SPI for chip configuration and data transfer
- 60 GHz radar with 5.6 GHz bandwidth and a chirp slope of up to 400 MHz/µs
- 4 MSps ADC
- Antenna in package (AIP) with ±60° FoV

Potential applications

- Presence detection and range zones segmentation for smart home and doorbell applications
- Vital sign tracking for health care devices, such as sleep trackers and baby monitors
- 1D gesture sensing for smart appliances such as kitchen machines or thermostats
- Distance measurement and level sensing

Product validation

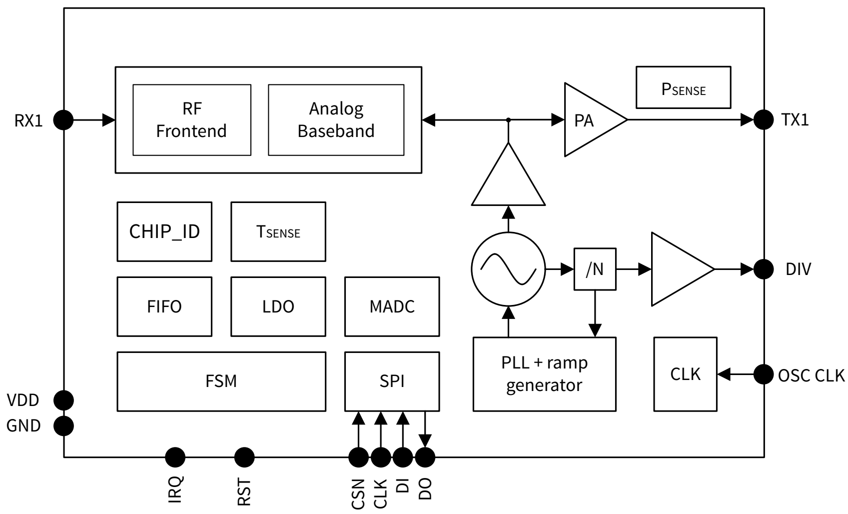
Qualified for applications listed above based on the test conditions in the relevant tests of JEDEC20/22.

Description

The BGT60UTR11AIP is a 60 GHz radar sensor with 1 transmitting and 1 receiving U-slotted patch antennas in package. The 5.6 GHz ultra-wide bandwidth allows FMCW operations with extremely high resolution. This enables precise range measurements, 1D gestures and also the measurement of vital signs such as breathing rate or heart rate.

Sensor configuration and data transfer are enabled with a single digital interface. Multiple devices connected to the same bus can be configured and triggered together by using the implemented broadcast mode. Device specific programmable wake-up times allow time domain multiplexed radar frames.

The integrated state machine enables independent and real time data acquisition without interaction to the processor. Three possible power mode options give the user full flexibility between performance and power consumption optimizations.



Product Name	Package	Marking type
BGT 60UTR11AIP	PG-VF2BGA-28-1	611A

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1 Introduction

Smart sensors can be based on radar systems, in special case, *frequency-modulated continuous wave (FMCW)* radars. Those systems can comprise several blocks: *radio frequency (RF)* front-end, *analog base band (ABB)*, *analog-to-digital converter (ADC)*, *phase-locked loop (PLL)*, memory (*first in first out (FIFO)*), *serial peripheral interface (SPI)* and antennas. Smart sensors require a high level of integration, thus, the components listed above should be integrated in a single chip solution. BGT60UTR11AIP offers this level of integration in a single chip.

1.1 Product overview

The core functionality of BGT60UTR11AIP is to transmit frequency-modulated continuous wave signal through the *transmitter (TX)* channel and receive the echo signal from the target object on the *receiver (RX)* channel. The receiver path includes a baseband filtering, a *variable gain amplifier (VGA)*, as well as an *ADC*. The digitized output is stored in a *FIFO* based memory. The data are transferred to an external host, *microcontroller unit (MCU)* or *application processor (AP)*, to run radar signal processing. A typical implementation of a sensor system consists of two main blocks:

- Radar sensor (BGT60UTR11AIP) handles the *RF* signals and provides the sampled *intermediate frequency (IF)* signals
- AP or microcontroller unit which captures and processes the digital radar signals

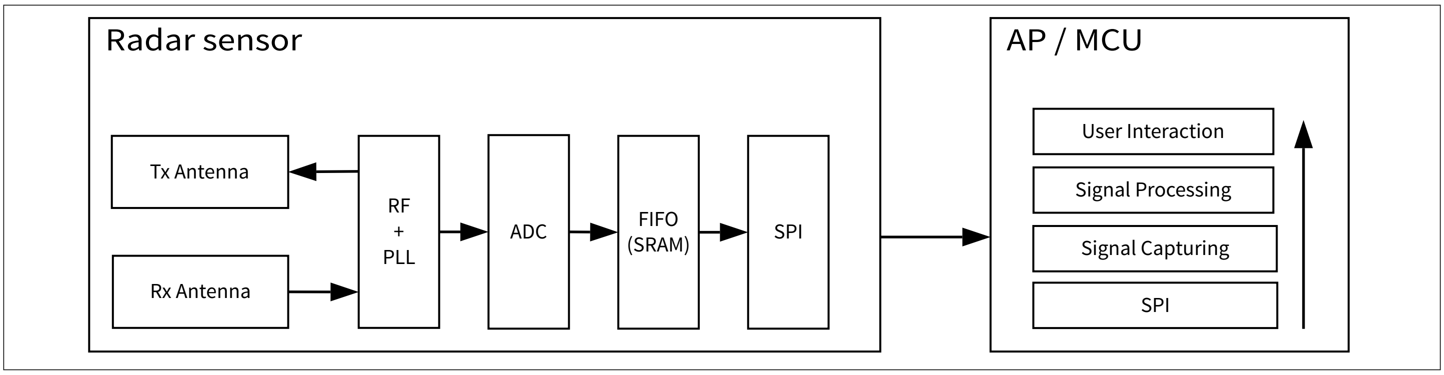

Figure 2 Data flow in the complete radar sensor system

1.2 BGT60UTR11AIP block diagram

BGT60UTR11AIP block diagram is presented in the following figure.

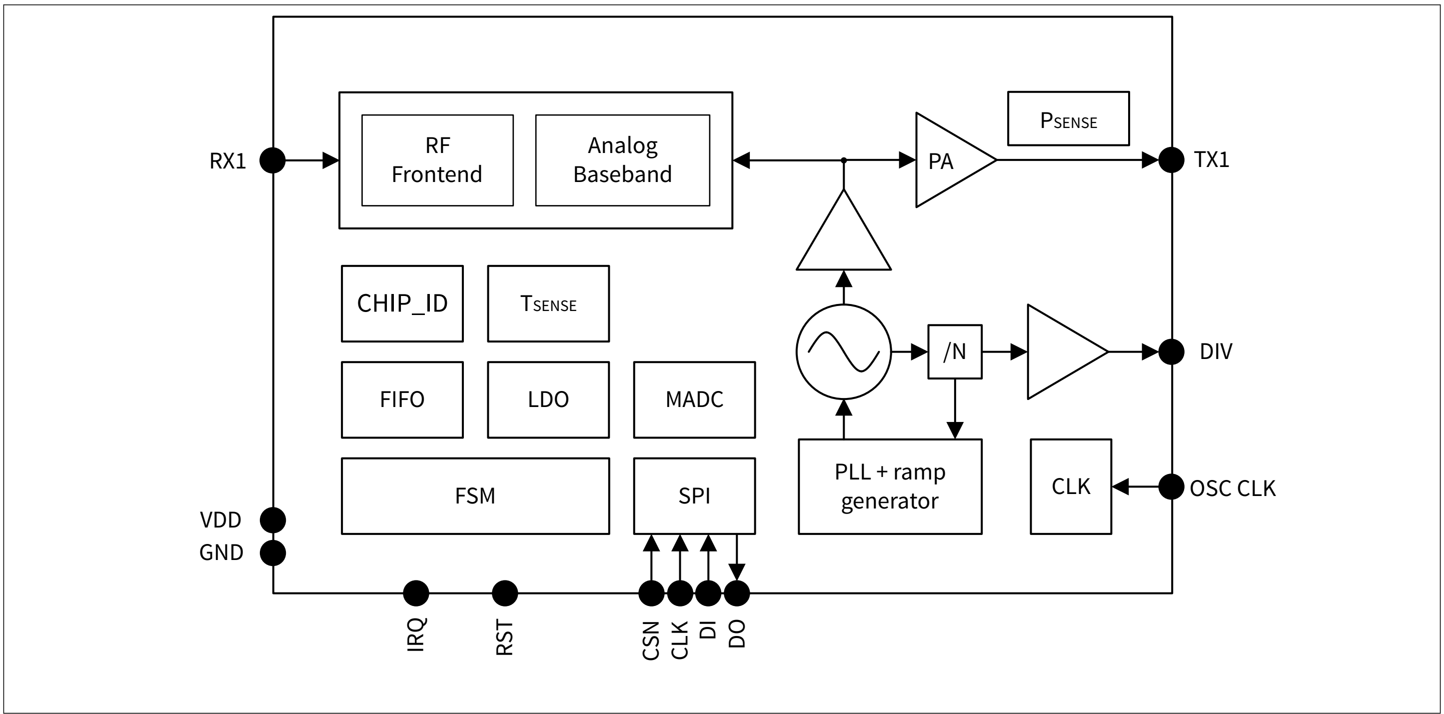

Figure 3 **BGT60UTR11AIP block diagram**

Feature list:

- Single supply voltage level of 1.8 V for both, digital and analog domains
- Integrated *low-dropout voltage regulator (LDO)* to supply the digital domain
- Separated 3.3 V supply for loop filter
- RF-Frontend at 60 GHz covering frequencies from 57.4 to 63.0 GHz with 1 TX and 1 RX channels
- Baseband chain consisting of *high-pass filter (HPF)*, low noise *VGA*, and *anti-aliasing filter (AAF)*
- 1 *ADC* channel with 12 bits resolution and up to 4 MSps sampling rate to sample the RX-IF channel
- Integrated RF *PLL*, timers, counters and a *finite state machine (FSM)* to run sets of frames in standalone mode (no communication with *AP* or microcontroller unit required except first trigger and raw data transfer)
- Full duplex *FIFO* structure as data buffer (49 kbit = 2048 words x 24 bits)
- Standard *SPI* mode for configuration and status register read accesses
- Dedicated power modes for power reduction
- An external 38.4/40/76.8/80 MHz reference oscillator can be used as a system clock source
- An internal frequency doubler is used in case the input clock is 38.4/40 MHz
- *built-in test equipment (BITE)* for *end of line (EOL)* test in production at Infineon to verify *RF* performance
- *linear feedback shift register (LFSR)* test pattern generator on chip for data transfer check
- Fabricated with BiCMOS Infineon process technology
- Housed in a laminate package
- Antennas integrated in the package
- 48 bits for unique CHIP ID for each device

1.3 BGT60UTR11AIP pin definition and function

The following figure shows the transparent top view of the BGT60UTR11AIP laminate package with the pin and antenna number assignment.

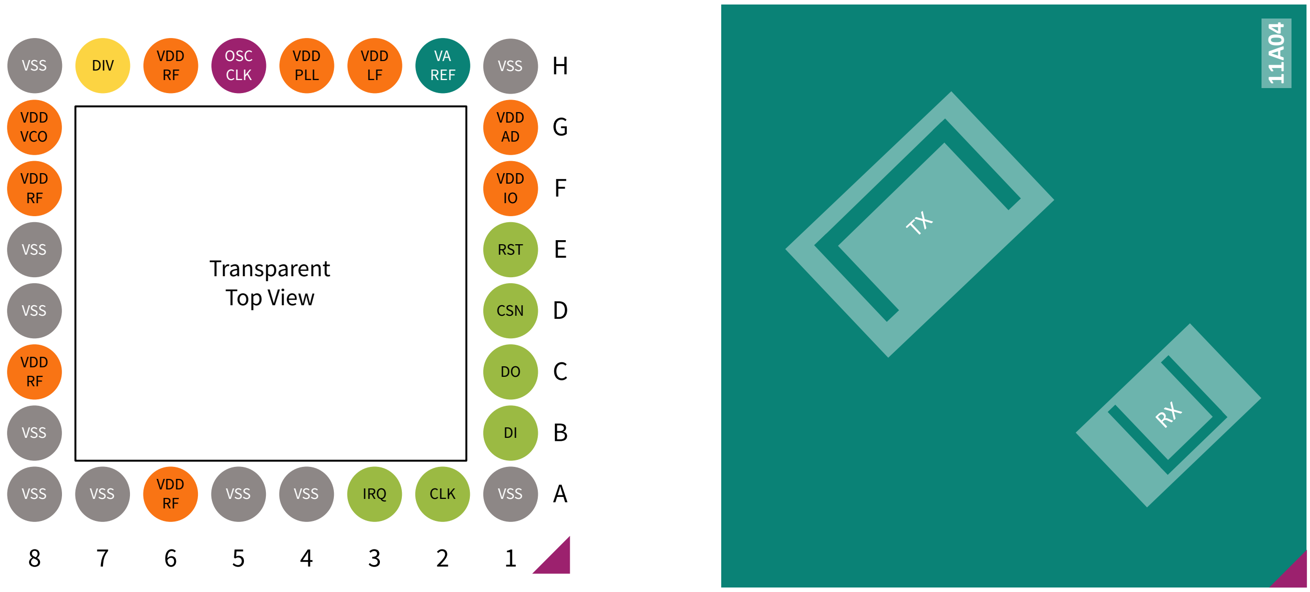

Figure 4 **BGT60UTR11AIP pin and antenna number assignment**

The function of each pin is described in the following tables.

Table 1 **Ball definition**

Ball	Function
A1, A4, A5, A7, A8, B8, D8, E8, H1, H8	VSS_{RF}, VSS_{A}, VSS_{D}
A2	CLK
A3	IRQ
B1	DI
C1	DO
D1	CSN
E1	RST
F1	VDD_{IO}
A6, C8, F8, H6	VDD_{RF}
G1	VDD_{AD}
G8	VDD_{VCO}
H2	V_{AREF}
H3	VDD_{LF}
H4	VDD_{PLL}
H5	OSC_CLK
H7	DIV

Table 2 **Antenna definition**

Antenna	Function
TX1	Transmitter 1
RX1	Receiver 1

1.3.1 IO and supply pins

The following table gives an overview on the input/output pins of BGT60UTR11AIP.

Abbreviations:

- V_{IN}: voltage input pin
- V_{OUT}: voltage output pin
- D_{IN}: digital input pin
- D_{OUT}: digital output pin
- A_{IN}: analog input pin
- A_{OUT}: analog output pin
- GND_D: digital ground connection
- GND_A: analog ground connection

Table 3 **BGT60UTR11AIP input/output pins**

Symbol	Type	Domain	Description	Type
DIV	A_{OUT}	VDD_{RF}	VCO divided by 16 output	Analog
OSC_CLK	A_{IN}	VDD_{RF}	Oscillator input	Analog
CLK	D_{IN}	VDD_{IO}	SPI clock input	Digital
CSN	D_{IN}	VDD_{IO}	SPI chip select input, active low	Digital
DI	D_{IN}	VDD_{IO}	SPI signal from the host output (MOSI)	Digital
DO	D_{OUT}	VDD_{IO}	SPI signal to the host input (MISO)	Digital
RST	D_{IN}	VDD_{IO}	Hardware reset pin	Digital
IRQ	D_{OUT}	VDD_{IO}	Interrupt output	Digital

The power supply pins are described in the following table.

Table 4 **BGT60UTR11AIP supply pins**

Domain	Type	Value	Description	Domain
VDD_{AD}	V_{IN}	1.8 V	Analog and digital supply voltage	Analog-ADC, Digital
VDD_{IO}	V_{IN}	1.2 V 1.8 V	IO pad supply voltage	IO
V_{AREF}	V_{OUT}	1.2 V	Positive reference voltage output; for bypass cap	Analog-ADC
VDD_{VCO}	V_{IN}	1.8 V	Analog supply voltage to the VCO	Analog-RF
VDD_{RF}	V_{IN}	1.8 V	Analog supply voltage	Analog-RF

(table continues...)

Table 4 (continued) BGT60UTR11AIP supply pins

Domain	Type	Value	Description	Domain
VDD_{LF}	V_{IN}	3.3 V	Analog supply voltage for the level shifter for the PLL loop filter	Analog-RF
VDD_{PLL}	V_{IN}	1.8 V	Analog supply voltage to the PLL	Analog-RF
VSS_{RF}	GND_A	0 V	Analog ground connection	Analog-RF
VSS_A	GND_A	0 V	Analog ground connection	Analog-ADC
VSS_D	GND_D	0 V	Digital ground connection	Digital

1.4 BGT60UTR11AIP functional block diagram

BGT60UTR11AIP consists of some main functional blocks:

- *FSM* which manages the complete chip
- Register banks, see Chapter 4
- *FIFO*, 49 kbit = 2048 words x 24 bits
- *SPI*, up to 50 MHz clock
- Two clock domains
  - system clock domain for example 38.4/40/76.8/80 MHz for *PLL*, *ADC* and FIFO
  - SPI clock for example 50 MHz
- PLL, 3rd order sigma-delta based to perform *FMCW* ramp
- *RF* frontend consisting of 1 *RX* channel, 1 *TX* channel, *local oscillator (LO)* generation and divider by 4/5, see Chapter 7.1
- *ABB* consisting of *HPF*, *VGA* and *AAF*, see Chapter 7.2
- 1 channel multi ADC, 12 bits differential SAR ADC interfaced to the ABB via a driver and to the FIFO via a multiplexer, see Chapter 8
- Antenna built in package, see Chapter 11

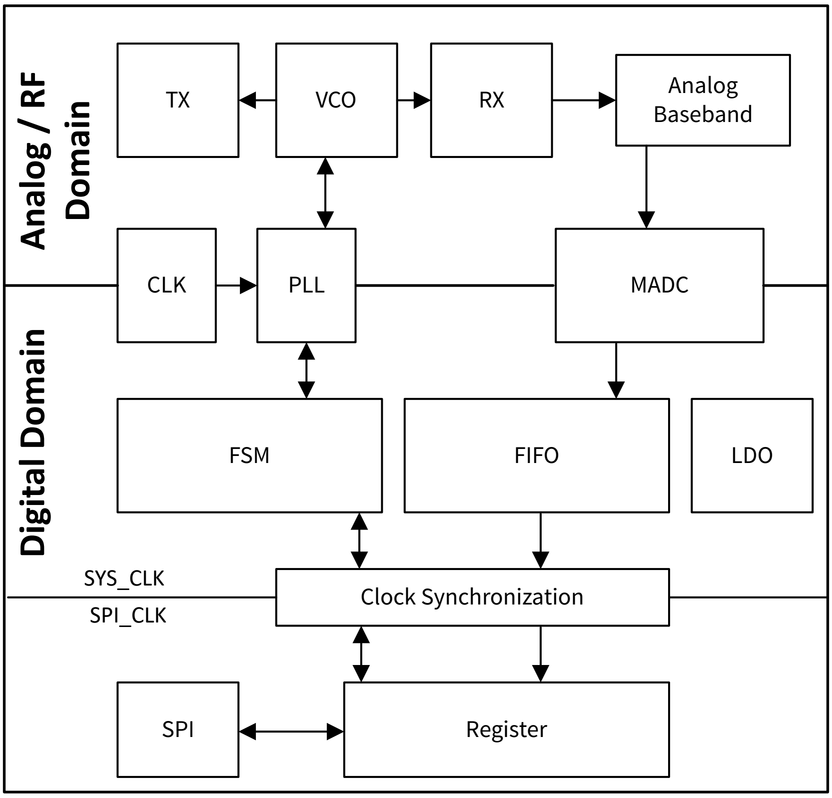

Figure 5 BGT60UTR11AIP functional overview

2 General product specification

The reference for all specified data is the Infineon application board, available on request.

2.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

T_b = -40 °C to 105 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Parameters not subject to production test.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	VDD_{AD}	-0.3	-	+2.0	V	-
Supply Voltage	VDD_{IO}	-0.3	-	+2.0	V	-
Supply Voltage	VDD_{RF}	-0.3	-	+2.0	V	-
Supply Voltage	VDD_{VCO}	-0.3	-	+2.0	V	-
Supply Voltage	VDD_{PLL}	-0.3	-	+2.0	V	-
Supply Voltage	VDD_{LF}	-0.3	-	+3.7	V	-
RF Input Power Level	P_{RF}	-	-	+10	dBm	At the RX input pad (die)
Junction Temperature	T_j	-40	-	+125	°C	-
Storage Temperature	T_{stg}	-40	-	+150	°C	-

Warning: ***Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.***

2.2 Range of functionality

Table 6 Range of functionality

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	VDD_{AD}	1.71	1.8	1.89	V	Noise on each supply domain should not exceed the level of 20 µVpp in the frequency range 20 kHz - 1 MHz[1]
Supply Voltage	VDD_{IO}	1.14 1.71	1.2 1.8	1.26 1.89	V	
Supply Voltage	VDD_{RF}	1.71	1.8	1.89	V	
Supply Voltage	VDD_{VCO}	1.71	1.8	1.89	V	
Supply Voltage	VDD_{PLL}	1.71	1.8	1.89	V	
Supply Voltage	VDD_{LF}	2.5	3.3 [2]	3.63	V	

(table continues...)

Table 6 (continued) Range of functionality

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Chip Backside Temperature	T_b	-20	-	70	°C	Measured with the on-chip temperature sensor
Frequency Range	f_{RF}	57.4	-	63.0	GHz	-
Oscillator Input Clock Frequency	f_{OSC_CLK}#1	75	80	85	MHz	1.8 V CMOS clock 78 MHz not allowed (frequency doubler disabled)
	f_{OSC_CLK}#2[3)]	37.5	40	42.5	MHz	1.8 V CMOS clock 39 MHz not allowed (frequency doubler enabled)
Duty cycle of f_{OSC_CLK}	f_{DUTOSC}	45	50	55	%	-
Rise and Fall Time of f_{OSC_CLK}	$t_{RS,FS,SYS}$	-	2	6	ns	-
Phase Jitter of f_{OSC_CLK}	J_{PHOSC}	-	1	-	ps	*BW*: 12 kHz to 20 MHz

1) This value will ensure no artifact/false target in the Range-Doppler map when it is calculated with a minimum of 8 chirps.
2) Specified maximum bandwidth requires at least VDD_{LF} = 3.3 V.
3) In case f_{OSC_CLK}#2 is used as input clock, an internal doubler will be used to multiply the input frequency by two. The doubler duty-cycle can be calibrated. See PLL interfaces and clock distribution, Reference clock distribution.

2.3 Current consumption

Table 7 Overall current consumption

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Idd Deep Sleep[1)]	Idd_{DS}	0.05	0.178	0.555[2)]	mA	
Idd Idle[3)]	Idd_{Idle}	-	1.8	-	mA	-
Idd Init0, 1RX + 1TX	Idd_{Init0}	-	3.2	-	mA	-
Idd Init1, 1RX + 1TX[4)]	Idd_{Init1}	-	149	-	mA	-
Idd Active, 1RX + 1TX[5)]	Idd_{Active}	110	174	220	mA	-

1) All registers in reset mode, f_{SYS_CLK} clock path disabled.
2) The value at maximum refers to the maximum temperature, +70 °C, and the maximum supply, 1.89 V.
3) MADC band gap running.
4) Idd for the rest of interchirp similar to Init1.
5) Device set in radar mode; DAC TX set to 31_D.

Table 8 ***VDD_{AD}* domain current consumption**

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V, VDD_{IO}= 1.14 V to 1.26 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Idd Deep Sleep[1)]	$ADIdd_{DS}$	0.05	0.147	0.490[2)]	mA	-
Idd Idle[3)]	$ADIdd_{Idle}$	-	2.0	-	mA	-
Idd Init0, 1RX + 1TX	$ADIdd_{Init0}$	-	2.5	-	mA	-
Idd Init1, 1RX + 1TX[4)]	$ADIdd_{Init1}$	-	3.3	-	mA	-
Idd Active, 1RX + 1TX[5)]	$ADIdd_{Active}$	2.1	3.3	6.2	mA	-

1) All registers in reset mode, f_{SYS_CLK} clock path disabled.
2) The value at maximum refers to the maximum temperature, +70 °C, and the maximum supply, 1.89 V.
3) MADC band-gap running.
4) Idd for the rest of interchirp similar to Init1.
5) Device set in radar mode, FIFO in low power mode, DAC TX set to 31_D for an output power of +5 dBm.

Table 9 ***VDD_{PLL}* domain current consumption**

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Idd Deep Sleep[1)]	$PLLIdd_{DS}$	0	0.0002	0.01	mA	-
Idd Idle[2)]	$PLLIdd_{Idle}$	-	0.0002	-	mA	-
Idd Init0, 1RX + 1TX	$PLLIdd_{Init0}$	-	0.9	-	mA	-
Idd Init1, 1RX + 1TX[3)]	$PLLIdd_{Init1}$	-	7.9	-	mA	-
Idd Active, 1RX + 1TX[4)]	$PLLIdd_{Active}$	5	8	10	mA	-

1) All registers in reset mode, f_{SYS_CLK} clock path disabled.
2) MADC band-gap running.
3) Idd for the rest of interchirp similar to Init1.
4) Device set in radar mode, DAC TX set to 31_D.

Table 10 ***VDD_{LF}* domain current consumption**

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Idd Deep Sleep[1)]	$LFIdd_{DS}$	0	0.0002	0.01	mA	-
Idd Idle[2)]	$LFIdd_{Idle}$	-	0.0002	-	mA	-
Idd Init0, 1RX + 1TX	$LFIdd_{Init0}$	-	0.39	-	mA	-
Idd Init1, 1RX + 1TX[3)]	$LFIdd_{Init1}$	-	0.39	-	mA	-
Idd Active, 1RX + 1TX[4)]	$LFIdd_{Active}$	0.2	0.39	0.53	mA	-

1) All registers in reset mode, f_{SYS_CLK} clock path disabled.
2) MADC band-gap running.
3) Idd for the rest of interchirp similar to Init1.

4) Device set in radar mode, DAC TX set to 31_D.

Table 11 **VDD_{RF} + VDD_{VCO} domain current consumption**

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Idd Deep Sleep[1)]	$RFIdd_{DS}$	0	0.003	0.045	mA	-
Idd Idle[2)]	$RFIdd_{Idle}$	-	0.005	-	mA	-
Idd Init0, 1RX + 1TX	$RFIdd_{Init0}$	-	0.005	-	mA	-
Idd Init1, 1RX + 1TX[3)]	$RFIdd_{Init1}$	-	137	-	mA	-
Idd Active, 1RX + 1TX[4)]	$RFIdd_{Active}$	100	162	220	mA	-

1) All registers in reset mode, f_{SYS_CLK} clock path disabled.
2) MADC band-gap running.
3) Idd for the rest of interchirp similar to Init1.
4) Device set in radar mode, DAC TX set to 31_D.

Table 12 **VDD_{IO} domain current consumption**

VDD_{IO}= 1.71 V to 1.89 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Idd Deep Sleep[1)]	$IOIdd_{DS}$	0	-	0.1[2)]	mA	Standard SPI
Idd Active [3)]	$IOIdd_{Active}$	0	-	0.17	mA	Standard SPI

1) All registers in reset mode, f_{SYS_CLK} clock path disabled.
2) The value at maximum refers to the maximum temperature, +70°C, and the maximum supply, 1.89 V.
3) Activity on SPI MISO and MOSI line.

2.4 ESD integrity

Table 13 **ESD integrity**

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V, VDD_{IO}= 1.08 V to 1.32 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
ESD robustness, *human body model (HBM)*	$V_{ESD\text{-}HBM}$	-2000	-	+2000	V	According to JS-001. All pins.
ESD robustness, *charged device model (CDM)*	$V_{ESD\text{-}CDM}$	-500	-	+500	V	According to JS-002.

charged device model: Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

human body model: Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).

2.5 Thermal resistance

Table 14 Thermal resistance

VDD_X= 1.71 V to 1.89 V, VDD_{LF}= 2.5 V to 3.3 V, VDD_{IO}= 1.08 V to 1.32 V and T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Package thermal resistance	R_{th}	-	35	-	K/W	Chip backside to ambient temperature

3 Shapes, frames and channel set definition

This section is intended to provide the user with an overview on the overall modulation and power modes capabilities of BGT60UTR11AIP. Specifically, the structure of timers, counters, shapes, channel set and frames will be presented. The section also gives a description of how the *FSM* is setting and controlling the *PLL* for the expected modulation shapes and sequences programmed by the host.

3.1 Shapes and frames

The shape is the modulation chirp that should be performed by the PLL. Two basic shapes are allowed (see Shape definition):

- Triangular shape: consisting of a frequency upchirp and a frequency downchirp
- Saw-tooth shape: consisting of a frequency upchirp followed by a fast downchirp

The shapes are set and enabled in the PLLx[0..7] registers (see PLL shape x register 0 and PLL shape x register 7) by the bit PLLx7:SH_EN. Up to four different shapes can be programmed. If more than one shape is used, the lower shapes must be programmed (e.g. if 3 shapes are needed by the application, then x = 1...3).

N_SHAPE_EN is the number of shapes enabled.

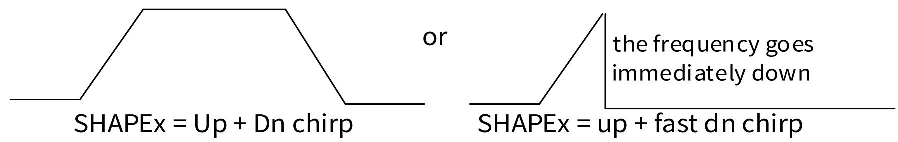

Figure 6 Shape definition

Shape group

Each shape defined above can be repeated several times (see Shape group). The same shape repeated several times represents a shape group (SG). The repetition factor for the shape x is called REPSx and described in PLL shape x register 7. Each shape is repeated $RSx = 2^{REPSx}$ times.

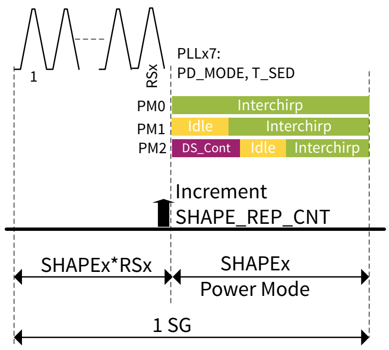

Figure 7 Shape group

After the last repetitions the FSM will enter, for a period PLLx7:T_SED (see PLL shape x register 7), the power mode programmed according to what is specified in PLLx7:PD_MODE (see PLL shape x register 7).

After a shape group, the shape groups counter STAT1: SHAPE_GRP_CNT is incremented (see Status register 1). In Shape set an example of four programmed shape groups is shown. It represents a shape set.

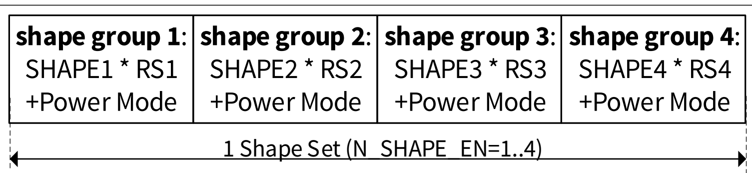

Figure 8 Shape set

Frame

A frame, as shown in Example of one frame, is a sequence of shape sets followed by a specific power mode. Each shape set can be repeated several times. The repetition factor for the shape set x is called REPTx and described in Chirp control register 0. Each shape set is repeated $RTx = 2^{REPTx}$ times.

The length of a frame is defined through CCR2: FRAME_LEN (see Chirp control register 2), which is the number of shape groups to be executed.

At each start of a frame, the first shape SHAPE1 together with the first channel set, CSU1+CSC1, is loaded.

The number of frame groups the FSM will execute will be:

- min(CCR2:FRAME_LEN, N_SHAPE_EN * RT)

With RT ≤ (4096/shape groups) and CCR2:FRAME_LEN < 4096.

After the last shape group in a frame, the power mode from CCR1:PD_MODE is used for the period programmed in CCR1:T_FED instead of PPLx7:MODE for period PLLx7:T_SED.

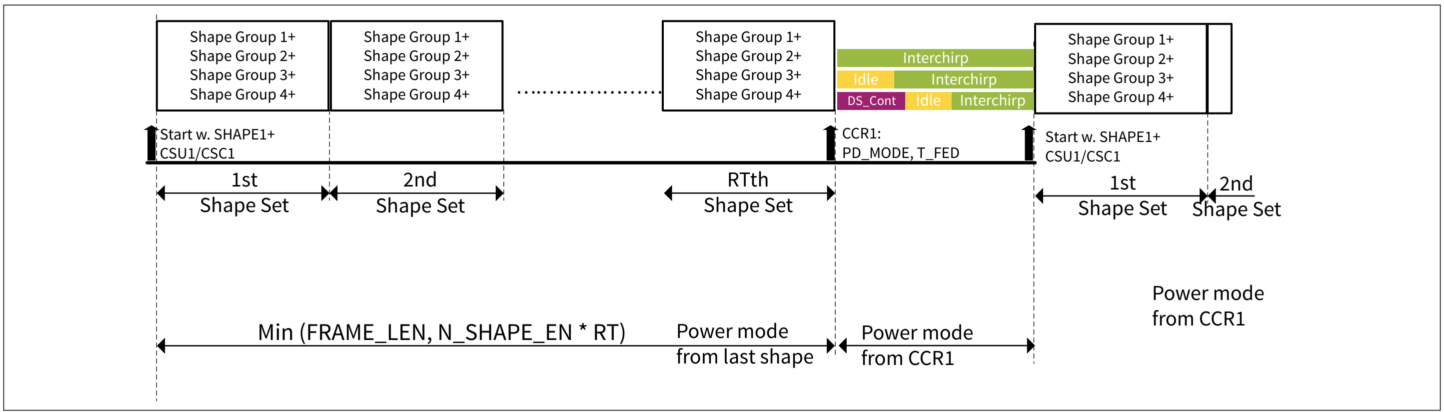

Figure 9 **Example of one frame**

Maximum number of frames

- The overall frame generation starts after the wake-up period with the first frame
- After the last frame CCR2: MAX_FRAME_CNT (see Chirp control register 2) is reached, the FSM will enter the deep sleep mode instead of the power mode defined at the end of the last but one frame
  - In order to trigger the chip again, a FSM reset is required

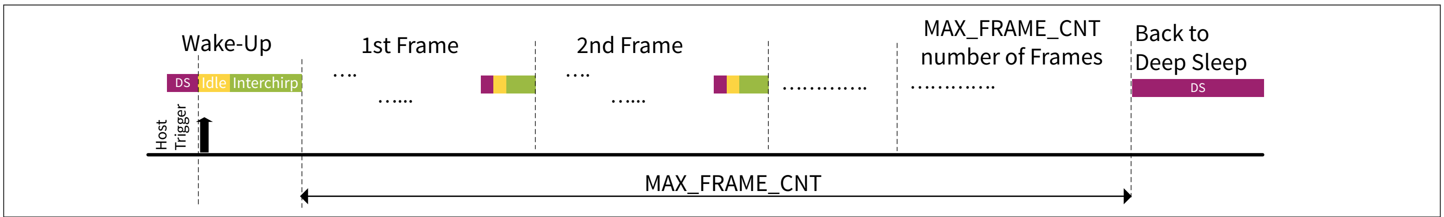

Figure 10 **Maximum number of frames**

3.2 Channel set

A channel set is a set of registers to control the configurations of the available transmit and receive channels. Each channel set can be repeated several times. The repetition factor for the channel set x is called REPCx and described in Channel set control x register. Each channel set is repeated RCx = 2^REPCx times. There are in total 10 channel sets of 3 different types acting in the specific "modes". 8 channel sets relate to the shapes (4 shapes x "up" and "down" segment settings) and two to the power modes, idle and deep sleep, respectively:

- Deep sleep power mode is related to channel set CSDS and CSCDS
- Idle mode is related to channel set CSI and CSCI

- 8 channel sets are defined for the shapes:
  - CSU1 … CSU4 registers for up-chirp
  - CSD1 … CSD4 registers for down-chirp
  - CSC1 … CSC4 channel set configuration registers for up- and down-chirp
- Each shape from above has up to 2 channel sets CSUx and CSDx
  - In case triangular shape is used, CSUx and CSDx are applied
  - In case sawtooth shape is used, CSDx is skipped
- Channel sets are repeated independent of the shapes
- Channel set repetition factor tells how often a single channel set is repeated until the next channel set is loaded
- On the channel set sequence:
  - The lower channel set number is followed by the next higher channel set number
  - In case the highest channel set number is reached, the next channel set loaded is channel set 1
- On the enabling sequence of channel sets:
  - In case not all channel sets are used, the lower number channel sets have to be used
  - In between the enabled channel sets must not be a disabled channel set
  - E.g.: 2 channel sets expected: use only CS1 and CS2. In case 3 channel sets are expected, use only CS1, CS2, and CS3
- Start and end of channel set sequences:
  - After reset, the first channel set loaded is CS1
  - After a frame starts the first channel set loaded will be CS1

***Note**:* *It would be preferable to have REPS = REPC.*

3.3 Power modes

The following figure shows the flow chart on all possible power modes for the FSM.

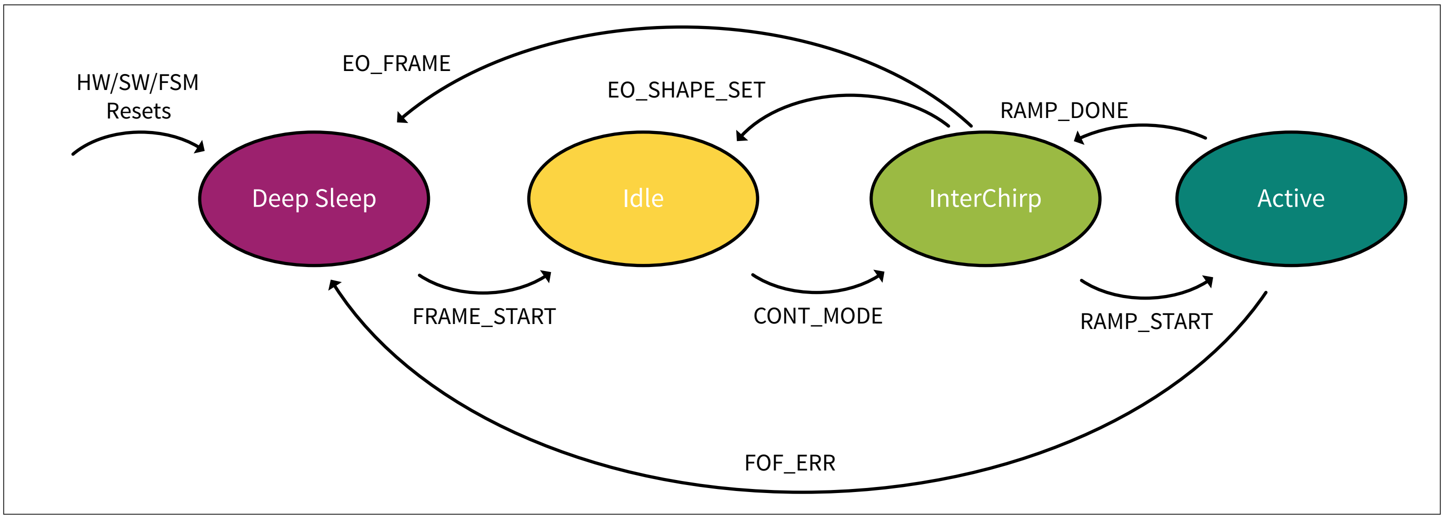

Figure 11 FSM flow chart

Power Management through the power modes

The power modes enable the host to have full flexibility on power consumption during each state of radar frame generation. A set of isolation registers (see Channel set control x register) enables/disables the different blocks of the chip. The power modes are managed by the FSM.

3.3.1 Mode descriptions

In active, idle, and deep sleep mode the power mode can be defined in the CSCx register, Channel set control x register, for all channel sets: CSC1..4, CSI, CSCDS (CSUx = Channel Set Upchirp, CSDx = Channel Set Downchirp, CSI = Channel Set Idle, CSDS = Channel Set Deep Sleep).

Active mode definition:

- During a shape: PLLx7:PD_MODE = 0_D
- Power mode defined through registers CSx (CHS1..CHS4), same mode for up-/downchirp
- Default Setting: all expected settings are enabled by the host

Interchirp mode definition:

- During a shape: PLLx7:PD_MODE = 0_D
- Power mode basically the same as active mode, exception: TX1 off (PAOFF)

Idle mode definition:

- After a shape: PLLx7:PD_MODE = 1_D
- After a frame: CCR1:PD_MODE = 1_D
- Idle mode is defined through CSCI
- Wake-up from deep sleep for TR_WKUP

The idle mode can be used as a low-power mode in between interchirp modes or after deep sleep mode to further reduce the overall power consumption while not entering the deep sleep mode. The wake-up times after Idle mode are faster compared to the ones after deep sleep mode.

Entering deep sleep mode:

- After a frame: CCR1:PD_MODE = 2_D and CCR0:CONT_MODE = 0_B
- Deep sleep mode is defined through CSCDS register (see Channel set control x register)
- All blocks can be turned off
- Internal system clock is also turned off - to achieve extra power saving - when CONT_MODE = 0_B otherwise (CONT_MODE = 1_B) the clock is kept up to count the internal timer T_FED/T_SED during the deep sleep
- In order to wake up the FSM from the deep sleep, the host has to program:
  - PACR1:OSCCLKEN = 1_B to enable the clock gating
  - Then the first trigger can be applied via FRAME_START

  ***Note**: No re-configuration need to be performed as the register content is retained in deep sleep mode.*

Entering deep sleep continuous mode:

- After a shape: PLLx7: PD_MODE = 2_D and PLLx7:CONT_MODE = 1_B
- After a frame: CCR1:PD_MODE = 2_D and CCR0:CONT_MODE = 1_B

In case CCR0:CONT_MODE = 1_B is enabled, the wake-up from deep sleep is done automatically. The internal system clock is kept running.

In case of errors:

If a FIFO overflow condition occurs, the FSM will bring the radar sensor into the deep sleep power mode even if the internal counters are holding the previous value, i.e., the FSM is not reset and a reset is required. In order to reset the FIFO, the host should send at least a MAIN:FIFO_RESET command (see Main register).

If the FIFO overflow occurs, the event is reported in FSTAT:FOF_ERR (see FIFO status register) or in GSR0:FOF_ERR (see Chapter 4.49).

In this case, the data inside a FIFO can be read from the host as long as no reset occurs.

The flags FSTAT:FOF_ERR and GSR0:FOF_ERR are cleared after a reset.

***Note**: Each time the SPI will access the chip, the system clock will be enabled internally for synchronization reasons.*

3.3.2 Wake-up phase from "deep sleep" to "idle"

After VDD_D is powered up, the main LDO will require 20 µs to settle the internal generated core voltage VDD_C. Subsequently, the host has to perform a hardware reset to set the chip to the reset state (deep sleep). The following figure describes the timing for waking up the chip.

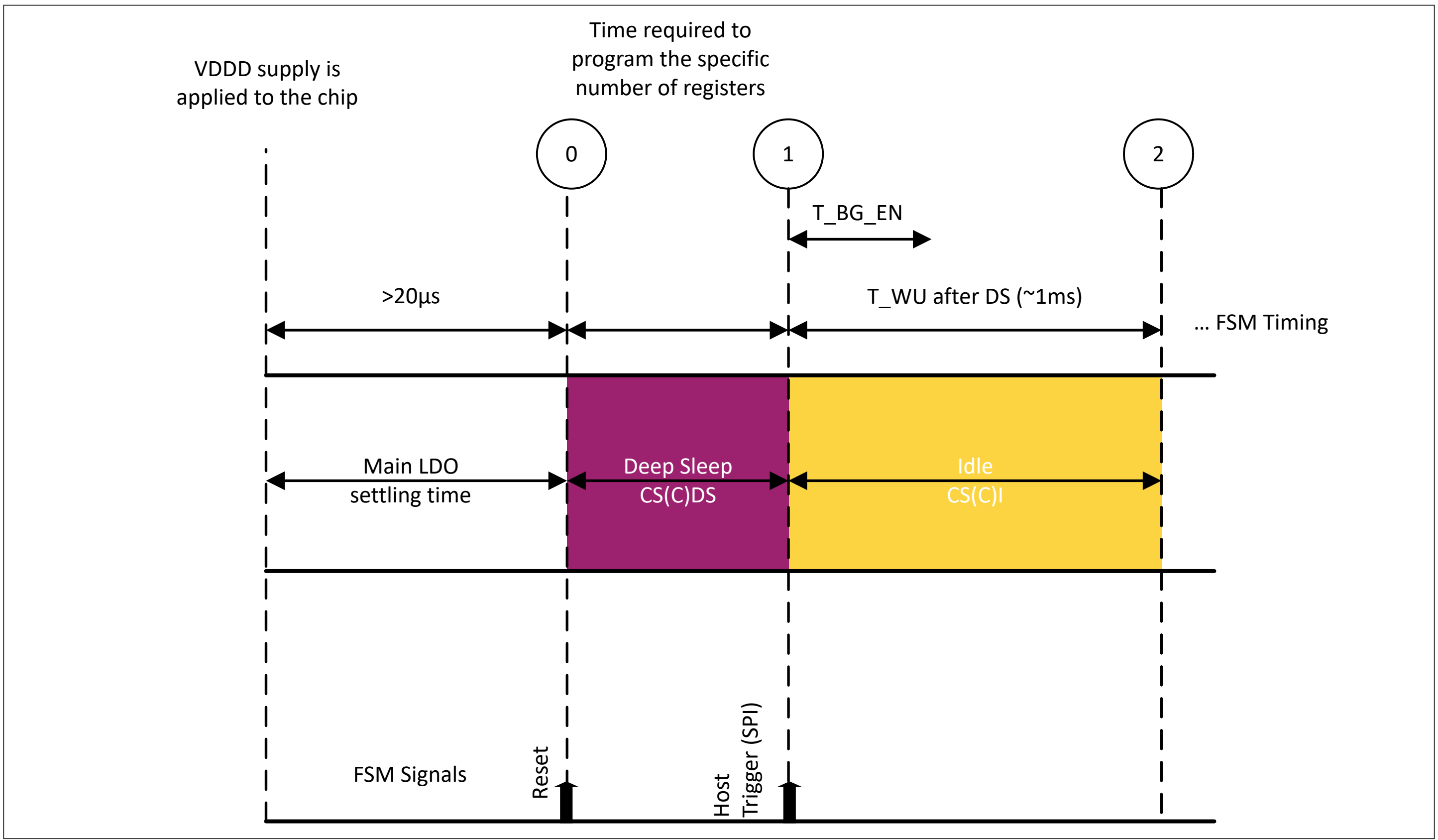

Figure 12 **Deep sleep to idle transition**

Table 15 **Transitions from deep sleep into idle**

From #	To #	Description	Signals	Related time
#0		Chip is reset by host (see Hardware reset sequence)		
#0	#1	Host programs all registers needed for expected functionality		
#1		Host enables the oscillator: PACR1:OSCCLKEN= 1_B to enable the clock gating		
#1		Host starts the first trigger; it can be applied through MAIN:FRAME_START		
#1		Activate bandgap for MADC		
#1	#2	Time required to settle the ADC BG (charge of external cap)		T_WU
#2		Enable PLL, MADC, and SADC		
#2		MADC sends ready signal to FSM	madc_rdy	

3.3.3 Idle to interchirp then active

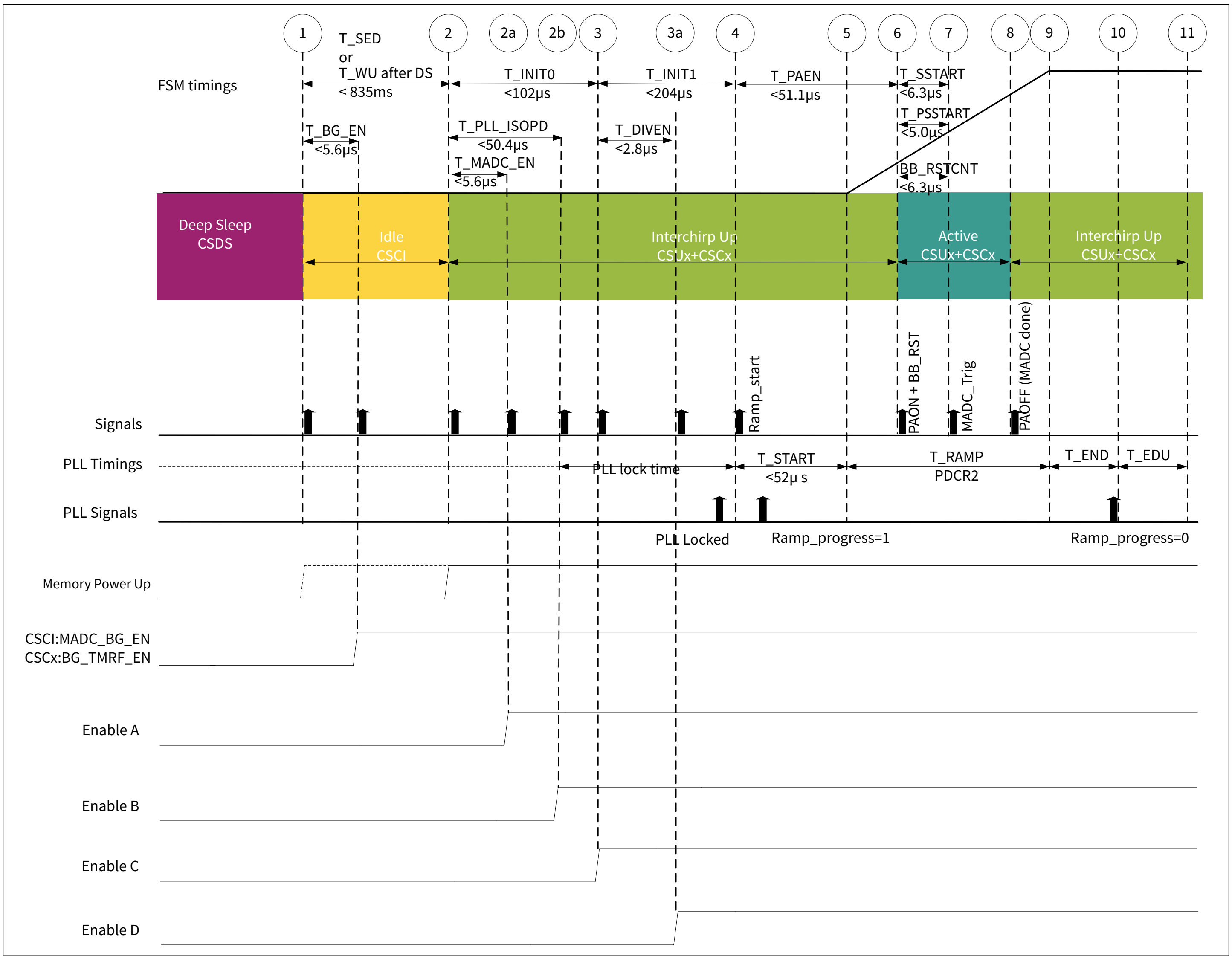

Figure 13 Transition from idle to interchirp to active to interchirp again

Table 16 Transition from idle to interchirp to active to interchirp

From #	To #	Description	Signals	Related time
#1		Idle mode is activated		
#1		The user has to enable the bandgap (CSCI:BG_EN= 1_B in Channel set control x register)		
#1		In the case the memory is powered up after DS (SFCTL:FIFO_PD_MODE = 1_D) the bandgap should be enabled delayed. This can be done by the user by programming CSCI:TR_BGEN		T_BG_EN
#1	#2	If Idle mode comes after a deep sleep (see transition from deep sleep to idle). Wake up time can be used as offset for chirps in case multiple devices are triggered together by *SPI* broadcast for example		T_WU

(table continues...)

Table 16 (continued) Transition from idle to interchirp to active to interchirp

From #	To #	Description	Signals	Related time
#1	#2	If Idle mode comes after an interchirp mode, the bandgap is already running		T_SED
#2		Interchirp Up mode is activated by selecting CSUx + CSCx register depending on the actual channel set (see Channel set up x register 0)		
#2		Host already enabled the blocks required by the PLL: CSx:VCO_EN = 1_B CSx:FDIV_EN = 1_B		
#2		FSM sets power mode from CSUx + CSCx		
#2		FSM sets PACR1.RFILTSEL = 0_B		
#2	#2a	In the case the memory is powered up after Idle (SFCTL:FIFO_PD_MODE = 2_D) the MADC should be enabled delayed. This can be done by the user by programming CSCI:TR_MADCEN		T_MADC_EN
#2a		After T_MADC_EN is over, enable A gets active which gates CSxx_1:MADC_BBCHx_EN		
#2	#2b	To save power there is the option to keep the PLL in reset state and enable the PLL delayed		T_PLL_ISOPD
#2b		After T_PLL_ISOPD is over, enable B gets active which gates CSCx:PLL_ISOPD		
#2	#3	The PLL needs some time to initialize the filter settings (see Chirp control register 3)		T_INIT0
#3		Enable C gets active which gates following signals: PACR1.RFILTSEL, CSxx_0:VCO_EN, CSxx_0:FDIV_EN, CSCx:ABB_ISOPD, CSCx:RF_ISOPD		
#3	#3a	To save power there is the option to close the feedback loop within the PLL delayed		T_DIVEN
#3a		After T_DIVEN is over, enable D gets active which gates PACR2:TR_DIVEN		
#3	#4	The PLL needs again some time to settle the mode (see Chirp control register 0)		T_INIT1
#4		PLL sends lock signal to FSM	PLL_lock	
#4		FSM triggers ramp start of PLL	RAMP_START	
#4	#5	PLL needs some settling time before chirp can start. The PLL timer is running in parallel to the FSM timer. T_START will be evaluated during system testing		T_START (PLL)
#5	#9	PLL will run the frequency chirp		T_RAMP (PLL)
#4	#6	Delay PA enable		T_PAEN
#6		Active mode starts here		

(table continues...)

Table 16 (continued) Transition from idle to interchirp to active to interchirp

From #	To #	Description	Signals	Related time
#6		PA is enabled (PAON). Host makes sure that PA is not ON before the chirp starts (>#5)	PAON	
#6		Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value		
#6	#7	Delay after PA is enabled before the power measurement is started (if activated in CSx)		T_PSSTART
#6	#7	During this phase, the baseband can settle		T_SSTART
#7		MADC is triggered for the active segment (Up)	MADC_TRIG	
#7	#8	MADC starts acquiring the given number of samples (PLLx:APU in PLL shape x register 3).		T_ACQUx
#8		MADC has completed the acquisition of the expected number of samples	MADC_ DONE	
#8		PA is disabled (PAOFF) This condition must be reached before #9 The condition is: T_PAEN + T_SSTART + T_ACQUx > T_START + T_RAMPx	PAOFF	
#8		Interchirp up mode is activated again here (CSUx + CSCx)		
#9		PLL has completed the up-chirp		
#9	#10	Programmable delay time (e.g. 3 µs)		T_END
#10		Ramp completed	RAMP_DONE	
#10	#11	Programmable delay time (e.g. 1 µs)		T_EDU
#11		Interchirp up mode ends here		
#11		Interchirp down mode is programmed here		

3.3.4 Saw-tooth shape timing

In the saw-tooth mode, after a normal upchirp segment there will be a fast ramp down segment. The saw-tooth shape should be enabled in the bitfield PACR2:FSTDNEN (see PLL analog control register 2). For the sawtooth only CSU (Upchirp) is used (see Channel set up x register 0). The time T_EDU (see PLL shape x register 2, PLLx2#) is applied after the segment is completed. See following figure.

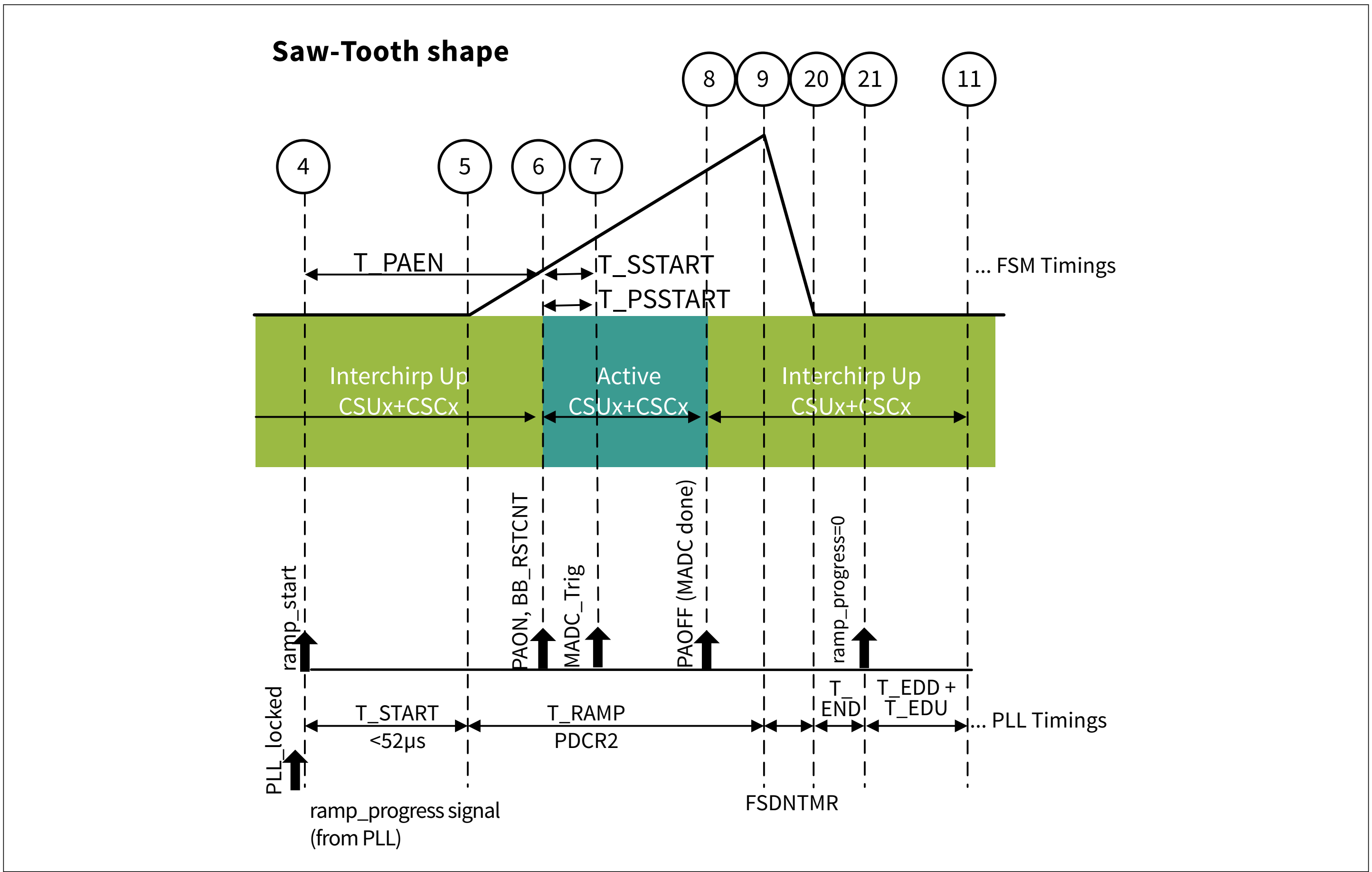

Figure 14 **Saw-tooth shape timing**

3.3.5 Different power modes after shapes and shape groups

After the downchirp shape, the chip can enter different power modes based on the settings (PLLx, CSx, CSCx):

- Interchirp mode in-between shapes – for fast chirp repetitions
- Idle mode after shape groups – in case of longer delay between shape groups and max power saving is required
- Deep sleep + idle mode after shape groups in case if very long delays are expected

3.3.5.1 Idle after shape or shape groups

The idle mode after a shape or shape groups can be set when a long time in low power mode between shapes is required. The following figure represents a time behavior continuation of what is presented in Figure 13.

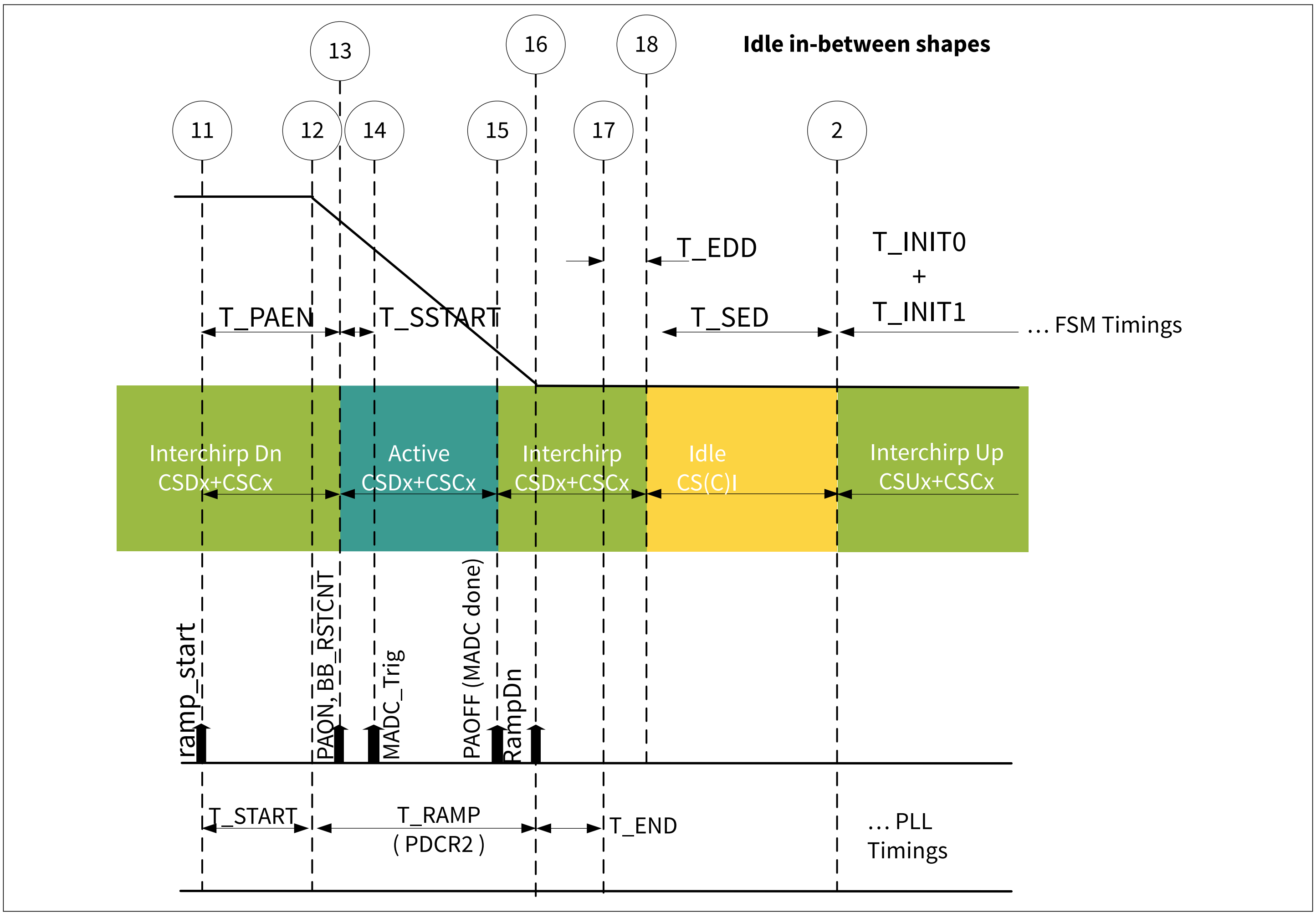

Figure 15 **Idle mode after shape groups**

Table 17 **End of shape and interchirp in-between shapes**

From #	To #	Description	Signals	Related time
#11		Interchirp Dn mode is programmed here (CSDx + CSCx)		
#11		FSM generates ramp_start signal	Ramp_start	
PLL related:				
#11	#12	Preparation for downchirp		T_START
#12	#16	downchirp time		T_RAMP
#16	#17	Some delay after downchirp is completed		T_END
FSM related:				
#11	#13	Some delay (see above T_PAEN)		T_PAEN
#13		Active mode is entered with settings from previous interchirp Dn mode (CSDx+CSCx)		
#13		PA is enabled (PAON) Host makes sure that PA is not on before the chirp starts (>#12)	PAON	

(table continues...)

Table 17 (continued) End of shape and interchirp in-between shapes

From #	To #	Description	Signals	Related time
#13		Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value		
#13	#14	During this phase, the baseband can settle		T_SSTART
#14	#15	MADC starts acquiring the given number of samples (PLLx:APD in PLL shape x register 3).	MADC_TRIG	T_ACQDx
#15		MADC has completed the acquisition of the expected number of samples	MADC_ DONE	
#15		PA is disabled (PAOFF) This condition must be reached before #16 The condition is: T_PAEN + T_SSTART + T_ACQDx > T_START + T_RAMPx.	PAOFF	
#15		Interchirp Dn mode is activated again here (CSDx + CSCx)		
#14	#16	FSM waits for PLL if ramp down to calculate #17 (TMREND)		
#16		PLL signals the end of the downchirp (ramp progress)	RampDN	
#17		Temperature measurement is started (if activated in CSx).		
#17	#18	Time delay programmed by the host		T_EDD
#18	#2	Time programmed by the host to stay in Idle mode		T_SED
#2		Same state #2 as in Figure 13 starts here		

3.3.5.2 Interchirp in-between shapes

Interchirp between shapes can be set when the required gap between two shapes is relatively small (< 25 μs).

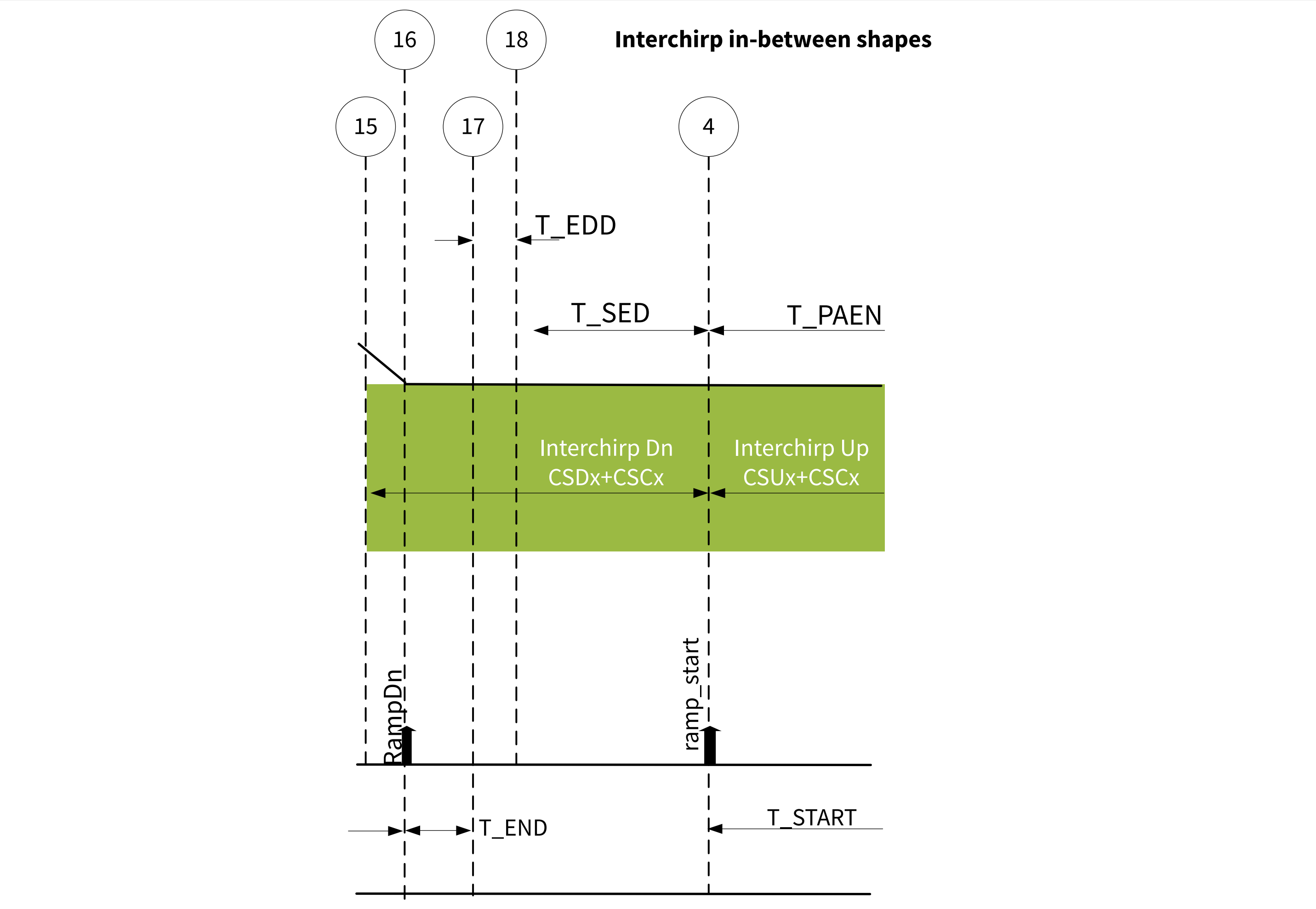

Figure 16 Interchirp in-between shapes

Table 18 Interchirp in-between shapes

From #	To #	Description	Signals	Related time
#15		Interchirp Dn (CSDx + CSCx) is activated after active mode		
#16		PLL signals the end of the downchirp (ramp progress)	RampDN	
#16	#17	Some delay after downchirp is completed		T_END
#17		PLL has completed its action		
#17		Temperature measurement is started (if activated in CSx).		
#17	#18	Time delay programmed by the host		T_EDD
#18	#4	The chip will remain in the same interchirp power state for the provided amount of time (T_EDD)		T_SED
#4		Same state #4 as in Figure 13 starts here		
#4		Interchirp up mode programed by FSM here (CSUx + CSCx)		

3.3.5.3 Deep sleep continuous + idle wake-up after shape groups

In deep sleep cont(inuous) mode after the shape group is completed, the FSM wakes up automatically after the programed time T_SED. The internal clock is kept running during this time. Deep sleep cont is the only deep sleep power mode possible between shape groups.

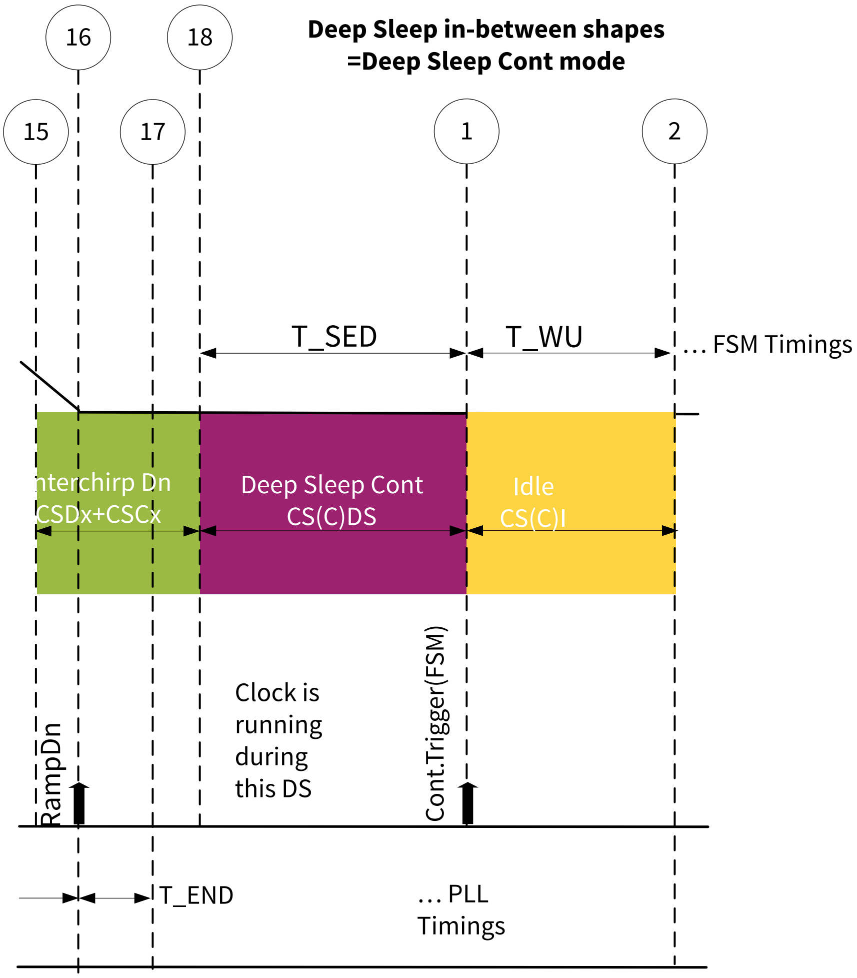

Figure 17 Deep sleep + idle wake-up after shape groups

Table 19 Deep sleep cont + idle wake-up after shape groups

From #	To #	Description	Signals	Related time
#16	#17	Some delay after downchirp is completed		T_END
#17		PLL is completed its action		
#17		Temperature measurement is started (if activated in CSx).		
#17		Deep sleep cont mode is enabled. The difference to the normal deep sleep mode is, the f_{SYS_CLK} is kept running to count the internal timers		
#17		The internal system clock f_{SYS_CLK} is kept running		
#17	#18	Time delay programmed by the host		T_EDD
#18	#1	The chip will be in deep sleep cont mode		T_SED

(table continues...)

Table 19 (continued) Deep sleep cont + idle wake-up after shape groups

From #	To #	Description	Signals	Related time
#1		Continuous trigger coming from the FSM		
#1		Same start-up procedure as Figure 13 starts here		

3.4 System constraints

3.4.1 MADC sampling timing conditions and calculations

The number of MADC samples during a frequency chirp (up or down segment of the shape) should fulfill some specific requirements.

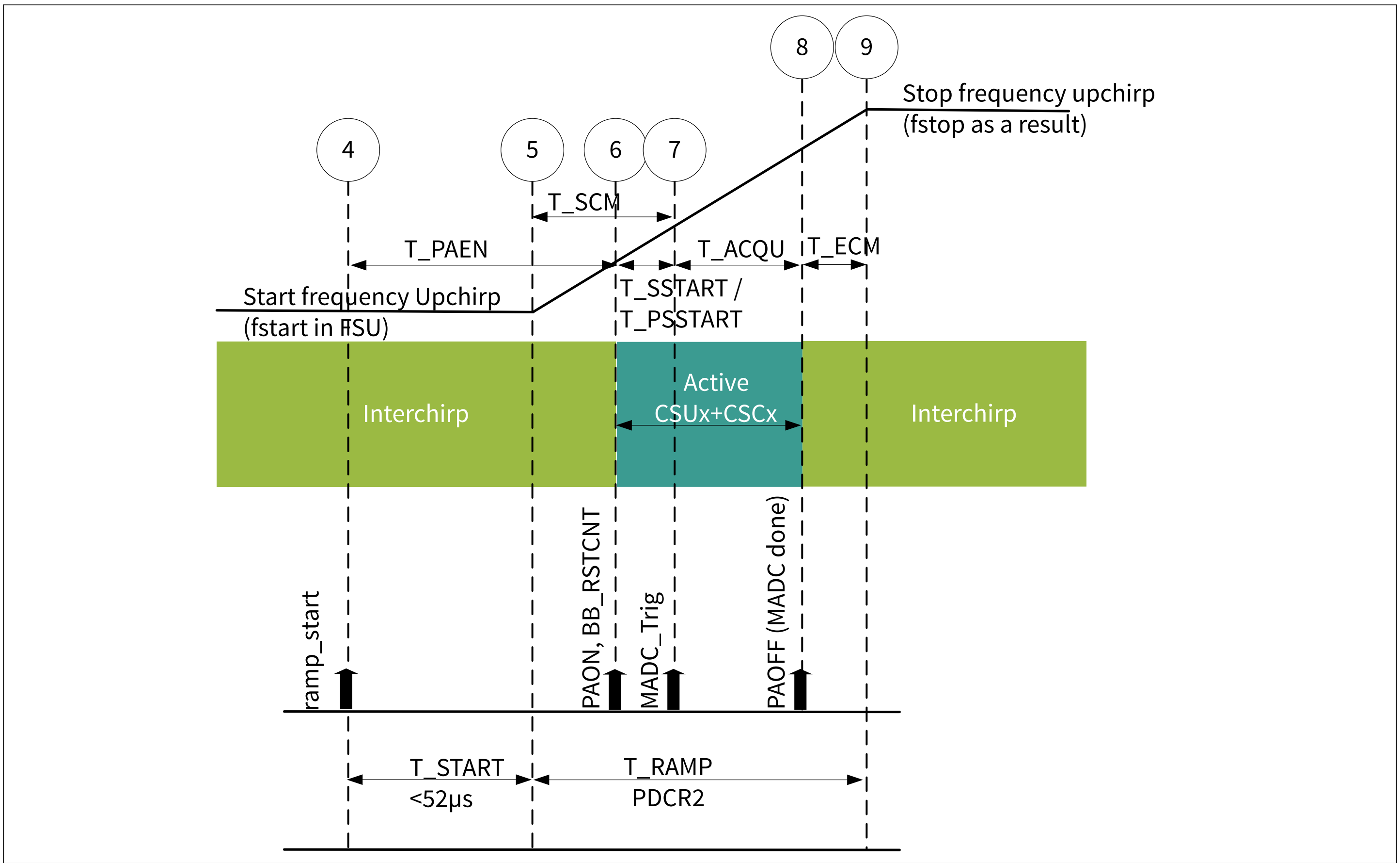

Figure 18 T_RAMP timing conditions

Table 20 T_RAMP timing conditions

From #	To #	Description	Signals	Related time
#4		PLL starts counting		
#4	#5	PLL starts		T_START
#5	#9	PLL performs the frequency upchirp, chirp from fstart (PLLx[1]:FSU) to fstop		T_RAMP
#6	#8	Active phase		
#4	#7	Time to start the MADC		T_PAEN+T_SSTART
#6	#7	Delay after PA is enabled before the power measurement is started (if activated in CSx)		T_PSSTART
#7	#8	MADC sampling time for upchirp raw data		T_ACQUX

(table continues...)

Table 20 (continued) T_RAMP timing conditions

From #	To #	Description	Signals	Related time
#8	#9	End chirp margin T_ECM is needed to avoid transmission out of band. Empirically derived in system		T_ECM
#5	#7	Start chirp margin T_SCM is needed to avoid transmission out of band. Empirically derived in system		T_SCM

Summary:

ADC sampling rate f_{ADC_SAMP} (see Chapter 8.5.5):

- $f_{ADC\_SAMP} = f_{ADC\_CLK}$/ADC_DIV

ADC acquisition time for Upchirp T_ACQUx:

- T_ACQUx = APUx/f_{ADC_SAMP}

Where APU is the number of samples.

End chirp margin T_ECM is tested in system but assumed to be more than 0 µs:

- T_ECM > 0 µs, T_SCM > 0 µs

Condition on the data acquisition start time:

- T_PAEN + T_SSTART > T_START

Considering the start chirp margin TCM at the beginning:

- T_PAEN +T_SSTART – T_SCM = T_START

Overall timing equation:

- T_PAEN + T_SSTART + T_ACQUx + T_ECM = T_START + T_RAMP

Example with fixed number of samples:

In case the user expects a fixed number of samples, the APU is set and T_RAMP is calculated.

The time for a frequency ramp T_RAMP is:

- T_RAMP (PLLx2#:RTU in PLL shape x register 2) = T_PAEN + T_SSTART + T_ACQUx + T_ECM – T_START

Example with fixed chirp-time (T_RAMP):

- T_ACQUx = T_RAMP – (T_SCM + T_ECM)
- APU = (T_ACQUx * f_{ADC_SAMP}),
- APU (PLLx3#:APU in PLL shape x register 3) = (T_RAMP – (T_SCM + T_ECM)) *(f_{SYS_CLK}/ADC_DIV)

3.4.2 PLL frequency ramp setup

The RF frequency ramps generated by the PLL are controlled through the PLLx registers (see PLL shape x register 0), where the bit fields FSU, RSU and RTU control the Upchirp of a shape and the registers FSD, RSD and RTD control the down chirp of a shape. The following description refers only to up chirp ramp setup. The given formulas can be adopted to down chirp ramps by replacing FSU by FSD, RSU by RSD and RTU by RTD.

Each RF frequency ramp is defined by the start frequency programmed to FSU, the ramp slope programmed to RSU and the ramp time programmed to RTU. It must be noted that the slope in RSU is specified as frequency increment per clock cycle while the ramp time in RTU is specified as number of steps where a single step means 8 clock cycles. The relation between RSU and RTU is shown in the following figure.

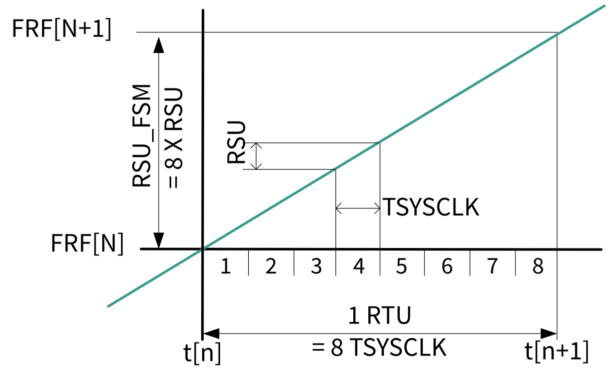

Figure 19 Relationship between RTU and RSU

The value NFSU that is programmed to FSU bit field to control the ramp start frequency is a signed 2's complement number in the range of $-2^{23} \dots (2^{23} - 1)$. The relation between the RF frequency f_{RF} and NFSU is given by:

$$f_{\text{RF}} = 8f_{\text{SYS\_CLK}}\left[4\left(N_{\text{DIVSET}} + 2\right) + 8 + \frac{N_{\text{FSU}}}{2^{20}}\right] \quad (1)$$

where f_{SYS_CLK} is the frequency of the reference clock oscillator and N_{DIVSET} is the value programmed to the bit field DIVSET in register PACR2 (default 20, see PLL analog control register 2). Accordingly the value N_{FSU} can be calculated by this formula:

$$N_{\text{FSU}} = 2^{20}\left[\frac{f_{\text{RF}}}{8f_{\text{SYS\_CLK}}} - 4\left(N_{\text{DIVSET}} + 2\right) - 8\right] \quad (2)$$

The value N_{RSU} that is programmed to RSU bit field to control the frequency increment per clock cycle is also a signed 2's complement number in the range of $-2^{23} \dots (2^{23} - 1)$. The relation between the RF frequency increment Δf_{RF} and N_{RSU} is given by:

$$\Delta f_{\text{RF}} = 8f_{\text{SYS\_CLK}}\frac{N_{\text{RSU}}}{2^{20}} \quad (3)$$

or

$$N_{\text{RSU}} = 2^{20}\frac{\Delta f_{\text{RF}}}{8f_{\text{SYS\_CLK}}} \quad (4)$$

***Note**: Both slope bit fields RSU and RSD can hold positive and negative values, so an up chirp can also be programmed with a falling ramp and a down chirp can be programmed with a rising ramp. The naming convention "up chirp" and "down chirp" are based on the assumption that a triangle shape always starts with the rising ramp. Therefore regardless of the actual ramp slope the up chirp registers always refer to the first chirp of a shape and the down chirp registers always refer to the 2nd chirp of a shape in triangle mode.*

PLL setup example 1 (f_{SYS_CLK} = 80 MHz)

With a reference clock frequency of 40 MHz and activated frequency doubler the recommended value for N_{DIVSET} is 20, the default values. With these parameters the conversion formulas simplify to:

$$N_{\mathrm{FSU}} = 2^{20}\left[\frac{f_{\mathrm{RF}}}{640\ \mathrm{MHz}} - 96\right] \tag{5}$$

and

$$N_{\mathrm{RSU}} = 2^{20}\frac{\Delta f_{\mathrm{RF}}}{640\ \mathrm{MHz}} \tag{6}$$

With the PLL’s 24 bit 2’s complement frequency registers the total programmable RF frequency range is 56.32 GHz ≤ f_{RF} ≤ 66.559 GHz. This may be a wider range than the effectively achievable frequency range.
To achieve a frequency ramp for example from 58 GHz to 62 GHz in 36 µs, the FSU register is programmed to:

$$N_{\mathrm{FSU}} = 2^{20}\left[\frac{58\ \mathrm{GHz}}{640\ \mathrm{MHz}} - 96\right] = -5636096 \mathrel{\widehat{=}} AA0000_{\mathrm{hex}} \tag{7}$$

The ramp time bit field RTU is programmed to:

$$N_{\mathrm{RTU}} = \frac{t_{\mathrm{ramp}}}{8 * T_{\mathrm{SYS\_CLK}}} = 36\ \mu\mathrm{s}\frac{80\ \mathrm{MHz}}{8} = 360 \tag{8}$$

The frequency increment per clock cycle result to:

$$\Delta f_{\mathrm{RF}} = \frac{f_{\mathrm{RF,\,end}} - f_{\mathrm{RF,\,start}}}{8 * N_{\mathrm{RTU}}} = \frac{62\ \mathrm{GHz} - 58\ \mathrm{GHz}}{8 * 360} = \frac{4\ \mathrm{GHz}}{2880} = 1.3\overline{8}\ \mathrm{MHz} \tag{9}$$

Accordingly the bit field RSU is programmed to:

$$N_{\mathrm{RSU}} = 2^{20}\frac{1.3\overline{8}\ \mathrm{MHz}}{640\ \mathrm{MHz}} = 2275.\overline{5} \cong 2276 \mathrel{\widehat{=}} 0008E4_{\mathrm{hex}} \tag{10}$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{\mathrm{RF,\,end}} = f_{\mathrm{RF,\,start}} + 8 * N_{\mathrm{RTU}} * \frac{640\ \mathrm{MHz}}{2^{20}} N_{\mathrm{RSU}} = 62.000781\ GHz \tag{11}$$

PLL setup example 2 (f_{SYS_CLK} = 76.8 MHz)

With a reference clock frequency of 38.4 MHz and activated frequency doubler the recommended value for N_{DIVSET} is 21. With these parameters the conversion formulas simplify to:

$$N_{\mathrm{FSU}} = 2^{20}\left[\frac{f_{\mathrm{RF}}}{614.4\ \mathrm{MHz}} - 100\right] \tag{12}$$

and

$$N_{\mathrm{RSU}} = 2^{20}\frac{\Delta f_{\mathrm{RF}}}{614.4\ \mathrm{MHz}} \tag{13}$$

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is 56.5248 GHz ≤ f_{RF} ≤ 66.3552 GHz. This may be a wider range than the effectively achievable frequency range.
To achieve a frequency ramp from 58 GHz to 62 GHz in 36 µs, the FSU register is programmed to:

$$N_{\mathrm{FSU}} = 2^{20}\left[\frac{58\ \mathrm{GHz}}{614.4\ \mathrm{MHz}} - 100\right] = -5870933.\overline{3} \cong -5870933 \mathrel{\widehat{=}} A66AAB_{\mathrm{hex}} \tag{14}$$

The ramp time bit field RTU is programmed to:

$$N_{\mathrm{RTU}} = \frac{t_{\mathrm{ramp}}}{8 * T_{\mathrm{SYSCLK}}} = 36\ \mu\mathrm{s}\frac{76.8\ \mathrm{MHz}}{8} = 345.6 \cong 346 \tag{15}$$

The frequency increment per clock cycle results to:

$$\Delta f_{\mathrm{RF}} = \frac{f_{\mathrm{RF,\,end}} - f_{\mathrm{RF,\,start}}}{8 * N_{\mathrm{RTU}}} = \frac{62\ \mathrm{GHz} - 58\ \mathrm{GHz}}{8 * 346} = \frac{4\ \mathrm{GHz}}{2768} = 1.44509\ \mathrm{MHz} \tag{16}$$

Accordingly, the bit field RSU is programmed to:

$$N_{\mathrm{RSU}} = 2^{20}\frac{1.44509\ \mathrm{MHz}}{614.4\ \mathrm{MHz}} = 2466.28 \cong 2466 \mathrel{\widehat{=}} 0009A2_{\mathrm{hex}} \tag{17}$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{\mathrm{RF,\,start} = 614.4\ \mathrm{MHz}}\left[100 + \frac{N_{\mathrm{FSU}}}{2^{20}}\right] = 58.0000002\ \mathrm{GHz} \tag{18}$$

$$f_{\mathrm{RF,\,end}} = f_{\mathrm{RF,\,start}} + 8 * N_{\mathrm{RTU}} * \frac{614.4\ \mathrm{MHz}}{2^{20}} N_{\mathrm{RSU}} = 61.99954\ \mathrm{GHz} \tag{19}$$

4 BGT60UTR11AIP registers

An array of registers accessible via the SPI is used to control and program the states of the different blocks inside the chip.

The registers are arranged in blocks of 24 bits each. Each block is identified by its unique address. The registers are accessed from the SPI module. The bit fields from each register are arranged in MSB first order.

The following table gives an overview on the BGT60UTR11AIP registers.

4.1 Abbreviations

Access modes on the registers:

- r: readable register or bit field
- w: writeable register or bit field
- h: hardware writeable register or bit field

***Note**: The reserved (RSVD) bits in the registers should not be modified. They should be kept in the reset state unless otherwise specified. This is also valid for the* RSVD *states of multi bit fields.*

4.2 Register overview - BGT60UTR11AIP (ascending offset address)

Table 21 Register overview - BGT60UTR11AIP (ascending offset address)

Short name	Long name	Offset address	Page number
MAIN	Main register	000_H	38
ADC0	ADC control register	001_H	40
CHIP_Version	Digital and RF version register	002_H	42
STAT1	Status register 1	003_H	43
PACR1	PLL analog control register 1	004_H	43
PACR2	PLL analog control register 2	005_H	45
SFCTL	SPI and FIFO control register	006_H	47
CSI_0	Channel set idle register 0	008_H	48
CSI_1	Channel set idle register 1	009_H	49
CSI_2	Channel set idle register 2	$00A_H$	50
CSCI	Channel set control idle register	$00B_H$	51
CSDS_0	Channel set deep sleep register 0	$00C_H$	52
CSDS_1	Channel set deep sleep register 1	$00D_H$	54
CSDS_2	Channel set deep sleep register 2	$00E_H$	55
CSCDS	Channel set control deep sleep register	$00F_H$	56
CSUx_0	Channel set up x register 0	010_H+(x-1)*7	57
CSUx_1	Channel set up x register 1	011_H+(x-1)*7	58
CSUx_2	Channel set up x register 2	012_H+(x-1)*7	59
CSDx_0	Channel set down x register 0	013_H+(x-1)*7	60
CSDx_1	Channel set down x register 1	014_H+(x-1)*7	61

(table continues...)

Table 21 (continued) Register overview - BGT60UTR11AIP (ascending offset address)

Short name	Long name	Offset address	Page number
CSDx_2	Channel set down x register 2	015_H+(x-1)*7	62
CSCx	Channel set control x register	016_H+(x-1)*7	63
CCR0	Chirp control register 0	$02C_H$	64
CCR1	Chirp control register 1	$02D_H$	65
CCR2	Chirp control register 2	$02E_H$	66
CCR3	Chirp control register 3	$02F_H$	67
PLLx_0	PLL shape x register 0	030_H+(x-1)*8	68
PLLx_1	PLL shape x register 1	031_H+(x-1)*8	68
PLLx_2	PLL shape x register 2	032_H+(x-1)*8	69
PLLx_3	PLL shape x register 3	033_H+(x-1)*8	70
PLLx_4	PLL shape x register 4	034_H+(x-1)*8	70
PLLx_5	PLL shape x register 5	035_H+(x-1)*8	71
PLLx_6	PLL shape x register 6	036_H+(x-1)*8	71
PLLx_7	PLL shape x register 7	037_H+(x-1)*8	72
ADC1	Sensor ADC register	050_H	73
RFT0	RF test register 0	055_H	73
EFUSE0	EFUSE register 0	057_H	75
EFUSE1	EFUSE register 1	058_H	75
PDFT0	PLL test register 0	059_H	76
CHIP_ID0	Chip ID register 0	$05D_H$	76
CHIP_ID1	Chip ID register 1	$05E_H$	77
CLK_IN	Clock input register	$05F_H$	77
WU	Wake up register	060_H	78
STAT0	Status register 0	061_H	79
SENSOR_RESULT	Sensor ADC result register	062_H	80
FSTAT	FIFO status register	063_H	81

4.3 Main register

This register controls the top level behavior of the chip.

MAIN Offset address: 000_H

Main register Reset value: $1C\ 0B00_H$

23	22	21	20	19	18	17	16
LDO_MODE	**LOAD_STRENGTH**		**MADC_BG_CLK_DIV**		**RSVD**		**CW_MODE**
rw	rw		rw		r		rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				**PU_RST_EN**	**RSVD**	**PU_DO_EN**	**PU_DI_EN**	**PU_CLK_EN**	**PU_CSN_EN**	**PU_IRQ_EN**	**SPI_BC_MODE**	**FIFO_RESET**	**FSM_RESET**	**SW_RESET**	**FRAME_START**
r				rw	r	rw	rw	rw	rw	rw	rw	w	w	w	w

Field	Bits	Type	Description
FRAME_START	0	w	**Start a frame generation:** 0_B ... No effect 1_B ... Executes a frame start and clears this bit Note: Can be stopped by executing a HW_RESET, SW_RESET or FSM_RESET.
SW_RESET	1	w	**Reset the complete chip:** 0_B ... No effect 1_B ... Executes a software reset and clears this bit
FSM_RESET	2	w	**Reset the Finite State Machine:** 0_B ... No effect 1_B ... Executes a FSM reset and clears this bit
FIFO_RESET	3	w	**Reset the FIFO:** 0_B ... No effect 1_B ... Executes a FIFO reset and clears this bit
SPI_BC_MODE	4	rw	**Enables SPI broadcast mode:** 0_B ... Disabled 1_B ... Enabled Note: When enabled the output drivers of SPI pins are disabled to avoid conflicts on shared MISO line. Can be used to program/trigger multiple devices at the same time.
PU_IRQ_EN	5	rw	**Enables pull-up of IRQ pin:** 0_B ... Disabled 1_B ... Enabled
PU_CSN_EN	6	rw	**Enables pull-up of CSN pin:** 0_B ... Disabled 1_B ... Enabled
PU_CLK_EN	7	rw	**Enables pull-up of CLK pin:** 0_B ... Disabled 1_B ... Enabled
PU_DI_EN	8	rw	**Enables pull-up of DI pin:** 0_B ... Disabled 1_B ... Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
PU_DO_EN	9	rw	**Enables pull-up of DO pin:** 0_B ... Disabled 1_B ... Enabled
RSVD	10, 15:12, 18:17	r	**Reserved**
PU_RST_EN	11	rw	**Enables pull-up of RST pin:** 0_B ... Disabled 1_B ... Enabled
CW_MODE	16	rw	**Continuous wave mode:** 0_B ... Normal mode 1_B ... Continuous wave mode Note: When active no shapes are executed but PLL, RF, ADC run with values programmed in PDFT0, PDFT1 and channel set 1 registers.
MADC_BG_CLK_DIV	20:19	rw	**MADC bandgap clock frequency divider value:** 0_D ... Bandgap clock off 1_D ... Divider value is 1 2_D ... Divider value is 2 3_D ... Divider value is 4 Note: not clock tree balanced
LOAD_STRENGTH	22:21	rw	**LDO dummy load to smooth current peaks (over and under shoots of VDD_C caused by toggling of digital logic):** 0_D ... Disabled 1_D ... 100 µA (current in the dummy load) 2_D ... 200 µA (current in the dummy load) 3_D ... 400 µA (current in the dummy load)
LDO_MODE	23	rw	**The LDO settling time is defined by:** 0_B ... Low power (50 µA), slow settling time 1_B ... High power (100 µA), fast settling time

4.4 ADC control register

The bits in this register are used to set properly the ADC in the RX chain.

ADC0 Offset address: 001_H

ADC control register Reset value: $0A\ 0240_H$

23	22	21	20	19	18	17	16
ADC_DIV							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_DIV		**RSVD**	**TRIG_MADC**	**MSB_CTRL**	**TRACK_CFG**		**DSCAL**	**STC**		**BG_CHOP_EN**	**BG_TC_TRIM**			**ADC_OVERS_CFG**	
rw		r	w	rw	rw		rw	rw		rw	rw			rw	

Field	Bits	Type	Description
ADC_OVERS_CFG	1:0	rw	**ADC oversampling configuration:** 0_D ... No oversampling (standard 11 bits conversion) 1_D ... Reserved 2_D ... Reserved 3_D ... Reserved
BG_TC_TRIM	4:2	rw	**Temperature coefficient trimming (static):** 0_D ... Minimum value 7_D ... Maximum value
BG_CHOP_EN	5	rw	**Enables chopping within the bandgap:** 0_B ... Disabled 1_B ... Enabled
STC	7:6	rw	**Sample time control:** 0_D ... 50 ns 1_D ... 100 ns 2_D ... 200 ns 3_D ... 400 ns
DSCAL	8	rw	**Disables startup calibration:** 0_B ... Enabled 1_B ... Disabled
TRACK_CFG	10:9	rw	**Tracking conversion configuration bits:** 0_D ... No sub conversion 1_D ... 1 sub conversion 2_D ... 3 sub conversions 3_D ... 7 sub conversions Note: Sub conversions are executed and averaged.
MSB_CTRL	11	rw	**MSB decision time selection during calibration and conversion:** 0_B ... Single MSB decision time 1_B ... Double MSB decision time
TRIG_MADC	12	w	**Trigger for manual ADC conversion:** 0_B ... No effect 1_B ... Executes a single ADC conversion and clears this bit
RSVD	13	r	**Reserved**

(table continues...)

(continued)

Field	Bits	Type	Description
ADC_DIV	23:14	rw	**ADC sampling frequency divider value. The actual sampling frequency will be $f_{ADC\_SAMP} = f_{ADC\_CLK}$ / ADC_DIV:** $0_D..19_D$ ... Reserved 20_D ... Minimum divider value 1023_D ... Maximum divider value Note: A typical value is 33_D resulting in f_{ADC_SAMP} = 2.42 MS/s (@f_{SYS_CLK} = 80 MHz)

4.5 Digital and RF version register

The register CHIP_Version provides information regarding the digital code version, the RF block version, and the antenna configuration (number of channels, position of the antennas e.g.). It is used by the driver to configure the device properly according to the information below.

CHIP_Version | Offset address: 002_H

Digital and RF version register | Reset values see: Table 22

23	22	21	20	19	18	17	16
RSVD				**RSVD**		**RSVD**	
r				r		r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIGITAL_ID								**RF_ID**							
r								r							

Field	Bits	Type	Description
RF_ID	7:0	r	**Revision of analog logic:** 12_D ... BGT60UTR11AIP Note: EES sample: 7_D
DIGITAL_ID	15:8	r	**Revision of digital control logic:** 7_D ... BGT60UTR11AIP
RSVD	23:16,	r	**Reserved**

Table 22 **Reset values of CHIP_Version**

Reset type	Reset value	Note
Reset	X000 0000 0000 0111 0000 1100_B	

4.6 Status register 1

The status register provides internal counter values for the actual number of frames and shapes. They are also provided to the data header. However, it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after e.g. 100 µs.

STAT1 Offset address: 003_H

Status register 1 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
FRAME_CNT							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_CNT				SHAPE_GRP_CNT											
rh				rh											

Field	Bits	Type	Description
SHAPE_GRP_CNT	11:0	rh	**Shape group counter:** 0_D ... Reset value / rollover value after maximum value reached 4095_D ... Maximum value
FRAME_CNT	23:12	rh	**Frame counter:** 0_D ... Reset value / rollover value after maximum value reached 4095_D ... Maximum value Note: This field is for debug only. FRAME_CNT info should not be used when endless mode enabled (please check CCR2:MAX_FRAME_CNT).

4.7 PLL analog control register 1

The bits in this register are used to properly set the PLL.

PACR1 Offset address: 004_H

PLL analog control register 1 Reset value: $19\ 6524_H$

23	22	21	20	19	18	17	16
OSCCLKEN	LFEN	CPEN	BIASFORC	ICPSEL			LOCKFORC
rw	rw	rw	rw	rw			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKSEL			RSVD	RLFSEL	RFILTSEL	VREFSEL		U2IEN	BGAPEN	VDIGREG		DIGPON	VANAREG		ANAPON
rw			r	rw	rw	rw		rw	rw	rw		rw	rw		rw

Field	Bits	Type	Description
ANAPON	0	rw	**Enables the power of the analog regulator:** 0_B ... Disabled 1_B ... Enabled
VANAREG	2:1	rw	**Selects the output voltage of analog regulator:** 0_D ... 1.44 V 1_D ... 1.50 V 2_D ... 1.55 V 3_D ... 1.60 V (@V_{bg} = 1.2 V)
DIGPON	3	rw	**Enables the power of the digital regulator:** 0_B ... Disabled 1_B ... Enabled
VDIGREG	5:4	rw	**Selects the output voltage of digital regulator:** 0_D ... 1.44 V 1_D ... 1.50 V 2_D ... 1.55 V 3_D ... 1.60 V (@V_{bg} = 1.2 V)
BGAPEN	6	rw	**Enables bandgap reference:** 0_B ... Disabled 1_B ... Enabled
U2IEN	7	rw	**Enables voltage-to-current converter:** 0_B ... Disabled 1_B ... Enabled
VREFSEL	9:8	rw	**Selects the reference voltage/common mode level of loop filter:** 0_D ... 433 mV 1_D ... 506 mV 2_D ... 578 mV 3_D ... 650 mV
RFILTSEL	10	rw	**Selects the resistance R_{filt} of the reference filter:** 0_B ... R_{filt} = 100 kΩ 1_B ... R_{filt} = 1 MΩ Note: Switch together with CPEN from 0_B to 1_B to improve start-up time!
RLFSEL	11	rw	**Selects the resistance R_{lf} inside the loop filter:** 0_B ... R_{lf} = 5 kΩ 1_B ... R_{lf} = 7 kΩ
RSVD	12	r	**Reserved**

(table continues...)

(continued)

Field	Bits	Type	Description
LOCKSEL	15:13	rw	**Selects the lock detection window:** 0_D ... 0.265 ns 1_D ... 0.5 ns 2_D ... 1.0 ns 3_D ... 1.5 ns 4_D ... 2.0 ns 5_D ... 2.8 ns 6_D ... 3.8 ns 7_D ... 4.6 ns
LOCKFORC	16	rw	**Forces the lock signal:** 0_B ... Lock not forced 1_B ... Lock forced (to high)
ICPSEL	19:17	rw	**Selects the charge pump current:** 0_B ... 40 µA 1_B ... 80 µA 2_B ... 120 µA 3_B ... 160 µA 4_B ... 200 µA 5_B ... 240 µA 6_B ... 280 µA 7_B ... 280 µA
BIASFORC	20	rw	**Enables fixed biasing inside charge pump:** 0_B ... Disabled (Bias regulation loop active) 1_B ... Enabled (Bias regulation loop deactivated)
CPEN	21	rw	**Enables charge pump:** 0_B ... Disabled 1_B ... Enabled
LFEN	22	rw	**Enables loop filter:** 0_B ... Disabled 1_B ... Enabled
OSCCLKEN	23	rw	**Enables system clock (SYS_CLK):** 0_B ... Disabled 1_B ... Enabled Note: This bit is controlled by FSM during operation. After deep sleep this bit should be enabled by the host. Before the MAIN:FRAME_START is raised the OSCCLKEN must be enabled!

4.8 PLL analog control register 2

The bits in this register are used to properly set the PLL.

PACR2 Offset address: 005_H

PLL analog control register 2 Reset value: $04\ 0014_H$

23	22	21	20	19	18	17	16
TR_DIVEN			**RSVD**	**DTSEL**		**TRIV REG**	**FSDN TMR**
rw			r	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSDNTMR								**FSTDNEN**		**DIVE N**	**DIVSET**				
rw								rw		rw	rw				

Field	Bits	Type	Description
DIVSET	4:0	rw	**Set fixed part of integer division factor:** $0_D..19_D$ ... Reserved 20_D ... valid for 80 MHz system clock 21_D ... valid for 76.8 MHz or 38.4 MHz system clock $22_D..31_D$ ... Reserved Note: Consider offset of |2|
DIVEN	5	rw	**Enables divider:** 0_B ... Disabled (input clock of divider gated) 1_B ... Enabled
FSTDNEN	7:6	rw	**Enables fast down chirp** 0_D ... Disabled 1_D ... Reserved 2_D ... Enabled fast down chirp 3_D ... Reserved
FSDNTMR	16:8	rw	**Defines the time for the PLL loop filter discharge during fast down chirp operation. When FSTDNTMR = 0_D and FSTDNEN ≠ 0_D, the fast down chirp length is internally assigned to a default value (@typ f_{SYS_CLK}):** T_FSTDN = (FSTDNTMR + 1) * T_{SYS_CLK} $0_D..4_D$ ... Reserved 5_D ... 75 ns $6_D..511_D$ ... Reserved
TRIVREG	17	rw	**Set regulator off state to tristate (for both analog and digital regulator):** 0_B ... Off state is 0.0 V 1_B ... Off state is tristate Note: Setting active for digital regulator if DIGPON = 0_B or ANAPON = 0_B.
DTSEL	19:18	rw	**Select PFD dead time / dead zone:** 0_D ... 180 ps to 350 ps 1_D ... 270 ps to 510 ps 2_D ... 360 ps to 680 ps 3_D ... 450 ps to 840 ps
RSVD	20	r	**Reserved**

(table continues...)

(continued)

Field	Bits	Type	Description
TR_DIVEN	23:21	rw	**Time for T_DIVEN. Defines the delay after PACR2:DIVEN is handed over to PLL and pll_rst_n is released. Running in parallel to T_INIT1.** T_DIVEN = (TR_DIVEN * 32 + 1) * T_{SYS_CLK}: 0_D ... Minimum value 7_D ... Maximum value

4.9 SPI and FIFO control register

This register is used to configure the SPI and FIFO.

SFCTL — Offset address: 006_H

SPI and FIFO control register — Reset value: $79\ 6000_H$

23	22	21	20	19	18	17	16
RSVD				**PAD_MODE**	**PREFIX_EN**	**LFSR_EN**	**MISO_HS_READ**
r				rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_PD_MODE		**RSVD**	**FIFO_CREF**												
rw		r	rw												

Field	Bits	Type	Description
FIFO_CREF	12:0	rw	**FIFO compare reference defines the compare filling status for interrupt and CREF reporting. When filling status is > FIFO_CREF an interrupt is issued:** 0_D ... Minimum value is 0, interrupt generated in case first sample is written into FIFO 2047_D ... Maximum value in case FIFO is full with 2048 memory locations
RSVD	13, 23:20	r	**Reserved**
FIFO_PD_MODE	15:14	rw	**RAM power mode for power saving (power switch):** 0_D ... FIFO RAM always powered up 1_D ... FIFO RAM powered down during Deepsleep and powered up after Deepsleep 2_D ... FIFO RAM powered down during Deepsleep + Idle and powered up after Idle 3_D ... Reserved Note: RAM is only powered down when FIFO is empty.

(table continues...)

(continued)

Field	Bits	Type	Description
MISO_HS_READ	16	rw	**Change working edge of SPI DO (MISO) to enable higher SPI frequencies (>= 25 MHz):** 0_B ... MISO data is sent with falling edge of SPI_CLK 1_B ... MISO data is sent with rising edge of SPI_CLK Note: HS_RD = 0_B can only be used for a f_{SPI_CLK} less than 25 MHz. For high speed transfer please check the timing of the SPI master and adjust settings accordingly. The setting becomes active when the last bit of FSCTL is clocked out and it affects MISO immediately.
LFSR_EN	17	rw	**Enable LFSR data generation:** 0_B ... Disabled 1_B ... Enabled Note: LFSR should be enabled after a FIFO reset to ensure an empty FIFO.
PREFIX_EN	18	rw	**Enables the prefix data header written into the FIFO prior to the sampling data of each chirp:** 0_B ... Disabled 1_B ... Enabled
PAD_MODE	19	rw	**SPI pad driver mode to control the slew rate:** 0_B ... Normal mode 1_B ... Strong mode (enables up to 15% shorter fall times)

4.10 Channel set idle register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSI_0 Offset address: 008_H

Channel set idle register 0 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD			**ABB1_AAF_CTRL**	**RSVD**			
r			rw	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		**RX1MIX_EN**	**RX1LOBUF_EN**	**LO_DIST1_EN**	**LO_DIST2_EN**	**RSVD**			**FDIV_EN**	**TEMP_MEAS_EN**	**VCO_EN**	**RSVD**		**PD1_EN**	**TX1_EN**
r		rw	rw	rw	rw	r			rw	rw	rw	r		rw	rw

Field	Bits	Type	Description
TX1_EN	0	rw	**Enables the DAC and power amplifier of TX1:** 0_B ... Disabled 1_B ... Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
PD1_EN	1	rw	**Enables the power detector of TX1:** 0_B ... Disabled 1_B ... Enabled
RSVD	3:2, 9:7, 19:14, 23:21	r	**Reserved**
VCO_EN	4	rw	**Enables the VCO:** 0_B ... Disabled 1_B ... Enabled
TEMP_MEAS_EN	5	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
FDIV_EN	6	rw	**Enables the VCO frequency divider:** 0_B ... Disabled 1_B ... Enabled Note: DIV output
LO_DIST2_EN	10	rw	**Enables the local oscillator distribution buffer to RX1 channel:** 0_B ... Disabled 1_B ... Enabled
LO_DIST1_EN	11	rw	**Enables the local oscillator distribution buffer to TX1 channel:** 0_B ... Disabled 1_B ... Enabled
RX1LOBUF_EN	12	rw	**Enables the local oscillator buffer to the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
RX1MIX_EN	13	rw	**Enables the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
ABB1_AAF_CTRL	20	rw	**Selection of analog base band anti-aliasing filter frequency on channel 1:** 0_B ... 600 kHz 1_B ... 1 MHz

4.11 Channel set idle register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSI_1 Offset address: 009_H

Channel set idle register 1 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD			**MADC_BBCH1_EN**	**BB_RSTCNT**			
r			rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BB_RSTCNT		**RSVD**			**HP1_GAIN**	**RSVD**					**TX1_DAC**				
rw		r			rw	r					rw				

Field	Bits	Type	Description
TX1_DAC	4:0	rw	**TX1 output power setting:** 0_D ... Minimum output power 31_D ... Maximum output power
RSVD	9:5, 13:11, 23:21	r	**Reserved**
HP1_GAIN	10	rw	**Gain setting of the first stage of the high pass filter of channel 1:** 0_B ... 30 dB 1_B ... 18 dB
BB_RSTCNT	19:14	rw	**Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. T_{BBRST} = BB_RSTCNT * 8 * T_{SYS_CLK}:** 0_D ... No analog baseband reset 1_D ... Minimum value 127_D ... Maximum value
MADC_BBCH1_EN	20	rw	**Enables the baseband filters, baseband amplifiers and ADC on channel 1:** 0_B ... Disabled 1_B ... Enabled

4.12 Channel set idle register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSI_2 Offset address: $00A_H$

Channel set idle register 2 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										**VGA_GAIN1**			**HPF_SEL1**		
r										rw			rw		

Field	Bits	Type	Description
HPF_SEL1	2:0	rw	**High pass filter cutoff frequency setting of channel 1:** 0_D ... 20 kHz 1_D ... 40 kHz 2_D ... 80 kHz 3_D ... 140 kHz 4_D ... 160 kHz 5_D ... Reserved 6_D ... Reserved 7_D ... Reserved
VGA_GAIN1	5:3	rw	**VGA gain setting of channel 1:** 0_D ... 0 dB 1_D ... 5 dB 2_D ... 10 dB 3_D ... 15 dB 4_D ... 20 dB 5_D ... 25 dB 6_D ... 30 dB 7_D ... Reserved
RSVD	23:6	r	**Reserved**

4.13 Channel set control idle register

The channel set control register CSCI is related to the channel set register CSI.

All bits are used to define a specific power mode.

ISOPD represent a logical isolation layer and is used to disable complete modules (e.g. MADC) while preserving its configuration (no change in the ADC0 register configuration).

CSCI Offset address: $00B_H$

Channel set control idle register Reset value: $24\ 0960_H$

23	22	21	20	19	18	17	16
	TR_BGEN			**TR_MADCEN**		**TR_PLL_ISOPD**	
	rw			rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TR_PLL_ISOPD			**PLL_ISOPD**	**BG_TMRF_EN**	**RSVD**	**MADC_ISOPD**	**MADC_BG_EN**	**RF_ISOPD**	**ABB_ISOPD**			**RSVD**		
	rw			rw	rw	r	rw	rw	rw	rw			r		

Field	Bits	Type	Description
RSVD	4:0, 9	r	**Reserved**

(table continues...)

(continued)

Field	Bits	Type	Description
ABB_ISOPD	5	rw	**Enables the isolation of all control signals to the ABB:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
RF_ISOPD	6	rw	**Enables the isolation of all control signals to the RF:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
MADC_BG_EN	7	rw	**Enables the bandgap of the MADC:** 0_B ... Disabled 1_B ... Enabled
MADC_ISOPD	8	rw	**Enables the isolation of all control signals to the MADC:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
BG_TMRF_EN	10	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
PLL_ISOPD	11	rw	**Enables the isolation of all control signals to the PLL:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
TR_PLL_ISOPD	17:12	rw	**Timer for T_PLL_ISOPD. Delay PLL isolation after IDLE state:** 0_D ... T_PLL_ISOPD = T_{SYS_CLK} 1_D..63_D ... T_PLL_ISOPD = (TR_PLL_ISOPD * 64 + 2) * T_{SYS_CLK} Note: if TR_PLL_ISOPD > 0_D then CSCI:PLL_ISOPD should be 1_B and T_INIT0 must be larger than T_PLL_ISOPD.
TR_MADCEN	20:18	rw	**Timer for T_MADCEN. Delay MADC enable after IDLE state:** 0_D ... No delay 1_D..7_D ... T_MADCEN = (TR_MADCEN * 64 + 1) * T_{SYS_CLK} Note: T_INIT0 must be larger than T_MADCEN. Typical T_MADCEN = 0.8 µs.
TR_BGEN	23:21	rw	**Timer for T_BGEN. Delay bandgap enable after IDLE state (coming from DS or DS_CONT):** 0_D ... T_BGEN = T_{SYS_CLK} 1_D..7_D ... T_BGEN = (TR_BGEN * 64 + 2) * T_{SYS_CLK} Note: T_WU must be larger than T_BGEN. Typical T_BGEN = 0.8 µs.

4.14 Channel set deep sleep register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSDS_0 Offset address: $00C_H$

Channel set deep sleep register 0 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD			ABB1_AAF_CTRL	RSVD			
r			rw	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		RX1MIX_EN	RX1LOBUF_EN	LO_DIST1_EN	LO_DIST2_EN	RSVD			FDIV_EN	TEMP_MEAS_EN	VCO_EN	RSVD		PD1_EN	TX1_EN
r		rw	rw	rw	rw	r			rw	rw	rw	r		rw	rw

Field	Bits	Type	Description
TX1_EN	0	rw	**Enables the DAC and power amplifier of TX1:** 0_B ... Disabled 1_B ... Enabled
PD1_EN	1	rw	**Enables the power detector of TX1:** 0_B ... Disabled 1_B ... Enabled
RSVD	3:2, 9:7, 19:14, 23:21	r	**Reserved**
VCO_EN	4	rw	**Enables the VCO:** 0_B ... Disabled 1_B ... Enabled
TEMP_MEAS_EN	5	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
FDIV_EN	6	rw	**Enables the VCO frequency divider:** 0_B ... Disabled 1_B ... Enabled Note: DIV output
LO_DIST2_EN	10	rw	**Enables the local oscillator distribution buffer to RX1 channel:** 0_B ... Disabled 1_B ... Enabled
LO_DIST1_EN	11	rw	**Enables the local oscillator distribution buffer to TX1 channel:** 0_B ... Disabled 1_B ... Enabled
RX1LOBUF_EN	12	rw	**Enables the local oscillator buffer to the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
RX1MIX_EN	13	rw	**Enables the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
ABB1_AAF_CTRL	20	rw	**Selection of analog base band anti-aliasing filter frequency on channel 1:** 0_B ... 600 kHz 1_B ... 1 MHz

4.15 Channel set deep sleep register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSDS_1 Offset address: $00D_H$

Channel set deep sleep register 1 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD			MADC_BBCH1_EN	BB_RSTCNT			
r			rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BB_RSTCNT		RSVD			HP1_GAIN	RSVD					TX1_DAC				
rw		r			rw	r					rw				

Field	Bits	Type	Description
TX1_DAC	4:0	rw	**TX1 output power setting:** 0_D ... Minimum output power 31_D ... Maximum output power
RSVD	9:5, 13:11, 23:21	r	**Reserved**
HP1_GAIN	10	rw	**Gain setting of the first stage of the high pass filter of channel 1:** 0_B ... 30 dB 1_B ... 18 dB
BB_RSTCNT	19:14	rw	**Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. T_{BBRST} = BB_RSTCNT * 8 * T_{SYS_CLK}:** 0_D ... No analog baseband reset 1_D ... Minimum value 127_D ... Maximum value

(table continues...)

(continued)

Field	Bits	Type	Description
MADC_BBCH1_EN	20	rw	**Enables the baseband filters, baseband amplifiers and ADC on channel 1:** 0_B ... Disabled 1_B ... Enabled

4.16 Channel set deep sleep register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSDS_2 Offset address: $00E_H$

Channel set deep sleep register 2 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										**VGA_GAIN1**			**HPF_SEL1**		
r										rw			rw		

Field	Bits	Type	Description
HPF_SEL1	2:0	rw	**High pass filter cutoff frequency setting of channel 1:** 0_D ... 20 kHz 1_D ... 40 kHz 2_D ... 80 kHz 3_D ... 140 kHz 4_D ... 160 kHz 5_D ... Reserved 6_D ... Reserved 7_D ... Reserved
VGA_GAIN1	5:3	rw	**VGA gain setting of channel 1:** 0_D ... 0 dB 1_D ... 5 dB 2_D ... 10 dB 3_D ... 15 dB 4_D ... 20 dB 5_D ... 25 dB 6_D ... 30 dB 7_D ... Reserved
RSVD	23:6	r	**Reserved**

4.17 Channel set control deep sleep register

The channel set control register CSCDS is related to the channel set register CSDS.

All bits are used to define a specific power mode.

ISOPD represent a logical isolation layer and is used to disable complete modules (e.g. MADC) while preserving its configuration (no change in the ADC0 register configuration).

CSCDS Offset address: $00F_H$

Channel set control deep sleep register Reset value: $00\ 0960_H$

23–16
RSVD
r

15–12	11	10	9	8	7	6	5	4–0
RSVD	**PLL_ISOPD**	**BG_TMRF_EN**	**RSVD**	**MADC_ISOPD**	**MADC_BG_EN**	**RF_ISOPD**	**ABB_ISOPD**	**RSVD**
r	rw	rw	r	rw	rw	rw	rw	r

Field	Bits	Type	Description
RSVD	4:0, 9, 23:12	r	**Reserved**
ABB_ISOPD	5	rw	**Enables the isolation of all control signals to the ABB:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
RF_ISOPD	6	rw	**Enables the isolation of all control signals to the RF:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
MADC_BG_EN	7	rw	**Enables the bandgap of the MADC:** 0_B ... Disabled 1_B ... Enabled
MADC_ISOPD	8	rw	**Enables the isolation of all control signals to the MADC:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
BG_TMRF_EN	10	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
PLL_ISOPD	11	rw	**Enables the isolation of all control signals to the PLL:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.

4.18 Channel set up x register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSU_0 (x=1-4)

Offset address: 010_H+(x-1)*7

Reset value: 00 0000_H

Bits	23:21	20	19:16
Field	RSVD	ABB1_AAF_CTRL	RSVD
Type	r	rw	r

Bits	15:14	13	12	11	10	9:7	6	5	4	3:2	1	0
Field	RSVD	RX1MIX_EN	RX1LOBUF_EN	LO_DIST1_EN	LO_DIST2_EN	RSVD	FDIV_EN	TEMP_MEAS_EN	VCO_EN	RSVD	PD1_EN	TX1_EN
Type	r	rw	rw	rw	rw	r	rw	rw	rw	r	rw	rw

Field	Bits	Type	Description
TX1_EN	0	rw	**Enables the DAC and power amplifier of TX1:** 0_B ... Disabled 1_B ... Enabled
PD1_EN	1	rw	**Enables the power detector of TX1:** 0_B ... Disabled 1_B ... Enabled
RSVD	3:2, 9:7, 19:14, 23:21	r	**Reserved**
VCO_EN	4	rw	**Enables the VCO:** 0_B ... Disabled 1_B ... Enabled
TEMP_MEAS_EN	5	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
FDIV_EN	6	rw	**Enables the VCO frequency divider:** 0_B ... Disabled 1_B ... Enabled Note: DIV output
LO_DIST2_EN	10	rw	**Enables the local oscillator distribution buffer to RX1 channel:** 0_B ... Disabled 1_B ... Enabled

(table continues...)

(continued)

Field	Bits	Type	Description
LO_DIST1_EN	11	rw	**Enables the local oscillator distribution buffer to TX1 channel:** 0_B ... Disabled 1_B ... Enabled
RX1LOBUF_EN	12	rw	**Enables the local oscillator buffer to the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
RX1MIX_EN	13	rw	**Enables the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
ABB1_AAF_CTRL	20	rw	**Selection of analog base band anti-aliasing filter frequency on channel 1:** 0_B ... 600 kHz 1_B ... 1 MHz

4.19 Channel set up x register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSU_1 (x=1-4)

Offset address: 011_H+(x-1)*7

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
RSVD			**MADC_BBCH1_EN**	**BB_RSTCNT**			
r			rw	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BB_RSTCNT		**RSVD**			**HP1_GAIN**	**RSVD**					**TX1_DAC**				
rw		r			rw	r					rw				

Field	Bits	Type	Description
TX1_DAC	4:0	rw	**TX1 output power setting:** 0_D ... Minimum output power 31_D ... Maximum output power
RSVD	9:5, 13:11, 23:21	r	**Reserved**
HP1_GAIN	10	rw	**Gain of the first stage of the high pass filter of channel 1:** 0_B ... 30 dB 1_B ... 18 dB

(table continues...)

(continued)

Field	Bits	Type	Description
BB_RSTCNT	19:14	rw	**Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. T_{BBRST} = BB_RSTCNT * 8 * T_{SYS_CLK}:** 0_D ... No analog baseband reset 1_D ... Minimum value 127_D ... Maximum value
MADC_BBCH1_EN	20	rw	**Enables the baseband filters, baseband amplifiers and ADC on channel 1:** 0_B ... Disabled 1_B ... Enabled

4.20 Channel set up x register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSU_2 (x=1-4)

Offset address: 012_H+(x-1)*7

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										VGA_GAIN1			HPF_SEL1		
r										rw			rw		

Field	Bits	Type	Description
HPF_SEL1	2:0	rw	**High pass filter cutoff frequency setting of channel 1:** 0_D ... 20 kHz 1_D ... 40 kHz 2_D ... 80 kHz 3_D ... 140 kHz 4_D ... 160 kHz 5_D ... Reserved 6_D ... Reserved 7_D ... Reserved

(table continues...)

(continued)

Field	Bits	Type	Description
VGA_GAIN1	5:3	rw	**VGA gain setting of channel 1:** 0_D ... 0 dB 1_D ... 5 dB 2_D ... 10 dB 3_D ... 15 dB 4_D ... 20 dB 5_D ... 25 dB 6_D ... 30 dB 7_D ... Reserved
RSVD	23:6	r	**Reserved**

4.21 Channel set down x register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSD_0 (x=1-4)

Offset address: 013_H+(x-1)*7

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
RSVD			ABB1_AAF_CTRL	RSVD			
r			rw	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		RX1MIX_EN	RX1LOBUF_EN	LO_DIST1_EN	LO_DIST2_EN	RSVD			FDIV_EN	TEMP_MEAS_EN	VCO_EN	RSVD		PD1_EN	TX1_EN
r		rw	rw	rw	rw	r			rw	rw	rw	r		rw	rw

Field	Bits	Type	Description
TX1_EN	0	rw	**Enables the DAC and power amplifier of TX1:** 0_B ... Disabled 1_B ... Enabled
PD1_EN	1	rw	**Enables the power detector of TX1:** 0_B ... Disabled 1_B ... Enabled
RSVD	3:2, 9:7, 19:14, 23:21	r	**Reserved**

(table continues...)

(continued)

Field	Bits	Type	Description
VCO_EN	4	rw	**Enables the VCO:** 0_B ... Disabled 1_B ... Enabled
TEMP_MEAS_EN	5	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
FDIV_EN	6	rw	**Enables the VCO frequency divider:** 0_B ... Disabled 1_B ... Enabled Note: DIV output
LO_DIST2_EN	10	rw	**Enables the local oscillator distribution buffer to RX1 channel:** 0_B ... Disabled 1_B ... Enabled
LO_DIST1_EN	11	rw	**Enables the local oscillator distribution buffer to TX1 channel:** 0_B ... Disabled 1_B ... Enabled
RX1LOBUF_EN	12	rw	**Enables the local oscillator buffer to the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
RX1MIX_EN	13	rw	**Enables the mixer on channel 1:** 0_B ... Disabled 1_B ... Enabled
ABB1_AAF_CTRL	20	rw	**Selection of analog base band anti-aliasing filter frequency on channel 1:** 0_B ... 600 kHz 1_B ... 1 MHz

4.22 Channel set down x register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSD_1 (x=1-4)

Offset address: 014_H+(x-1)*7

Reset value: 00 0000_H

Bits	Field	Type
23–21	RSVD	r
20	MADC_BBCH1_EN	rw
19–14	BB_RSTCNT	rw
13–11	RSVD	r
10	HP1_GAIN	rw
9–5	RSVD	r
4–0	TX1_DAC	rw

Field	Bits	Type	Description
TX1_DAC	4:0	rw	**TX1 output power setting:** 0_D ... Minimum output power 31_D ... Maximum output power
RSVD	9:5, 13:11, 23:21	r	**Reserved**
HP1_GAIN	10	rw	**Gain of the first stage of the high pass filter of channel 1:** 0_B ... 30 dB 1_B ... 18 dB
BB_RSTCNT	19:14	rw	**Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. T_{BBRST} = BB_RSTCNT * 8 * T_{SYS_CLK}:** 0_D ... No analog baseband reset 1_D ... Minimum value 127_D ... Maximum value
MADC_BBCH1_EN	20	rw	**Enables the baseband filters, baseband amplifiers and ADC on channel 1:** 0_B ... Disabled 1_B ... Enabled

4.23 Channel set down x register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

CSD_2 (x=1-4)

Offset address: 015_H+(x-1)*7

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										**VGA_GAIN1**			**HPF_SEL1**		
r										rw			rw		

Field	Bits	Type	Description
HPF_SEL1	2:0	rw	**High pass filter cutoff frequency setting of channel 1:** 0_D … 20 kHz 1_D … 40 kHz 2_D … 80 kHz 3_D … 140 kHz 4_D … 160 kHz 5_D … Reserved 6_D … Reserved 7_D … Reserved
VGA_GAIN1	5:3	rw	**VGA gain setting of channel 1:** 0_D … 0 dB 1_D … 5 dB 2_D … 10 dB 3_D … 15 dB 4_D … 20 dB 5_D … 25 dB 6_D … 30 dB 7_D … Reserved
RSVD	23:6	r	**Reserved**

4.24 Channel set control x register

The channel set control register CSCx is related to the channel set register CSUx.

Besides REPC, all other bits are used to define a specific power mode.

ISOPD represent a logical isolation layer and is used to disable complete modules (e.g. MADC) while preserving its configuration (no change in the ADC0 register configuration).

REPC is one parameter used to define the modulation sequence.

CSC (x=1-4) Offset address: 016_H+(x-1)*7

Reset value: 00 0960_H

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				**PLL_ISOPD**	**BG_TMRF_EN**	**RSVD**	**MADC_ISOPD**	**MADC_BG_EN**	**RF_ISOPD**	**ABB_ISOPD**	**CS_EN**	**REPCS**			
r				rw	rw	r	rw	rw	rw	rw	rw	rw			

Field	Bits	Type	Description
REPCS	3:0	rw	**Repetition factor of channel set:** 0_D..15_D … RC = 2^{REPC}

(table continues...)

(continued)

Field	Bits	Type	Description
CS_EN	4	rw	**Enables channel set (CS):** 0_B ... Disabled 1_B ... Enabled Note: At least the first channel set should be used (CSC1:CS_EN = 1_B).
ABB_ISOPD	5	rw	**Enables the isolation of all control signals to the ABB:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
RF_ISOPD	6	rw	**Enables the isolation of all control signals to the RF:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
MADC_BG_EN	7	rw	**Enables the bandgap of the MADC:** 0_B ... Disabled 1_B ... Enabled
MADC_ISOPD	8	rw	**Enables the isolation of all control signals to the MADC:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.
RSVD	9, 23:12	r	**Reserved**
BG_TMRF_EN	10	rw	**Enables the temperature sensor:** 0_B ... Disabled 1_B ... Enabled
PLL_ISOPD	11	rw	**Enables the isolation of all control signals to the PLL:** 0_B ... Disabled 1_B ... Enabled Note: In case the isolation is enabled all control signals are connected to 0_B.

4.25 Chirp control register 0

Register CCR0 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

CCR0 Offset address: $02C_H$

Chirp control register 0 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
TR_INIT1_MUL		**TR_INIT1**					
rw		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_INIT1		**REPT**				**CONT_MODE**	**TR_END**								
rw		rw				rw	rw								

Field	Bits	Type	Description
TR_END	8:0	rw	**Timer for T_END. Waiting time after the generation of a ramp:** 0_D ... T_END = 5 * T_{SYS_CLK} 1_D..511_D ... T_END = (TR_END * 8 + 5) * T_{SYS_CLK}
CONT_MODE	9	rw	**Continuous mode. After last channel set repetition RT, the specified power mode (CCR1:PD_MODE) is applied and** 0_B ... the FSM stops immediately 1_B ... after T_FED the next channel set is applied Note: In case DS power mode (CCR1:PD_MODE = 2_D) is selected and the continuous mode is not active the system clock is disabled internally.
REPT	13:10	rw	**Repetition factor for a channel set in a frame:** 0_D..15_D ... RT = 2^{REPT} **Note:** The host should program the maximum value 15_D as default.
TR_INIT1	21:14	rw	**Timer for T_INIT1:** 0_D ... T_{SYS_CLK} 1_D..255_D ... T_INIT1 = (TR_INIT1 * $2^{TR\_INIT\_MUL}$ * 8 + TR_INIT_MUL + 3) * T_{SYS_CLK} Note: These values are used for every up and every down-ramp. Note: After the wake-up period the timer for T_INIT1 should be at least 15 µs according to the typical ADC calibration time.
TR_INIT1_MUL	23:22	rw	**Timer multiplier factor for T_INIT1:** 0_D..3_D ... $2^{TR\_INIT1\_MUL}$

4.26 Chirp control register 1

Register CCR1 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

CCR1 Offset address: $02D_H$

Chirp control register 1 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
TR_FED_MUL					TR_FED		
rw					rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_FED					PD_MODE		TR_START								
rw					rw		rw								

Field	Bits	Type	Description
TR_START	8:0	rw	**Timer for T_START. Ramp start delay defines the delay before generating the ramp:** $0_D..511_D$ ... T_START = (TR_START * 8 + 10) * T_{SYS_CLK}
PD_MODE	10:9	rw	**Power down mode. After the last repetition RT, the chip enters the defined power mode (during T_FED):** 0_D ... Keep the same power mode (CSx + CSCx) 1_D ... Change to IDLE power mode (CSI + CSCI) 2_D ... Change to DS power mode (CSDS + CSCDS) 3_D ... Reserved
TR_FED	18:11	rw	**Timer for T_FED:** 0_D ... T_{SYS_CLK} $1_D..255_D$ ... T_FED = (TR_FED * $2^{TR\_FED\_MUL}$ * 8 + TR_FED_MUL + 3) * T_{SYS_CLK}
TR_FED_MUL	23:19	rw	**Timer multiplier factor for T_FED:** $0_D..31_D$ ... $2^{TR\_FED\_MUL}$

4.27 Chirp control register 2

Register CCR2 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

CCR2 Offset address: $02E_H$

Chirp control register 2 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
FRAME_LEN							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_LEN				MAX_FRAME_CNT											
rw				rw											

Field	Bits	Type	Description
MAX_FRAME_CNT	11:0	rw	**Maximum number of frames to be executed. When MAX_FRAME_CNT is reached, the shape generation is stopped, and the chip is set to deep sleep power mode. The next frame can be triggered only after a reset (eg. FSM_RESET). The frame generation can be stopped at any time by resetting the FSM (see MAIN:FSM_RESET).** 0_D ... Endless frame generation 1_D ... 1 frame is generated 4095_D ... 4095 frames are generated
FRAME_LEN	23:12	rw	**Frame Length specifies the number of shape groups in a frame. When specified frame length is reached the frame counter is incremented and the shape group counter is reset:** 0_D ... Minimum value (1 shape group) 4095_D ... Maximum value (4096 shape groups)

4.28 Chirp control register 3

Register CCR3 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

CCR3 Offset address: $02F_H$

Chirp control register 3 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
TR_INIT0_MUL		**TR_INIT0**					
rw		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_INIT0	**TR_SSTART**						**TR_PAEN**								
rw	rw						rw								

Field	Bits	Type	Description
TR_PAEN	8:0	rw	**Timer for T_PAEN. Delay time after PLL start and power amplifier enable:** 0_D ... Reserved $1_D..511_D$ ... T_PAEN = TR_PAEN * 8 * T_{SYS_CLK}
TR_SSTART	14:9	rw	**Timer for T_SSTART. Delay time after power amplifier enable and first trigger to ADC:** $0_D..63_D$ ... T_SSTART = (TR_SSTART * 8 + 1) * T_{SYS_CLK}

(table continues...)

(continued)

Field	Bits	Type	Description
TR_INIT0	21:15	rw	**Timer for T_INIT0:** 0_D ... T_{SYS_CLK} $1_D..255_D$ ... T_INIT0 = (TR_INIT0 * $2^{TR\_INIT0\_MUL}$ * 8 + TR_INIT0_MUL + 3) * T_{SYS_CLK} Note: After the wake-up period the timer for T_INIT0 should be at least 70 µs according to the typical ADC calibration time.
TR_INIT0_MUL	23:22	rw	**Timer multiplier for T_INIT0:** $0_D..3_D$ ... $2^{TR\_INIT0\_MUL}$

4.29 PLL shape x register 0

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_0 (x=1-4)

Offset address: 030_H+(x-1)*8

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
FSU							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSU															
rw															

Field	Bits	Type	Description
FSU	23:0	rw	**Chirp start frequency for up chirp. Sigma delta start frequency for the ramp generator:** 0_D ... Sawtooth shape Note: In case FSD = 0_D, RSD = 0_D, and RTD = 0_D, the fast sawtooth shape is enabled. In all other cases the triangular shape is enabled.

4.30 PLL shape x register 1

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_1 (x=1-4)

Offset address: 031_H+(x-1)*8

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
RSU							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSU															
rw															

Field	Bits	Type	Description
RSU	23:0	rw	**Ramp step up chirp. A ramp step is the RF frequency difference added to the actual frequency during single clock cycle time of T_{SYS_CLK}. In case the value is zero the RF frequency will be almost constant during the RTU time.** Bit(23) represents the sign for the ramp: 0_D ... Up chirp 1_D ... Down chirp

4.31 PLL shape x register 2

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_2 (x=1-4)

Offset address: 032_H+(x-1)*8
Reset value: 00 0000_H

23	22	21	20	19	18	17	16
TR_EDU							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		RTU													
r		rw													

Field	Bits	Type	Description
RTU	13:0	rw	**Ramp time for up chirp. RTU defines the number of clock cycles for the up chirp. The actual ramp time is:** 0_D ... Timer disabled (needed for fast down chirp) 1_D..16383_D ... T_RAMP = RTU * 8 * T_{SYS_CLK}
RSVD	15:14	r	**Reserved**
TR_EDU	23:16	rw	**Timer for T_EDU. End of chirp delay applied after every up chirp:** 0_D ... T_EDU = 2 * T_{SYS_CLK} 1_D..255_D ... T_EDU = (TR_EDU * 8 + 5) * T_{SYS_CLK}

4.32 PLL shape x register 3

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_3 (x=1-4)

Offset address: 033_H+(x-1)*8

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
APD							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APD				APU											
rw				rw											

Field	Bits	Type	Description
APU	11:0	rw	**Number of samples for an up chirp of a single ADC:** 0_D..4095_D ... Number of samples
APD	23:12	rw	**Number of samples for a down chirp of a single ADC:** 0_D..4095_D ... Number of samples

4.33 PLL shape x register 4

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_4 (x=1-4)

Offset address: 034_H+(x-1)*8

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
FSD							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSD															
rw															

Field	Bits	Type	Description
FSD	23:0	rw	**Chirp start frequency for down chirp. Sigma delta start frequency for the ramp generator:** 0_D ... Sawtooth shape Note: In case FSD = 0_D, RSD = 0_D, and RTD = 0_D, the fast sawtooth shape is enabled. In all other cases the triangular shape is enabled.

4.34 PLL shape x register 5

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_5 (x=1-4)

Offset address: 035_H+(x-1)*8

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
RSD							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSD															
rw															

Field	Bits	Type	Description
RSD	23:0	rw	**Ramp step down chirp. A ramp step is the RF frequency difference added to the actual frequency during single clock cycle time of T_{SYS_CLK}. In case the value is zero the RF frequency will be almost constant during the RTD time.** Bit(23) represents the sign for the ramp: 0_D ... Up chirp 1_D ... Down chirp

4.35 PLL shape x register 6

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_6 (x=1-4)

Offset address: 036_H+(x-1)*8

Reset value: 00 0000_H

23	22	21	20	19	18	17	16
TR_EDD							
rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		RTD													
r		rw													

Field	Bits	Type	Description
RTD	13:0	rw	**Ramp time for down chirp. RTD defines the number of clock cycles for the down chirp. The actual ramp time is:** 0_D ... Timer disabled (needed for fast down chirp) 1_D..16383_D ... T_RAMP = RTD * 8 * T_{SYS_CLK}

(table continues...)

(continued)

Field	Bits	Type	Description
RSVD	15:14	r	**Reserved**
TR_EDD	23:16	rw	**Timer for T_EDD. End of chirp delay applied after every down chirp:** 0_D ... T_EDD = 2 * T_{SYS_CLK} 1_D..255_D ... T_EDD = (TR_EDD * 8 + 5) * T_{SYS_CLK}

4.36 PLL shape x register 7

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

PLL_7 (x=1-4)

Offset address: 037_H+(x-1)*8
Reset value: 00 0000_H

23	22	21	20	19	18	17	16
TR_SED_MUL					TR_SED		
rw					rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TR_SED					PD_MODE		CONT_MODE	RSVD			SH_EN	REPS			
rw					rw		rw	r			rw	rw			

Field	Bits	Type	Description
REPS	3:0	rw	**Repetition factor for a single shape:** 0_D..15_D ... RS = 2^{REPS}
SH_EN	4	rw	**Enable shape:** 0_B ... Disabled 1_B ... Enabled Note: Values for disabled shapes are ignored. At least the first shape needs to be enabled (PLL1_7:SH_EN = 1_B). Fields for unused shapes must be programmed to its default reset value.
RSVD	7:5	r	**Reserved**
CONT_MODE	8	rw	**Continuous mode. After last shape repetition RS, the specified power mode (PLLy_7:PD_MODE) is applied and** 0_B ... the FSM stops immediately 1_B ... after T_SED the next shape set is applied
PD_MODE	10:9	rw	**Power down mode. After the last repetition RS the chip enters the defined power mode (during T_SED):** 0_D ... Keep the same power mode (CSx + CSCx) 1_D ... Change to IDLE power mode (CSI + CSCI) 2_D ... Change to DS power mode (CSDS + CSCDS) 3_D ... Reserved

(table continues...)

(continued)

Field	Bits	Type	Description
TR_SED	18:11	rw	**Timer for T_SED:** 0_D ... T_{SYS_CLK} $1_D..255_D$ ... T_SED = (TR_SED * $2^{TR\_SED\_MUL}$ * 8 + TR_SED_MUL + 3) * T_{SYS_CLK}
TR_SED_MUL	23:19	rw	**Timer multiplier for T_SED:** $0_D..31_D$ ... $2^{TR\_SED\_MUL}$

4.37 Sensor ADC register

On chip sensor register settings.

ADC1 Offset address: 050_H

Sensor ADC register Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
SENSOR_SEL		TR_PSSTART					
rw		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															
r															

Field	Bits	Type	Description
RSVD	15:0	r	**Reserved**
TR_PSSTART	21:16	rw	**Delay after pa_on after the power amplifier is activated and power sensing is started.** T_PSSTART = TR_PSSTART * 8 * T_{SYS_CLK} 0_D ... Minimum delay 50_D ... Maximum delay $51_D..63_D$ ... Reserved Note: T_PSSTART ≤ T_SSTART - 1.3 µs (with 0.3 µs for ADC conversion).
SENSOR_SEL	23:22	rw	**Sensor selection for ADC input:** 0_D ... RX channel (CSx:MADC_BBCH1_EN must be set) 1_D ... Power sensor (CSx:PD1_EN must be set) 2_D ... Temperature sensor (CSx:TEMP_MEAS_EN must be set) 3_D ... IFx

4.38 RF test register 0

Register contains several bits used to enable dedicated paths for self-test.

RFT0 Offset address: 055_H

RF test register 0 Reset value: $00\ 1F40_H$

23	22	21	20	19	18	17	16
RF_TEST_MODE		**RSVD**			**TEST_SIG_IF1_EN**	**RSVD**	
rw		r			rw	r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	**TEST_SIG_RF1_EN**	**RFTSIGCLK_DIV_EN**	**RFTSIGCLK_DIV**												
r	rw	rw	rw												

Field	Bits	Type	Description
RFTSIGCLK_DIV	12:0	rw	**RF test tone signal divider value. $f_{RFTST} = f_{SYS\_CLK}$ / RFTSIGCLK_DIV:** 0_D ... Reserved 1_D ... Reserved 2_D ... Minimum value 8191_D ... Maximum value
RFTSIGCLK_DIV_EN	13	rw	**Enable the RF test tone signal output to the baseband:** 0_B ... Disabled 1_B ... Enabled
TEST_SIG_RF1_EN	14	rw	**Enable test signal for receiver RF1:** 0_B ... Disabled 1_B ... Enabled
RSVD	17:15, 21:19	r	**Reserved**
TEST_SIG_IF1_EN	18	rw	**Enable test signal for IF channel 1:** 0_B ... Disabled 1_B ... Enabled
RF_TEST_MODE	23:22	rw	**RF test mode.** 0_B ... Test mode disabled 1_B ... Mode 1: rf_bb:tx1_en toggles between 0_B and CSx:TX1_EN with f_{RFTST} 2_B ... Mode 2: rf_bb:tx1_dac toggles between 0_B and CSx:TX1_DAC with f_{RFTST} 3_B ... Mode 3: rf_bb:test_sig_rf1 toggles between 0_B and RFT0:TEST_SIG_RF1_EN with f_{RFTST} Note: RF test mode is only active for MAIN:CW_MODE = 1_B. Note: RFTSIGCLK_DIV must be programmed and RFTSIGCLK_DIV_EN must be enabled.

4.39 EFUSE register 0

Register contains several bits used to read out eFuses.

EFUSE0 — Offset address: 057_H

EFUSE register 0 — Reset values see: Table 23

23–20	19–16
RSVD	RSVD
r	r

15	14	13	12	11	10	9	8	7	6	5	4	3–2	1–0
RSVD	EFUSE_SENSE	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EFUSE_EN	RSVD	RSVD
r	w	r	r	r	r	r	r	r	r	r	rw	r	r

Field	Bits	Type	Description
RSVD	3:0, 13:5, 23:15,	r	**Reserved**
EFUSE_EN	4	rw	**Enable EFUSE:** 0_B ... Disabled 1_B ... Enabled
EFUSE_SENSE	14	w	**Start EFUSE read sequence:** 0_B ... No effect 1_B ... Executes EFUSE reading and clears this bit

Table 23 Reset values of EFUSE0

Reset type	Reset value	Note
Reset	X000 0000 0000 0010 0000 0000_B	

4.40 EFUSE register 1

Register contains several bits used to read out eFuses.

EFUSE1 — Offset address: 058_H

EFUSE register 1 — Reset value: 00 0300_H

23–16
RSVD
r

15–10	9	8–0
RSVD	EFUSE_READY	RSVD
r	rh	r

Field	Bits	Type	Description
RSVD	8:0, 23:10	r	**Reserved**
EFUSE_READY	9	rh	**EFUSE ready:** 0_B ... Not ready 1_B ... Ready Note: Only valid after EFUSE_SENSE was executed! Result stored in CHIP_ID0 and CHIP_ID1.

4.41 PLL test register 0

The setting in this register should be used when the CW mode is enabled. Sigma delta modulator (SDM) is bypassed in CW mode.

PDFT0 Offset address: 059_H

PLL test register 0 Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										**BYPSDM**				**BYPSDMEN**	**BYPRMPEN**
r										rw				rw	rw

Field	Bits	Type	Description
BYPRMPEN	0	rw	**Enable bypass ramp generator:** 0_B ... Ramp generator enabled 1_B ... Ramp generator disabled (bypassed)
BYPSDMEN	1	rw	**Enable bypass for sigma delta modulator:** 0_B ... Disabled 1_B ... Enabled
BYPSDM	5:2	rw	**Value used for bypassed sigma delta modulator:** 0_D ... Minimum value 15_D ... Maximum value
RSVD	23:6	r	**Reserved**

4.42 Chip ID register 0

The unique chip ID consists of 48 bits. Register CHIP_ID0 provides the first 24bits of the ID.

CHIP_ID0 Offset address: $05D_H$

Chip ID register 0 Reset value: $FF\ FFFF_H$

23	22	21	20	19	18	17	16
CHIP_ID							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIP_ID															
rh															

Field	Bits	Type	Description
CHIP_ID	23:0	rh	**Chip ID[23:0].** Note: Valid after EFUSE_SENSE was executed.

4.43 Chip ID register 1

The unique chip ID consists of 48 bits. Register CHIP_ID1 provides the second 24bits of the ID.

CHIP_ID1 Offset address: $05E_H$

Chip ID register 1 Reset value: $FF\ FFFF_H$

23	22	21	20	19	18	17	16
CHIP_ID							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIP_ID															
rh															

Field	Bits	Type	Description
CHIP_ID	23:0	rh	**Chip ID[47:24].** Note: Valid after EFUSE_SENSE was executed.

4.44 Clock input register

CLK_IN register bit fields are used to program the input clock path.

CLK_IN Offset address: $05F_H$

Clock input register Reset value: $00\ 0400_H$

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				IRQ_FD_SEL	DC_OUT_ADJ				DC_IN_ADJ					CLK_SEL	
r				rw	rw				rw					rw	

Field	Bits	Type	Description
CLK_SEL	1:0	rw	**Selection of input clock frequency and clock path:** 0_D ... Frequency doubler bypassed 1_D ... Frequency doubler without DC_IN 2_D ... Frequency doubler with DC_IN 3_D ... Frequency doubler with DC calibration for system clock and without DC calibration for PLL clock **Note:** It is important to program FD register first and enable the system clock afterwards by programming PACR2(23) register.
DC_IN_ADJ	6:2	rw	**Duty cycle of input clock can be adjusted before entering the internal clock doublers. This adjustment can be used for equalizing the input clock to a DC of 50 % by applying a positive or negative clock delay time to the input clock (from OSC_CLK pin). In case if MSB of DC_IN_ADJ = 0_B a positive delay is used, while a MSB of DC_IN_ADJ = 1_B applies a negative delay. Delay times are in steps of 125 ps.:** 0_D ... +0.23 ns (minimal positive adjustment) ... 15_D ... +2.1 ns (maximal positive adjustment) 16_D ... -0.23 ns (minimal negative adjustment) ... 31_D ... -2.1 ns (maximal negative adjustment)
DC_OUT_ADJ	10:7	rw	**Duty cycle adjustment of clock doubler for system clock. The system clock pulse width can be adjusted by 15 delay cells, starting from 4.3 ns up to 4.3 ns + 15 * 0.45 ns. The duty cycle then is DC_{SYS_CLK} = (4.3 ns + DC_OUT_ADJ * 0.4 ns) / T_{SYS_CLK}.** 0_D ... 4.3 ns 1_D ... 4.7 ns ... 4_D ... 6.10 ns (preferred value for e.g. 80 MHz) 5_D ... 6.55 ns (preferred value for e.g. 76.8 MHz) ... 15_D ... 11.05 ns Note: The duty cycle of the system clock can be adjusted via CLK_IN:DC_OUT_ADJ and can be monitored via IRQ pin.
IRQ_FD_SEL	11	rw	**Select frequency doubler output at IRQ pin:** 0_B ... Normal irq functionality at IRQ pin 1_B ... Frequency doubler output at IRQ pin Note: Frequency doubler has higher priority as interrupt.
RSVD	23:12	r	**Reserved**

4.45 Wake up register

Wake up register can be used as chirp offset in case multiple devices are used and triggered together via SPI broadcast.

WU Offset address: 060_H

Wake up register Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				**TR_TWKUP_MUL**				**TR_TWKUP**							
r				rw				rw							

Field	Bits	Type	Description
TR_TWKUP	7:0	rw	**Timer for T_WU:** 0_D ... T_{SYS_CLK} $1_D..255_D$ ... T_WU = (TR_WKUP * $2^{TR\_WKUP\_MUL}$ * 8 + TR_WKUP_MUL + 3) * T_{SYS_CLK} Note: T_WU_{TYP} = 1 ms
TR_TWKUP_MUL	11:8	rw	**Timer multiplier factor for T_WU:** $0_D..15_D$ ... $2^{TR\_WKUP\_MUL}$
RSVD	23:12	r	**Reserved**

4.46 Status register 0

The status register STAT0 provides the actual value of some specific internal states. However it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after e.g. 100 µs.

STAT0 Offset address: 061_H

Status register 0 Reset value: $00\ 0008_H$

23	22	21	20	19	18	17	16
RSVD							
r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		**SH_IDX**			**CH_IDX**			**PM**			**RSVD**	**LDO_RDY**	**ADC_BGUP**	**ADC_RDY**	**RSVD**
r		rh			rh			rh			r	rh	rh	rh	r

Field	Bits	Type	Description
RSVD	0, 4, 23:14	r	**Reserved**
ADC_RDY	1	rh	**ADC status:** 0_B ... Not ready 1_B ... Ready

(table continues...)

(continued)

Field	Bits	Type	Description
ADC_BGUP	2	rh	**ADC bandgap reference power up status:** 0_B ... Not ready 1_B ... Ready
LDO_RDY	3	rh	**LDO status (V_{DDC} above the threshold):** 0_B ... Not ready 1_B ... Ready
PM	7:5	rh	**Power mode of the FSM:** 0_D ... Deep sleep mode (after reset) 1_D ... Active mode 2_D ... Interchirp mode 3_D ... Idle mode 4_D ... Reserved 5_D ... Deep sleep mode 6_D ... Reserved 7_D ... Reserved
CH_IDX	10:8	rh	**Channel set index enabled by the FSM:** 0_D ... CSU1 1_D ... CSD1 2_D ... CSU2 3_D ... CSD2 4_D ... CSU3 5_D ... CSD3 6_D ... CSU4 7_D ... CSD4
SH_IDX	13:11	rh	**Shape index enabled by the FSM:** 0_D ... PLLU1 1_D ... PLLD1 2_D ... PLLU2 3_D ... PLLD2 4_D ... PLLU3 5_D ... PLLD3 6_D ... PLLU4 7_D ... PLLD4

4.47 Sensor ADC result register

The register SENSOR_RESULT is used to monitor the temperature as well as the power.

SENSOR_RESULT Offset address: 062_H

Sensor ADC result register Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
TEMP_RESULT							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMP_RESULT				**POWER_RESULT**											
rh				rh											

Field	Bits	Type	Description
POWER_RESULT	11:0	rh	**Power sensor result**
TEMP_RESULT	23:12	rh	**Temperature sensor result**

4.48 FIFO status register

The FIFO status register FSTAT is used to monitor the FIFO. It should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after e.g. 100 µs.

FSTAT Offset address: 063_H

FIFO status register Reset value: $10\ 0000_H$

23	22	21	20	19	18	17	16
FOF_ERR	**FULL**	**CREF**	**EMPTY**	**FUF_ERR**	**BURST_ERR**	**CLK_NUM_ERR**	**RSVD**
rh	rh	rh	rh	rh	rh	rh	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	**RAM_PWR_DOWN**	**FILL_STATUS**													
r	rh	rh													

Field	Bits	Type	Description
FILL_STATUS	13:0	rh	**FIFO fill status:** 0000_H ... FIFO is empty 0400_H ... FIFO is 50% filled 0800_H ... FIFO is full Note: This bit field is for debugging only. It should not be evaluated while the ADC is sampling and filing up the FIFO as the data are not stable. Can be evaluated when the FSM status is held, for example, after an FSM reset or in a specific power mode, Deep Sleep mode.

(table continues...)

(continued)

Field	Bits	Type	Description
RAM_PWR_DOWN	14	rh	**RAM power down state:** 0_B ... RAM powered up 1_B ... RAM powered down
RSVD	16:15	r	**Reserved**
CLK_NUM_ERR	17	rh	**Clock number error bit is set when SPI clock number does not match the expected number of clock cycles:** 0_B ... No error 1_B ... Clock number error Note: Bit will be reset after HW or SW reset.
BURST_ERR	18	rh	**In case of burst error this bit is set:** 0_B ... No error 1_B ... Burst error Note: Bit will be reset after HW or SW reset.
FUF_ERR	19	rh	**FIFO underflow error shows if the host was reading more sampling data from the FIFO than available. The flag is also shown in GSR0 as a part of FIFO over or underflow error bit FOU_ERR:** 0_B ... No FIFO underflow 1_B ... FIFO underflow Note: Bit will be reset after HW, SW or FIFO reset.
EMPTY	20	rh	**FIFO empty status:** 0_B ... FIFO not empty 1_B ... FIFO empty
CREF	21	rh	**FIFO fill status exceeds compare reference:** 0_B ... Fill status below reference 1_B ... Fill status above reference
FULL	22	rh	**FIFO full status:** 0_B ... FIFO not full 1_B ... FIFO full
FOF_ERR	23	rh	**FIFO overflow error bit shows if more sample data are transferred to the FIFO than FIFO memory locations are available to store the data. The flag is also shown in GSR0 as a part of FIFO over or underflow error bit FOU_ERR:** 0_B ... No FIFO overflow 1_B ... FIFO overflow Note: Bit will be reset after HW, SW or FIFO reset.

4.49 Global status register

The global status register GSR0 is related to SPI read/write monitoring.

GSR0 0_H

Global status register Reset value: $x1110100_B$

7	6	5	4	3	2	1	0
RSVD				**FOU_ERROR**	**MISO_HS_READ**	**SPI_BURST_ERROR**	**CLK_NUMBER_ERROR**
r				rh	rh	rh	rh

Field	Bits	Type	Description
CLK_NUMBER_ERROR	0	rh	**Defined within the SPI chapter:** 0_B ... No clock number error 1_B ... Error condition occurred
SPI_BURST_ERROR	1	rh	**SPI burst error defined within the SPI chapter:** 0_B ... No burst read/write error 1_B ... Burst error
MISO_HS_READ	2	rh	**SPI MISO high speed mode:** 0_B ... Not active 1_B ... Active
FOU_ERROR	3	rh	**Shows if FIFO overflow or underflow condition occurred. The error will be cleared after the following resets: FIFO reset or SW reset or HW reset:** 0_B ... No error 1_B ... Error condition occurred
RSVD	7:4	r	**Reserved**

5 Data organization and SPI interface

5.1 Data header

The main FSM is capable of generating a data header to be attached to the actual radar raw data. The structure of the header is shown in the following figure and table. The data header can be disabled by controlling the bit SFCTL:PREFIX_EN (see Chapter 4.9).

A sync-word is sent at the beginning of each acquisition to make the radar raw-data from each shape unique. This can be useful in case of broken communication with the application processor or in case of errors. Supposing the FIFO will generate a “FIFO overflow flag” the sync-word 0x000000 can be evaluated by the host controller and used to resync with the BGT60UTR11AIP and discard the data received before this sync word (if header or sync-word not used then the controller should reset the FIFO, discarding the actual FIFO data). On “FIFO underflow flag”, the received data bits from the host are 111111111111_B.

Following, the header includes also the frame counter and shape group counter, as well as the actual APU/APD value (see PLL shape x register 3) and temperature value.

Data Header

	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
0	SYNC_WORD1 = 0x000	SYNC_WORD0 = 0x000
1	FRAME_CNT[11:0]	SHAPE_GRP_CNT[11:0]
2	TEMP_RESULT	POWER_RESULT
3	Data 0	Data 1

Figure 20 Data header

Table 24 Data header description

Symbol	Word	Bits	Description	RST
SYNC_WORD1	#0	23:12	The sync-word can be used to identify the start of a new chirp. In case the MADC will output also a sequence of 0x000000, to make the sync-word unique, the data from the MADC will be automatically changed to 0x001 before transferring it to the FIFO.	0_D
SYNC_WORD0	#0	11:0	See SYNC_WORD1.	0_D
FRAME_CNT	#1	23:12	Same as STAT1:FRAME_CNT (see Status register 1)	0_D
SHAPE_GRP_CNT	#1	11:0	Same as STAT1:SHAPE_GRP_CNT (see Status register 1).	0_D
TEMP_RESULT	#2	23:12	Temperature value from the end of the previous chirp.	0_D
POWER_RESULT	#2	11:0	Power value from the beginning of the shape.	0_D
DATA0	#3	23:12	MSB data (see Chapter 5.2).	
DATA1	#3	11:0	LSB data (see Chapter 5.2).	

5.2 FIFO and data flow

The memory in the BGT60UTR11AIP is based on a *FIFO*. The FIFO consists of a circular shift register organized in 2048 words of 24 bits each. Following data flow mode from multi *ADC* to the FIFO is supported by the *FSM* (see following figure):

- Mode 1: One ADC active
  - Data from 1st sample, 12 bits, are temporarily stored in a buffer
  - When the 2nd sample, 12 bits, are available, both, 1st and 2nd (24 bits), are stored into one data word

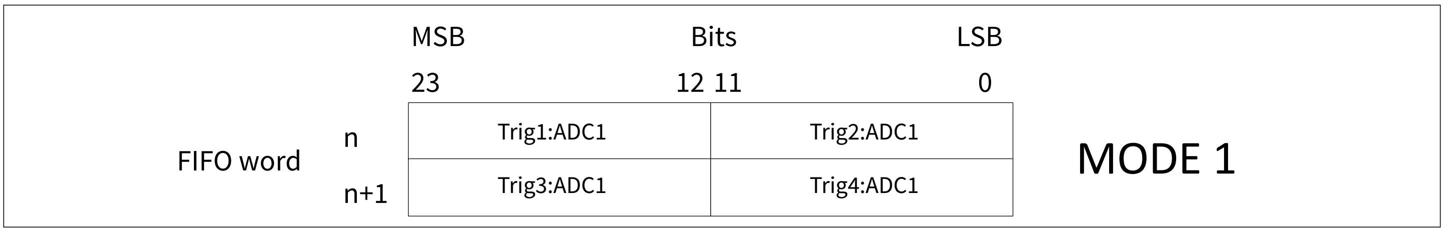

Figure 21 **FIFO organization**

Readout from the FIFO should be executed from the host controller using memory address with correct data length. Data length can be derived from the data header or based on the "sync-word".

***Note**: An illegal write to memory address space will lead to lost* FIFO *data!*

5.3 SPI – Serial Peripheral Interface module

The *SPI* is the communication interface between the host and the BGT60UTR11AIP. It enables the host to read from, or write to (program) the registers as well as reading from the FIFO.

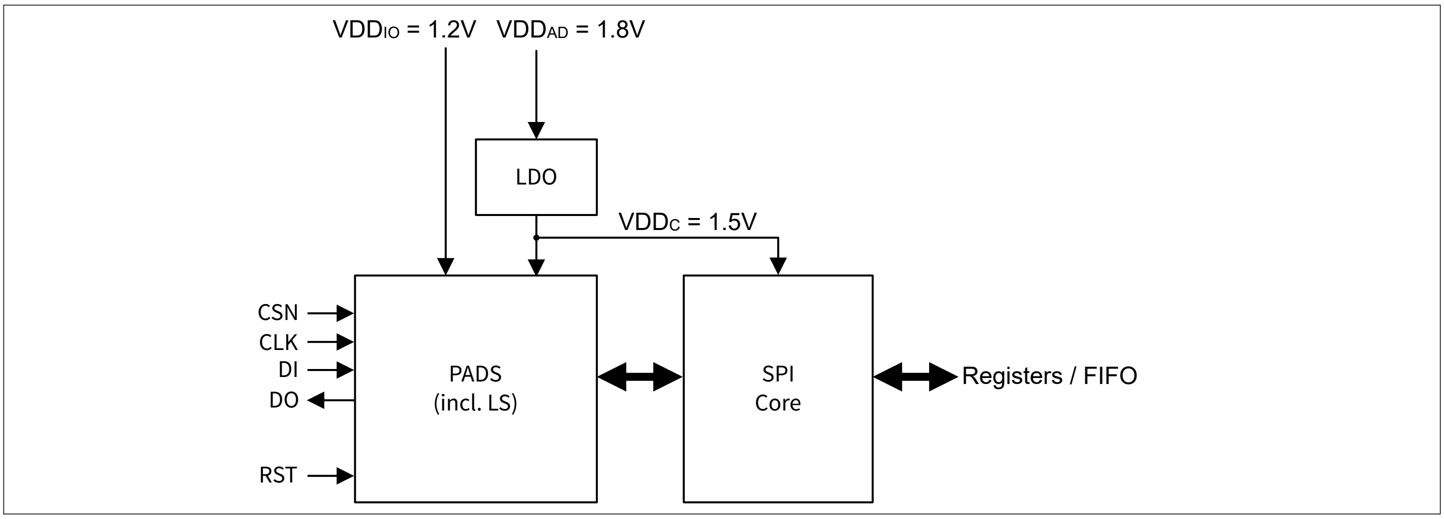

Figure 22 **SPI module**

BGT60UTR11AIP device features four I/O pins for SPI communication and one for chip reset. DIO pins are pulled up to logic high inside the pad.

- CSN to be connected to SS of the SPI master
- CLK to be connected to CLK of the SPI master
- DI to be connected to MOSI of the SPI master
- DO to be connected to MISO of the SPI master
- RST to be connected to reset

Table 25 **SPI pins**

Pin name	**Standard** SPI **mode function**	**Remarks**
CSN	CSN	Chip select not
CLK	CLK	SPI clock
DI	MOSI	HiZ, bidirectional

(table continues...)

Table 25 (continued) SPI pins

Pin name	Standard SPI mode function	Remarks
DO	MISO	HiZ, bidirectional
RST	RESET	HiZ

The SPI interface can be clocked up to 50 MHz. To meet the timing requirements for higher SPI clock frequencies (e.g., >25 MHz) the BGT60UTR11AIP device offers an additional high speed mode (SFCTL:MISO_HS_RD) which increase the timing budget on SPI master side by sending out data via DO with the rising edge instead of the falling edge of the CLK.

5.3.1 Standard SPI timing

The timing diagram for normal SPI mode (SFCTL:MISO_HS_RD = 0_B) is presented in the following figure. A *SPI* transfer is started with a falling edge of chip select signal CSN generated by the SPI master. At the same time, the SPI master shall drive the level of the data input signal DI (*master out slave in (MOSI)*) according to the first bit. Also, with the falling edge of the chip select signal CSN the SPI slave applies the level of the data on the output signal DO (*master in slave out (MISO)*) according to the first bit which shall be transferred to the SPI master, the level becomes stable after the period *t*(ds). The SPI master has to wait for the time *t*(L) before the clock signal CLK can be generated.

With the rising edge of CLK the SPI slave captures the level of DI. The SPI master must keep the DI level stable for *t*(sis) before and for *t*(sih) after the rising edge of CLK to ensure valid setup and hold time of the SPI slave. With the falling edge of CLK the SPI master shall set the level of DI according to the next bit the master wants to send.

The SPI master is supposed to read the level of DO with the rising edge of CLK. The SPI slave keeps the DO level stable for *t*(soh) after the falling edge of CLK. With the falling edge of CLK the SPI slave drives the level of DO according to the next bit, DO becomes stable after latest *t*(sov).

After the last bit has been transferred and CLK has gone to low level, the SPI master must set CSN to high level to stop the transfer. The master must take care that the period between the last rising edge of CLK and the rising edge of CSN is not shorter than *t*(T). Within the period *t*(dh) after the rising edge of CSN the SPI slave drives DO to high impedance state again.

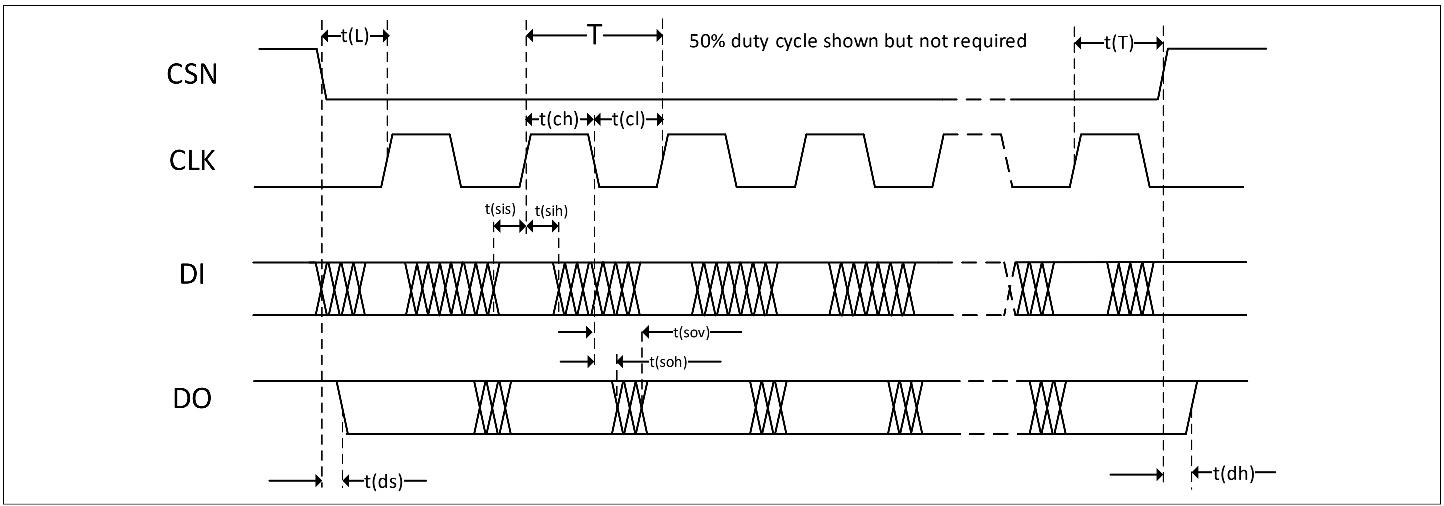

Figure 23 SPI interface timing diagram for SFCTL:MISO_HS_RD = 0_B

BGT60UTR11AIP can operate at SPI clock frequencies up to 50 MHz, but the maximum achievable SPI clock frequency is limited by DI related setup and hold times of SPI master and SPI slave. If for example the SPI master requires a longer setup time than *T*/2-*t*(sov), the SPI clock speed in normal SPI mode must be reduced. Alternatively, BGT60UTR11AIP can be switched to SPI high-speed mode by setting SFCTL:MISO_HS_RD = 1_B.

The timing diagram for high speed SPI mode is presented in Figure 24. In this mode the SPI master is still supposed to capture the level of DO with the rising edge of CLK. The SPI slave keeps the level of DO stable for *t*(soh) after the rising edge of CLK, and then sets the level of DO according to the next bit which is send out.

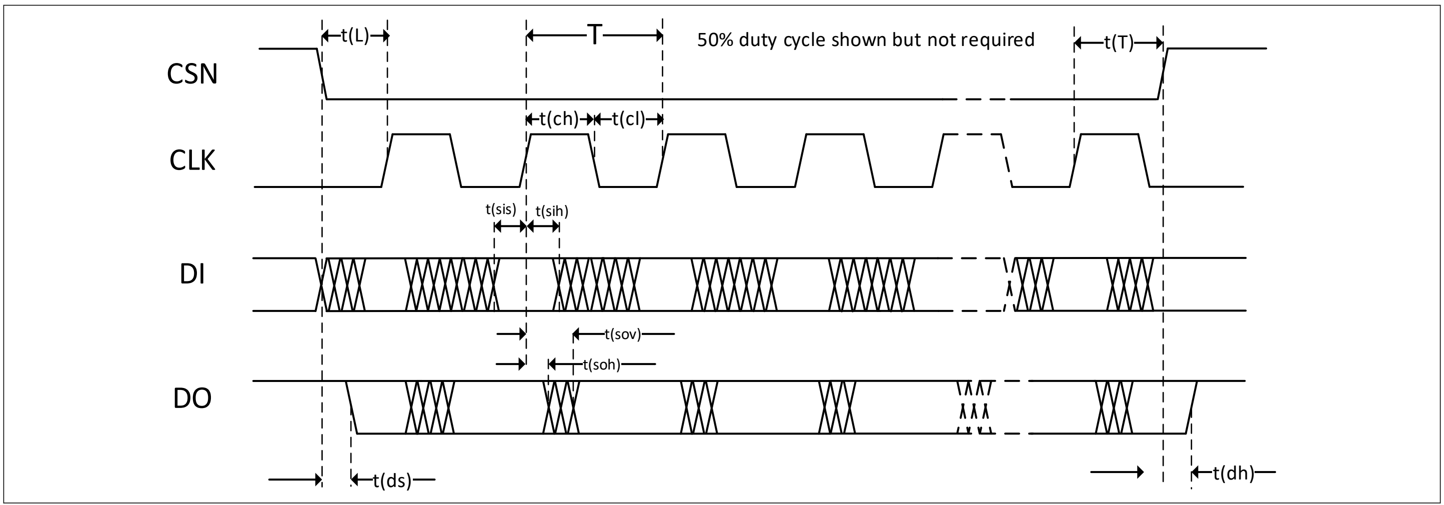

Figure 24 **SPI interface timing diagram for SFCTL:MISO_HS_RD = 1_B**

Table 26 **SPI Timing Requirements**

VDD_{IO} = 1.08 V to 1.32 V, T_b = -20 °C to +70 °C.

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
SPI clock period: 50 MHz, with 1% clock jitter	*T*	20	-	-	ns	-
Clock high	*t*(ch)	9.0	-	-	ns	-
Clock low	*t*(cl)	9.0	-	-	ns	-
Slave input setup	*t*(sis)	5.0	-	-	ns	-
Slave input hold	*t*(sih)	5.0	-	-	ns	-
Slave output valid	*t*(sov)	-	-	15.0	ns	see note
Slave output hold	*t*(soh)	1.0	-	-	ns	-
Lead time before the first working clock edge occurs	*t*(L)	9.0	-	-	ns	-
Tailing time after the last working clock edge	*t*(T)	1	-	-	ns	-
Data setup time after the DO goes in low impedance state	*t*(ds)	-	-	5	ns	Ensured by design
Data hold time before DO goes in hi impedance state	*t*(dh)	-	-	5	ns	Ensured by design

***Note**:*

- *If SFCTL:MISO_HS_RD is not set properly then data read on* MISO *may not be correct*
- *The timing is ensured for worst case condition: VDD_{IO} = 1.08 V, T_b = +70 °C, output load of C_{load} = 50 pF*
- *Better conditions results in a much shorter t(sov) time*

5.3.2 Logic levels

The digital inputs and outputs are fully *complementary metal-oxide semiconductor (CMOS)* compatible. All IO input/output timings are based on 50% voltage reference levels (see following figure). I/O interfaces are shown in Figure 28 and Figure 29, which include internal pull-ups.

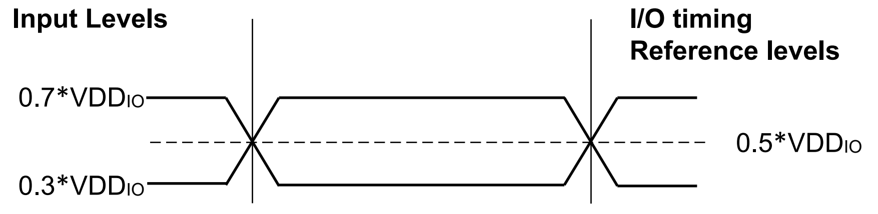

Figure 25 AC timing input/output reference levels

The input logic hysteresis prevents input buffers from oscillation. The minimum hysteresis range V_{HYST} is in between the lower (0.3 * VDD_{IO}) and upper logic level (0.7 * VDD_{IO}) boundaries (see Figure 26). Above 0.7 * VDD_{IO} the input signal is a logical '1' while below 0.3 * VDD_{IO} it is a logical '0' regardless of hysteresis. Due to temperature drifts and device variation the hysteresis range V_{HYST} can be up to 0.7 * VDD_{IO} or down to 0.3 * VDD_{IO} but typically around 0.5 * VDD_{IO}. Parameters are reported in Table 28.

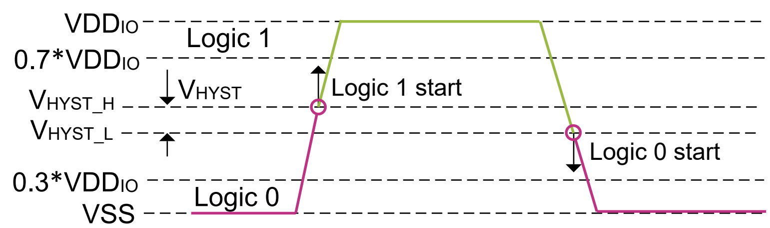

Figure 26 Logic input levels and hysteresis

The digital output pads have a programmable output pad strength that gives a specific slew-rate for rising signals, dV_{TR}, and falling signals, dV_{TF} (see following figure). Minimum slew rates were simulated considering a total capacitive load of 15 pF. Results reported in Table 29.

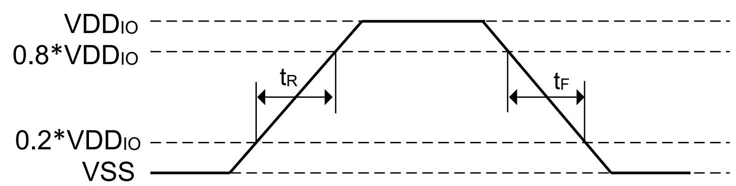

Figure 27 Rise/fall time, slew rate specified between 0.2 * VDD_{IO} and 0.8 * VDD_{IO}

Table 27 Logical Levels for Input Pins

VDD_{IO} = 1.08 to 1.32 V, T_b = -20 to +70 °C, ambient temperature not below -40 °C; all voltages with respect to VSS_{IO} digital ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
LOW level	$V_{IN(L)}$	0	-	0.3 * VDD_{IO}	V	-

(table continues...)

Table 27 (continued) Logical Levels for Input Pins

VDD_{IO} = 1.08 to 1.32 V, T_b = -20 to +70 °C, ambient temperature not below -40 °C; all voltages with respect to VSS_{IO} digital ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
HIGH level	$V_{IN(H)}$	0.7 * VDD_{IO}	-	VDD_{IO}	V	-
Input current (0 V < V_{IN} < VDD_{IO})	I_{IN}	-150	-	150	µA	-
Input capacitance CLK/CSN/DI/RST	C_{IN}	1.3	-	-	pF	-
Minimum hysteresis voltage range between 0.3 * VDD_{IO} and 0.7 * VDD_{IO}	V_{HYST}	250	-	-	mV	V_{HYST_H} - V_{HYST_L}
Upper hysteresis signal level	V_{HYST_H}	-	0.5 * VDD_{IO} + V_{HYST} / 2	0.7 * VDD_{IO}	V	-
Lower hysteresis signal level	V_{HYST_L}	0.3 * VDD_{IO}	0.5 * VDD_{IO} - V_{HYST} / 2	-	V	-

Table 28 Logic Levels for Output Pins

VDD_{IO} = 1.08 to 1.32 V, T_b = -20 to +70 °C, ambient temperature not below -40 °C; all voltages with respect to VSS_{IO} digital ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
LOW level	$V_{OUT(L)}$	0	-	0.2 * VDD_{IO}	V	-
HIGH level	$V_{OUT(H)}$	0.8 * VDD_{IO}	-	VDD_{IO}	V	-
Output current (LOW)	$I_{OUT(L)}$	-2	-	-	mA	
Output current (HIGH)	$I_{OUT(H)}$	-	-	2	mA	
Allowed load capacitance to provide maximum signal frequency on DO	C_{LOAD}	-	-	15	pF	-
Output pad slew rate for rising wave form	dV_{TR}	0.15	-	-	V/ns	0.2 * VDD_{IO} to 0.8 * VDD_{IO} with 50 pF load
Output pad slew rate for falling wave form	dV_{TF}	0.13	-	-	V/ns	0.2 * VDD_{IO} to 0.8 * VDD_{IO} with 50 pF load

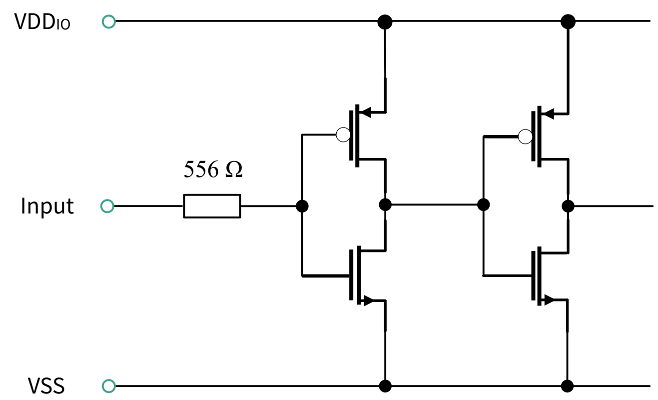

Figure 28 **Interface for input pins**

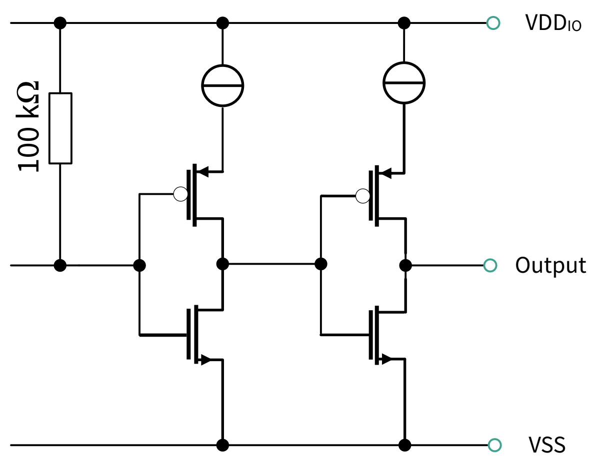

Figure 29 **Interface for output pins**

5.3.3 Overshoot and undershoot waveform definition

During operation, the applied signals and supply levels should not exceed absolute maximum *direct current (DC)* levels specified in datasheet. Digital signals can have positive or negative overshoots due to inductive and/or capacitive loads. Table 29 reports the allowed overshoot signal levels for all logic signals.

Table 29 **Overshoot and undershoot signal levels**

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Maximum absolute overshoot voltage level	V_{os}	-	-	VDD_{IO} + 0.5 V	V	see note
Maximum absolute undershoot voltage level	V_{us}	-	-	VSS_{IO} – 0.5 V	V	see note

***Note**:* *Maximum pad current not exceeding ±2 mA (see also Chapter 5.3.2). No slew rate limitation existing on digital signals for overshoots/undershoots.*

5.3.4 IBIS model

A BGT60UTR11AIP *Input/output Buffer Information Specification (IBIS)* model is available under *non-disclosure agreement (NDA)* upon request. It is based on timing simulations. In order to better reflect the real timing behavior, different pad models for input/output signals are used and summarized in the following table. The driver strength and the pull-up can be modified via registers.

Table 30 IBIS Pad types and models (see IBIS model)

Pin	Ibis PAD Model
CSN	IN: Selection_0
CLK	IN: Selection_0
DI	IN: Selection_0
DO	OUT: Selection_1
DIO2	Not available on BGT60UTR11AIP
RST	IN: Selection_0
IRQ	OUT: Selection_1

5.3.5 SPI functionality

Each word transferred over the *SPI* bus has a length of 1 command byte + 3 data Bytes. The communication is done bitwise. First the address is transferred with *most significant bit (MSB)* first. The address is followed by the R/W-bit and then followed by the data which is sent MSB first, too. At the same time, while command byte is received, a freely from system level configurative global status register (8 bits, GSR0) is serial shifted out on DO (MSB first). On the following 24 clock cycles the selected register content is shifted out on DO, MSB first.

Depending on sent R/W-bit there are two different operation modes available, the write mode and the read mode. Every write mode is a read mode too.

Write mode

After the start condition the desired address is sent. The address is 7 bits long followed by a bit that is a data direction bit (read/write). A one indicates a write operation (see following figure).

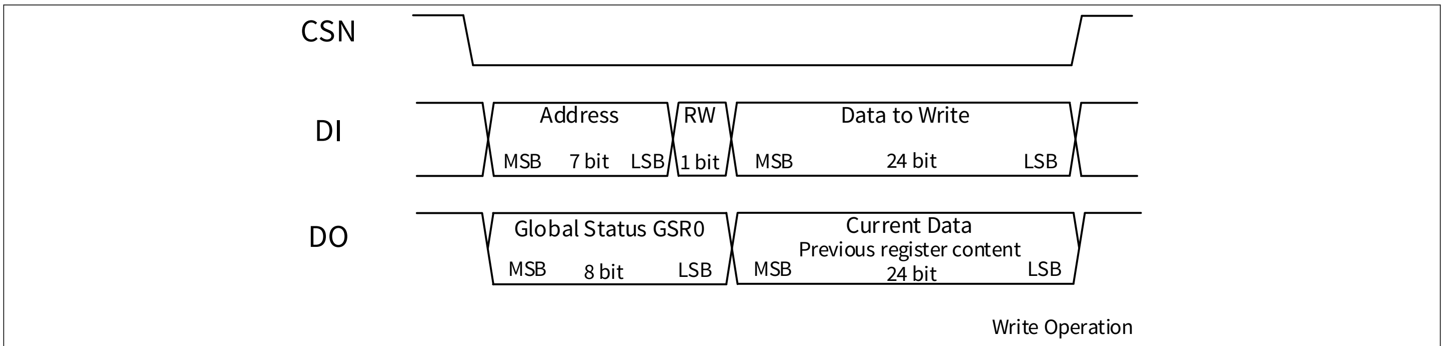

Figure 30 SPI timing write mode

Read mode

After the start condition, the desired address is sent like in the write operation. A zero of the R/W-bit indicates a read access. The data on DI after the command byte may contain any value. The DO behavior is the same as in write mode.

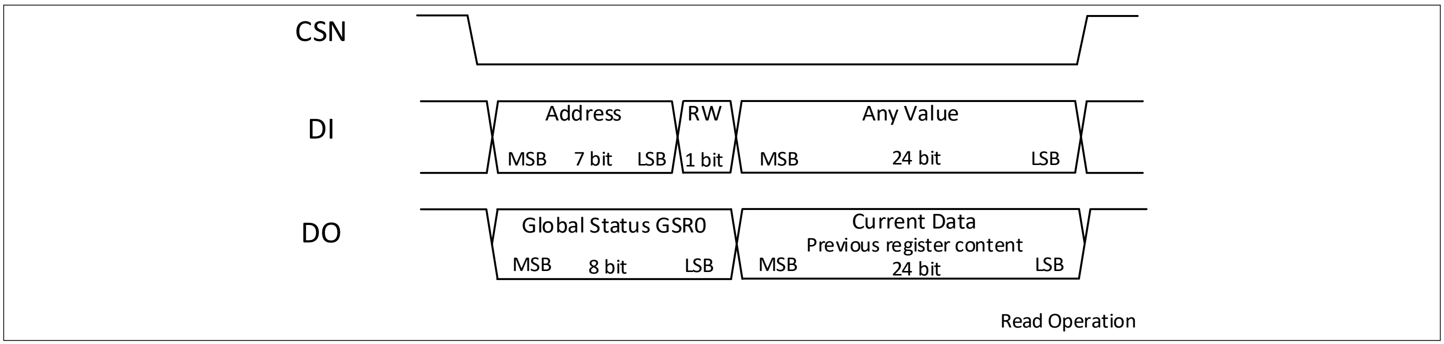

Figure 31 **SPI timing read mode**

5.3.6 SPI burst mode

The burst mode can be used to read or write out several registers or some data from the *SPI* instead of reading just single registers or data. The burst mode command is sent by the host. The burst mode command consists of several bit fields and is shown in the following table.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR							**RW**	**SADDR**							**RWB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NBURSTS							**RSVD**								

Field	Bits	Description
RSVD	8:0	**Reserved**
NBURSTS	15:9	Number of processed data blocks: 0_H… “unbounded” burst accesses 1_H..$7E_H$ … number of words to transfer
RWB	16	Burst read or write: 0_B … Perform a read burst 1_B… Perform a write burst, (writes to *FIFO* not supported)
SADDR	23:17	Starting address where the burst starts processing: < 64_H Register access == 64_H FIFO access > 64_H Reserved Address is incremented automatically inside a burst.
RW	24	Read/Write register access: 1_B … write to address $7F_H$
ADDR	31:25	To enter the burst mode the following address is used: $7F_H$ … request the burst read/write.

***Note**:* *A single data block is 24 bits width for both, the sampling memory and the registers.*

Burst mode operation

After the start condition the 32 bits burst mode command is sent from the SPI master on DI. At the same time, the status register GSR0 (four 1_B bits + four status bits) followed by 24 padding bits set to 0_B is shifted out on DO. After the command sequence is done, the register/FIFO data is shifted out to the SPI master on DO. In burst write mode, the register data to be written is shifted in from the SPI master (application processor e.g.).

Burst mode read sequence

In the read sequence, the SPI master reads from the device.

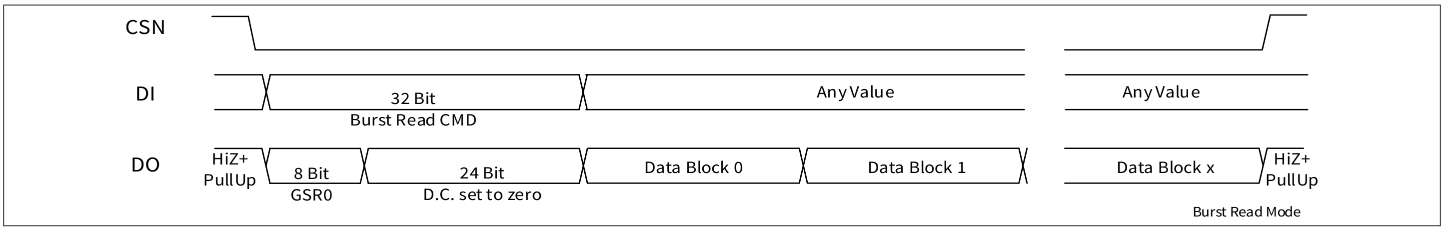

Figure 32 Burst mode read sequence

Burst mode write sequence

In the burst write mode, the SPI master writes to the device.

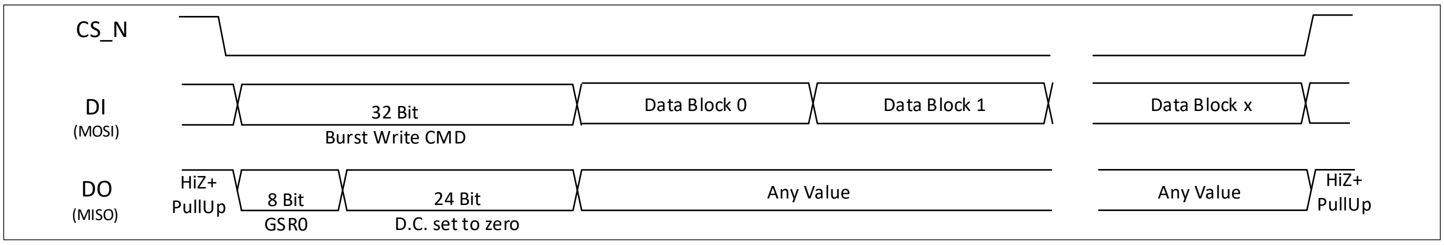

Figure 33 Burst mode write sequence

Sampling data arrangements in data blocks

The data from the FIFO are streamed out during the burst read request, starting from the FIFO address zero. The 1st *ADC* is the ADC channel with the lowest channel number. As far as the sampling memory is organized in 24 bits and up to 1 ADC channels are selectable through the ADC channel selection bits (CSx:MADC_BBCH_SEL, see Channel set up x register 1) the data blocks are arranged as follows.
In case a single ADC is selected the data blocks are shown in the following figure.

Single ADC channel data stream

Data Block 0		Data Block 1		Data Block 2		…	Data Block x	
1st ADC 1st Result	1st ADC 2nd Result	1st ADC 3rd Result	1st ADC 4th Result	1st ADC 5th Result	1st ADC 6th Result		1st ADC (N-1)th Result	1st ADC Nth Result

Figure 34 Single ADC channel selected

Example: Burst mode read sampling memory sequence

The following burst mode command is sent from the host to initialize the burst mode to read from the FIFO an undefined number of sampling data:

- BMCMD_RS = (ADDR = $7F_H$, RW = 1, SADDR = 64_H, RWB = 0, NBURSTS = 0_H)

Remark: For each burst read request to the sampling memory, the sampling-memory address pointer is reset to the initial value. So that memory can be read out from the beginning until the application processor stops burst reading.

Example: Burst mode read registers sequence

The following burst mode command is sent from the host to initialize the burst mode to read out 10 registers starting from register address 3:

- BMCMD_RR10 = (ADDR = $7F_H$, RW = 1, SADDR = 3_H, RWB = 0, NBURSTS = A_H)

5.3.7 SPI error detection

SPI_BURST_ERROR and CLK_NUM_ERROR (see FIFO status register) will be cleared after these resets:

- *software (SW)* reset
- *hardware (HW)* reset

SPI_BURST_ERROR, CLK_NUMBER_ERROR and FOU_ERROR are reported in the global status bits (GSR0) of the **next** *SPI* transaction and latched as sticky bits in the FSTAT register.

In order to understand if the captured sample data are corrupted, the host can evaluate the bit field CLK_NUM_ERR and SPI BURST_ERR as reported in the following table.

Table 31 SPI BURST_ERR and CLK_NUM_ERR Definitions

Length Range	Transaction	SPI BURST_ERR	CLK_NUM_ERR	Behavior on read/write
0	Null command	0_B	0_B	Ignored
1-31	Short length error in single	0_B	1_B	Command ignored
>32	Long length error in single	0_B	1_B	Extra bits ignored
1-31	Short length error in SPI burst header	0_B	1_B	Command ignored
<24xN	Missing whole data word in bounded burst	1_B	0_B	Available data words used
>24xN	Extra whole data word in bounded burst	1_B	0	Extra data word(s) ignored
%24>0	Misaligned bit-count for bounded burst	1_B	1_B	Extra bits ignored
%24>0	Misaligned bit-count for infinite burst	0_B	1_B	Partial data word may be discarded

***Note**:*

- *Ignored write transaction means that no register (or memory) content is affected by the partial write command, or incomplete data word.*
- *Ignored read transaction means that the returned data is invalid, and for the FIFO no words are removed by the partial read command, or incomplete data word.*
- *Discarded read transaction means that the data is already read from the* FIFO *but only partially transferred; subsequent read pops next word from* FIFO.
- *Data from the* FIFO *may be discarded after a length error in the infinite burst (NBURST=0) occurs. The* FIFO *read has to happen, since at that stage the data is required to be shifted out, but if not all bits are shifted out the* FIFO *is already read and the partial data word may be discarded.*

5.3.8 SPI broadcast mode

BGT60UTR11AIP comes with a special *SPI* feature called broadcast mode. This mode gives the user the capability to program multiple radar sensors which shares the same SPI bus.

To avoid driver conflicts of contradictory logic levels on the shared *MISO* line the SPI broadcast mode deactivates the output driver of the DO pin. This change becomes active with the rising edge of CS after MAIN:SPI_BC_MODE is programmed to 1_B. The deactivation of this mode is done in a similar way by programming MAIN:SPI_BC_MODE to 0_B which activates the output driver of the DO pin again with the rising edge of CS.

There are two main use cases to benefit from this SPI broadcast mode:

- To speed up initial radar sensors configuration by programming all devices at the same time
- To synchronize multiple radar sensors by triggering a frame at the same time (single SPI write command with MAIN:FRAME_START = 1_B

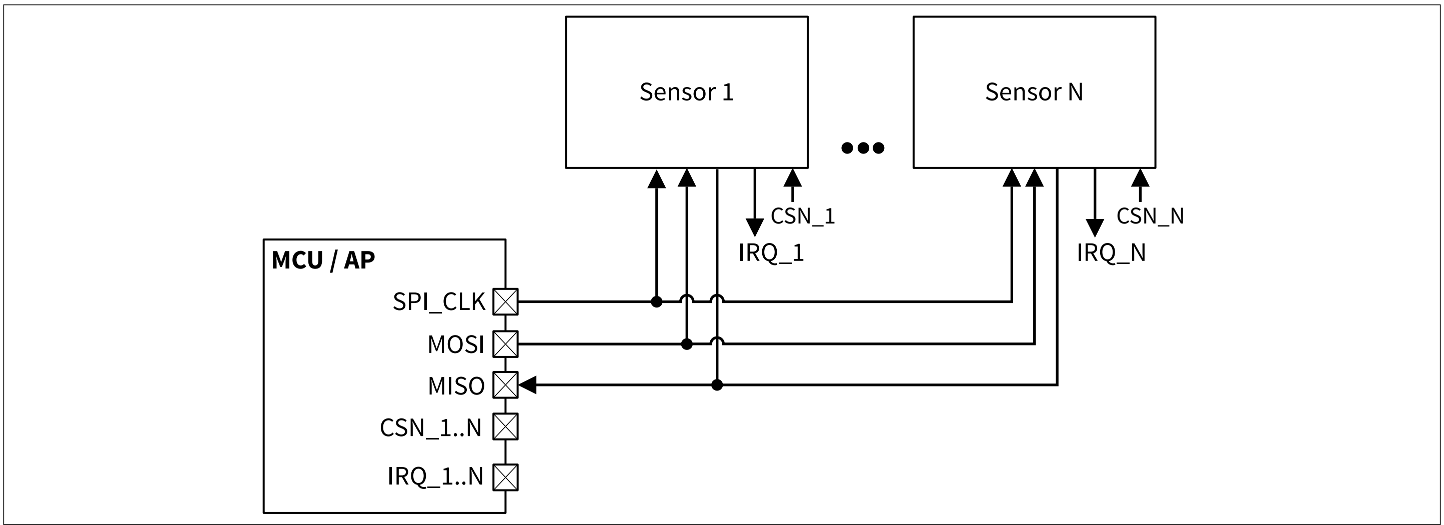

Figure 35 SPI broadcast block diagram

A SPI broadcast system with multiple sensors (e.g. sensor 1, sensor 2 …) shares the same SPI bus including SPI clock (SPI_CLK), data input and output (*MOSI*, MISO) and maybe also the same oscillator clock (OSC_CLK). However, each sensor requires an own chip select (CSN) pin on the SPI master (e.g. *MCU*, *AP*) side to enable individual control over each sensor. Also a dedicated interrupt input pin is needed on SPI master side for each sensor interrupt output (IRQ).

5.4 Hardware reset sequence

In order to perform a proper device reset, a special reset sequence is required. For example, after a device power-up.

While CSN is = '1_B' RST must perform a 1_B 0_B 1_B transition

The behavior is presented in the following figure with:

- T_CS_BRES = 100 ns
- T_RES = 100 ns
- T_CS_ARES = 100 ns

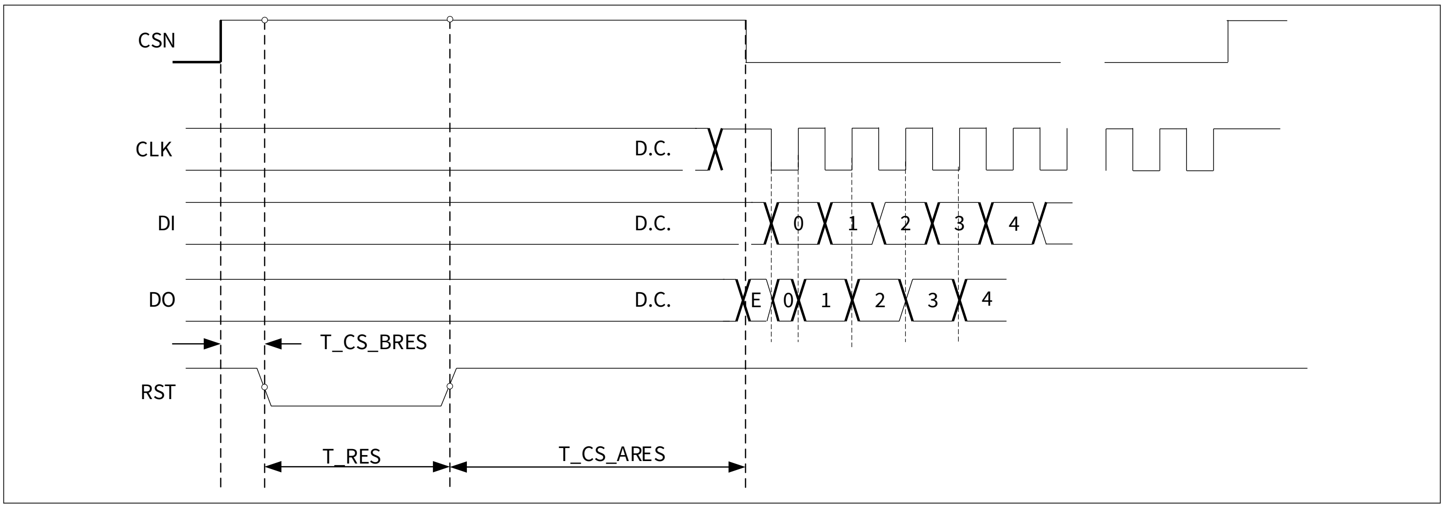

Figure 36 **Hardware reset sequence**

5.5 Software triggered resets

Besides the hard reset, three reset sequences are supported and can be triggered in the MAIN register (see also Main register). They are defined according to the following hierarchy:

- *SW* reset -> *FIFO* reset -> *FSM* reset

Software reset

- Resets all registers to default state
- Resets all internal counters (shape, frame e.g.)
- Perform FIFO reset
- Performs FSM reset
- A delay of 100 ns after the SW reset is needed before the next *SPI* command is sent

FIFO reset

- Reset the read and write pointers of the FIFO
- Array content will not be reset, but cannot be read out
- FIFO empty is signaled, filling status = 0_D
- Resets register FSTAT FIFO status register
- Performs an implicit FSM reset

FSM reset

- Resets FSM to DS power mode
- Resets FSM internal counters for channel/shape set and timers
- Resets Status register 0 and Status register 1 register
- Reset *PLL* ramp start signal
- Reset PA_ON
- Terminates frame (shape and frame counters incremented although maybe not complete)

6 PLL domain functional specification

The *PLL* is designed to generate high performance frequency chirps in the range of 57.4 GHz to 63.0 GHz. The modulation is performed inside the PLL bandwidth (in-band-modulation) with an analog charge pump based fractional-N RF-PLL architecture. It furthermore features a shape generator with high flexibility to allow different ramp shapes and duration times. The loop requires a low noise reference clock with a nominal frequency of SYS_CLK.

6.1 PLL interfaces and clock distribution

Figure 37 shows the interfaces to the *PLL* and the distribution of the internal system clock.

Supported are two different external oscillator input clock frequency ranges f_{OSC_CLK}#1 and f_{OSC_CLK}#2, which requires different settings of the PLL and the correct configuration of the clock input stages DC_IN (see Clock input register). Each clock-input stage consists of multiplexers for path selection and a selectable frequency doubler. In addition to this, the clock input-stage for the system includes different correction and adjustment options used for the frequency doubling DC_OUT (see Clock input register).

In case of f_{OSC_CLK} #1 the register bits CLK_IN:CLK_SEL should be set to 0_D, for f_{OSC_CLK} #2 the register bits CLK_SEL should be set to 1_D in order to use only the clock frequency doubler (see Clock input register).

The frequency doubler correction and adjustment options are the following:

- CLK_IN:CLK_SEL = 1_D: enables both frequency doublers without an input duty cycle adjustment
- CLK_IN:CLK_SEL = 2_D: enables frequency doubling with an input duty cycle adjustment via the bits CLK_IN:DC_IN_ADJ. This adjustment is applied to the input clock. The corrected clock is then the input to both duty cycle dependent frequency doublers (PLL and system clock)
- CLK_IN:CLK_SEL = 3_D enables the frequency doubling but only uses the input duty cycle correction for the frequency doubler that generates the system clock

For the case the frequency doubler is used (CLK_IN:CLK_SEL ≥ 1_D) the duty cycle of the generated doubled clock can be modified with the bits CLK_IN:DC_OUT_ADJ to a value close to 50%. This adjustment only applies to the system clock as the PLL only requires a minimum duty cycle for the reference clock, which is ensured by design.

6.1.1 Reference clock distribution

The external reference clock signal is provided via a short, low jitter path directly to the clock input port of the *PLL* analog part (PLL analog). Inside the PLL analog part the clock path is split and goes to two different clock input-stages. One stage is dedicated to the PLL and is under the internally regulated low noise supply of the PLL. The second input stage is used to provide the system clock through the *simplified timing shell (STS)* to the output of the PLL macro (osc_clk2dig). The STS is a defined timing interface between the PLL analog and the digital part. Since osc_clk2dig serves as the clock for the main *FSM* it must have an independent path to ensure availability even when the PLL is put into power down. Therefore, the usage of supplies generated inside the PLL is avoided for this path. The main FSM clock can be gated via a dedicated register bit called PACR1:OSCCLKEN (see PLL analog control register 1) which gates the clock path already at its beginning.

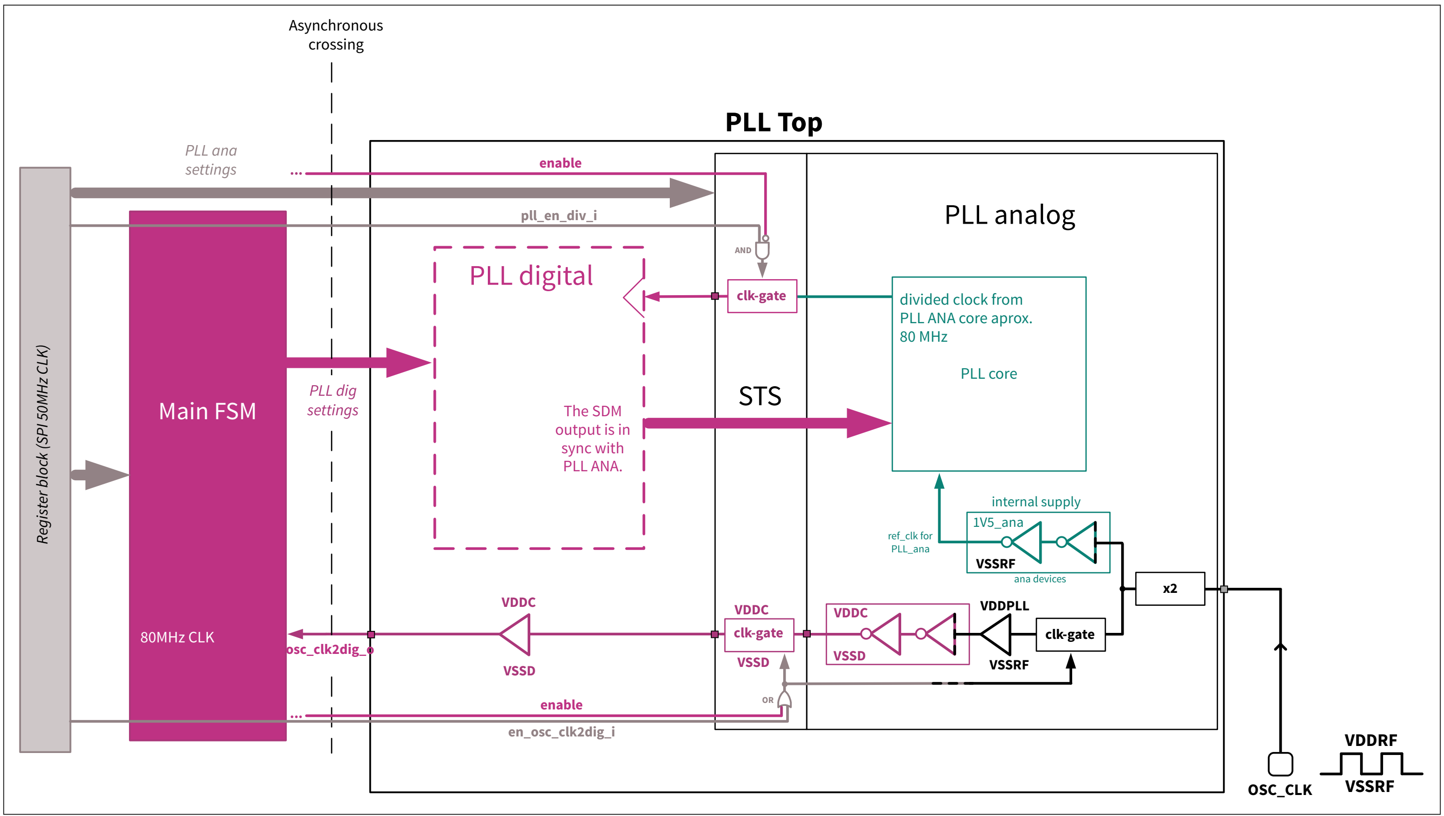

Figure 37 **PLL and SYS_CLK interface to the main FSM**

6.1.2 Interfaces to the PLL

Most static settings and control signals dedicated to the analog part of the *PLL* are treated as asynchronous signals and are passed from the register bank to the *STS* of the PLL. This applies to digital signals that are not timing critical. Ramp generation parameters provided from the main *FSM* to the digital part of the PLL are registered inside the PLL digital. The start signal of the ramp also acts as a synchronization signal of the ramp parameters. This is required since the PLL digital runs on the divided clock of the PLL which ensures a known and synchronous timing relation between the sigma-delta bit stream and the analog part of the PLL that realizes the ramping behavior. The divided clock is only available if the PLL macro and the *voltage controlled oscillator (VCO)* are activated. Other control signals from PLL digital to the analog part are kept asynchronous. In order to close the PLL loop the analog part of the PLL core has interfaces to the *RF* macro where the VCO and a part of the divider chain are located.

6.2 PLL parameters and specification

The following table summarizes the target parameters of the *PLL* based frequency generator.

Table 32 **PLL specifications**

VDD_{PLL} = 1.71 to 1.89 V, VDD_{LF} = 2.5 to 3.63 V, T_b = -20 °C to +70 °C.

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
PLL Chirp Parameters						
Output Frequency Range	f_{RF}	57.4	-	63.0	GHz	Range depends on the VDD_{LF} value

(table continues...)

Table 32 (continued) PLL specifications

VDD_{PLL} = 1.71 to 1.89 V, VDD_{LF} = 2.5 to 3.63 V, T_b = -20 °C to +70 °C.

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Continuous FM-Chirp Bandwidth	*BW*	0	-	5.6	GHz	PLL tuning range
VDD_{LF} Range	VDD_{LF}	2.5	-	3.63	V	Complete specified *BW* requires at least VDD_{LF} = 3.3 V
Chirp slope	Slope	-	-	400	MHz/µs	-
Frequency Ramp Linearity Error	Error	-	-	1	%	For 2 GHz *BW* minimum See Figure 38
Frequency Ramp Settling Time (fast chirp feature active)	$t_{PLL,settle}$	-	5	-	µs	See Figure 39
PLL Phase Noise Single Sideband	PN_{PLL}, 100 kHz	-	-80	-75	dBc/Hz	at 100 kHz offset

6.2.1 Frequency ramp linearity definition:

Frequency ramp linearity error is defined to be < 1% of the *frequency-modulated (FM)* chirp bandwidth. The linearity error is calculated as the deviation from an “ideal” frequency ramp. The specification needs to be fulfilled after the frequency ramp settling time (see also Chapter 3.3). The assumed worst-case FM chirp bandwidth for linearity evaluations is 2 GHz.

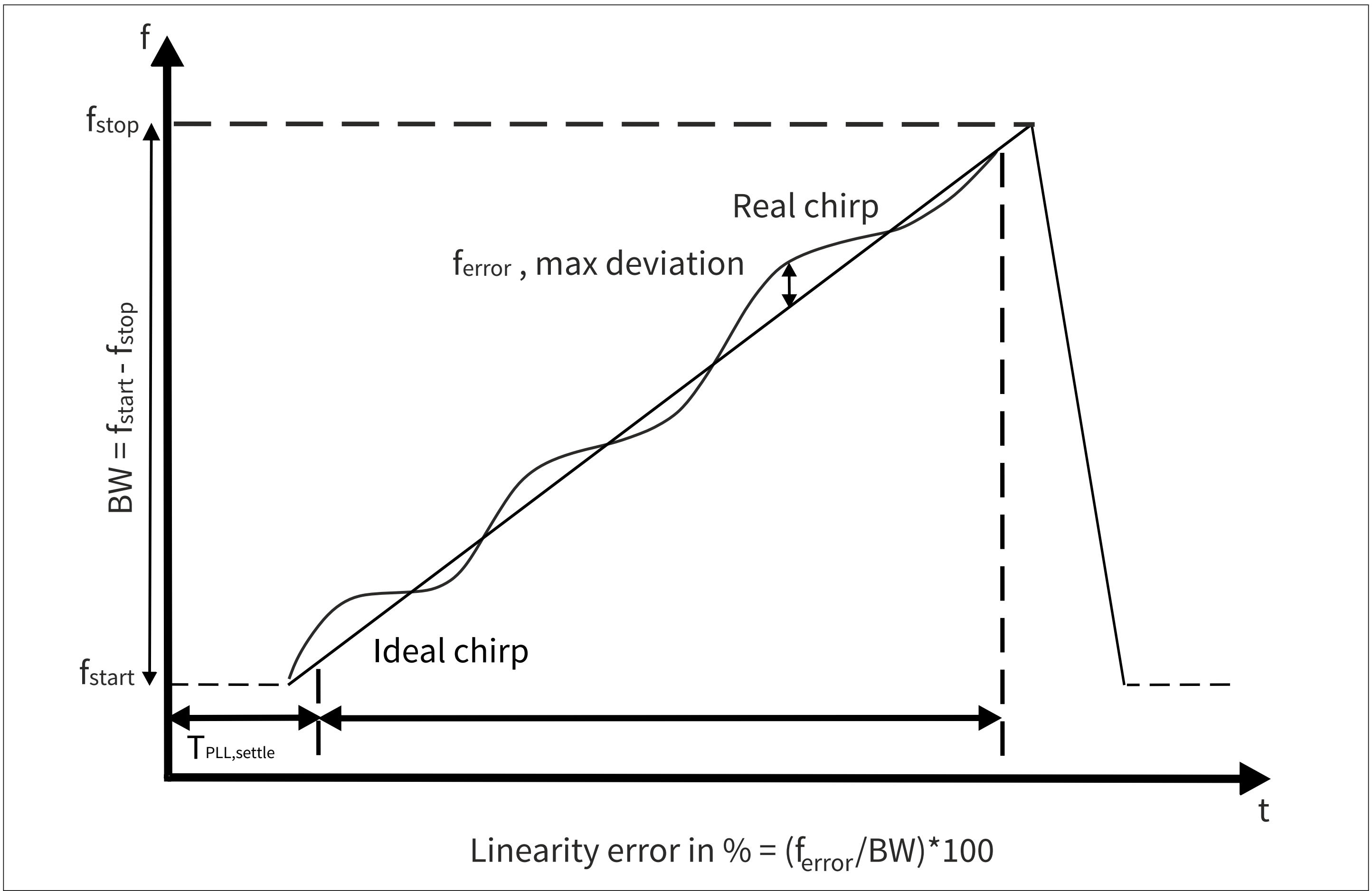

Figure 38 **Frequency linearity definition**

The max frequency error expected, assuming 2 GHz minimum *BW* and a max deviation of 1%, will be 20 MHz.

6.2.2 Frequency ramp settling time

It is the time required by the *PLL* to damp undershoot and overshoot in case of saw-tooth shapes. A qualitative view is shown in the following figure. See Chapter 3.3 for a more detailed definition of the timings.

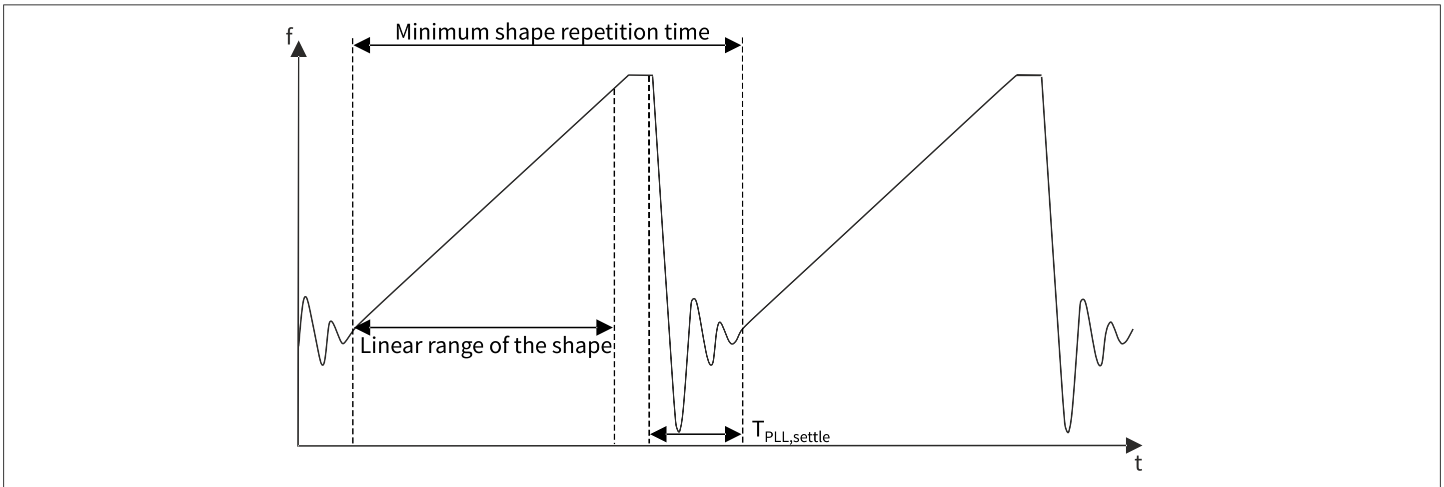

Figure 39 **Chirp settling time**

7 Analog-RF domain functional specification

In the analog functional specification all analog components like *RF* frontend (RF FE), baseband amplifiers, and filters are described in more details.

The register definitions for the components are in Channel set up x register 0.

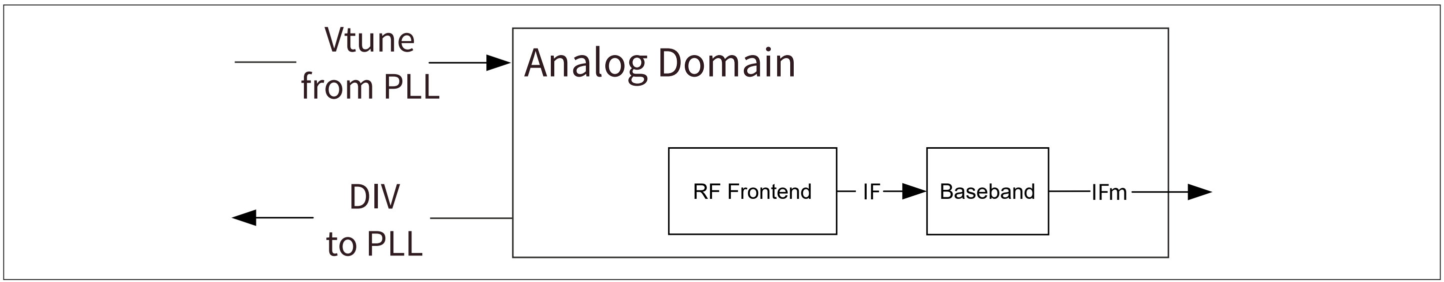

Figure 40 Analog domain simplified block diagram

7.1 RF frontend (RF FE)

In the *RF* frontend, all features to enable the radar functionality are implemented.

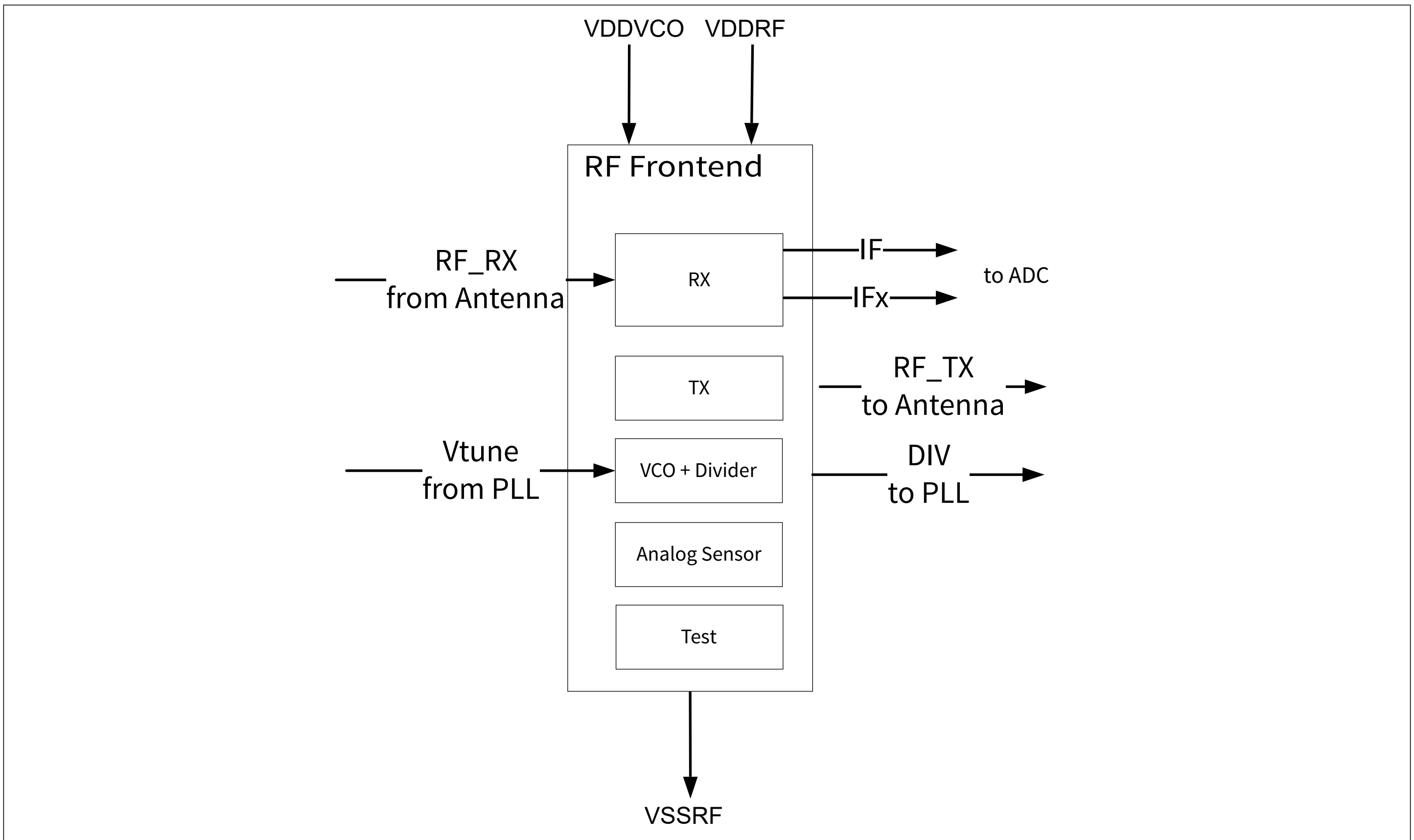

Figure 41 Simplified block diagram of transceiver frontend

7.1.1 On-chip analog sensor output

The analog sensor outputs are connected to the SADC. See for the SADC input configuration. See Channel set up x register 0 for enable pins definition.

7.1.2 RF FE specifications

In the table below the target specifications for the *RF* frontend measured at die PAD interface.

Table 33 RF FE specifications

Min and max values cover the specified frequency range, f_{RF} = 57.4 GHz to 63.0 GHz. Temperature range, T_b = -20 °C to +70 °C, and voltage supply range, VDD_{RF} = 1.71 V to 1.89 V (unless otherwise specified).

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Frequency Range	f_{RF}	57.4	-	63.0	GHz	-
Transmitter						
Transmit Output Power[1)]	P_{TX}	-	5.0	-	dBm	Conducted power
Output Power Variation over Temperature	P_{TX_Temp}	-2.0	-	2.0	dB	For TX DAC set to 31_D
Transmitter Power Control Dynamic Range	P_{TXD}	-	15	-	dB	-
DAC Resolution Transmitter Power Control	P_{TXC}	-	5	-	Bits	-
Receiver (for all RX channels)						
Receiver Conversion Gain[2)]	CG_{RX}	12	14	16	dB	-
Conversion Gain Variation Over Temperature	CG_{RX_Temp}	-3	-	3	dB	Including the complete baseband chain
Receiver Single Sideband Noise Figure	$NFssb_{RX}$	-	12	14	dB	at 100 kHz offset
Receiver 1-dB Compression Point	$P\text{-}1dB_{RX}$	-10	-5	-	dBm	-
LO feedthrough at the RX port	$LOfeed_{RX}$	-	-30	-	dBm	-
TX-to-RX Isolation	Iso_{TXRX}	-	50	-	dB	-
Sensors						
Temperature Sensor Range[3)]	T_b	-40	-	105	°C	-
Chip Backside Temperature (*Temp*) Vs Temperature Sensor Readout (*Tsense*) Relation	*Temp* *Tsense*	$Temp = \frac{Tsense - a}{b}$			°C V	-
Temperature Sensor Offset (a)	*a*	-0.19025	-0.17530	-0.15925	V	-
Temperature Sensor Slope (b)	*b*	-	0.001530	-	V/K	-

(table continues...)

Table 33 (continued) RF FE specifications

Min and max values cover the specified frequency range, f_{RF} = 57.4 GHz to 63.0 GHz. Temperature range, T_b = -20 °C to +70 °C, and voltage supply range, VDD_{RF} = 1.71 V to 1.89 V (unless otherwise specified).

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Output Power at Chip Pad Vs TX Peak Detector Readout Relation	P_{out} *PPD_PA*[4]	$P_{out} = t_1 * \ln\left(\frac{PPD\_PA + y_0}{A_1}\right)$ y_0 = 0.02933 V A_1 = 0.19253 V t_1 = 8.912 dBm			dBm V	*PPD_PA* selected
TX Peak Detector Accuracy	PPD_PA_{acc}	-2	-	2	dB	Over f_{RF}
TX Peak Detector Dynamic Range	PPD_PA_{DR}	-10	-	10	dBm	Min. 8 bits

1) At die pad.
2) Power to voltage gain.
3) If storage temperature exceeds 125° C an additional drift of the temperature sensor readout up to ±20 K might occur.
4) Output power can be evaluated by sampling the level of the peak detector level at the output of the TX power amplifier. This signal has to be compared to a reference to de-embed thermal drift of the sensor.

***Note**: The spurs of the system clock signal could affect the sensor readout. In order to have a more stable read out for the sensors an average over 16 samples for each sensor measurement is recommended.*

7.2 Analog baseband: amplifiers and filters

The baseband amplifiers and filters adjusts the *IF* signals to fulfill the system requirements. They set the signal levels to drive full scale the *ADC* inputs without clipping.

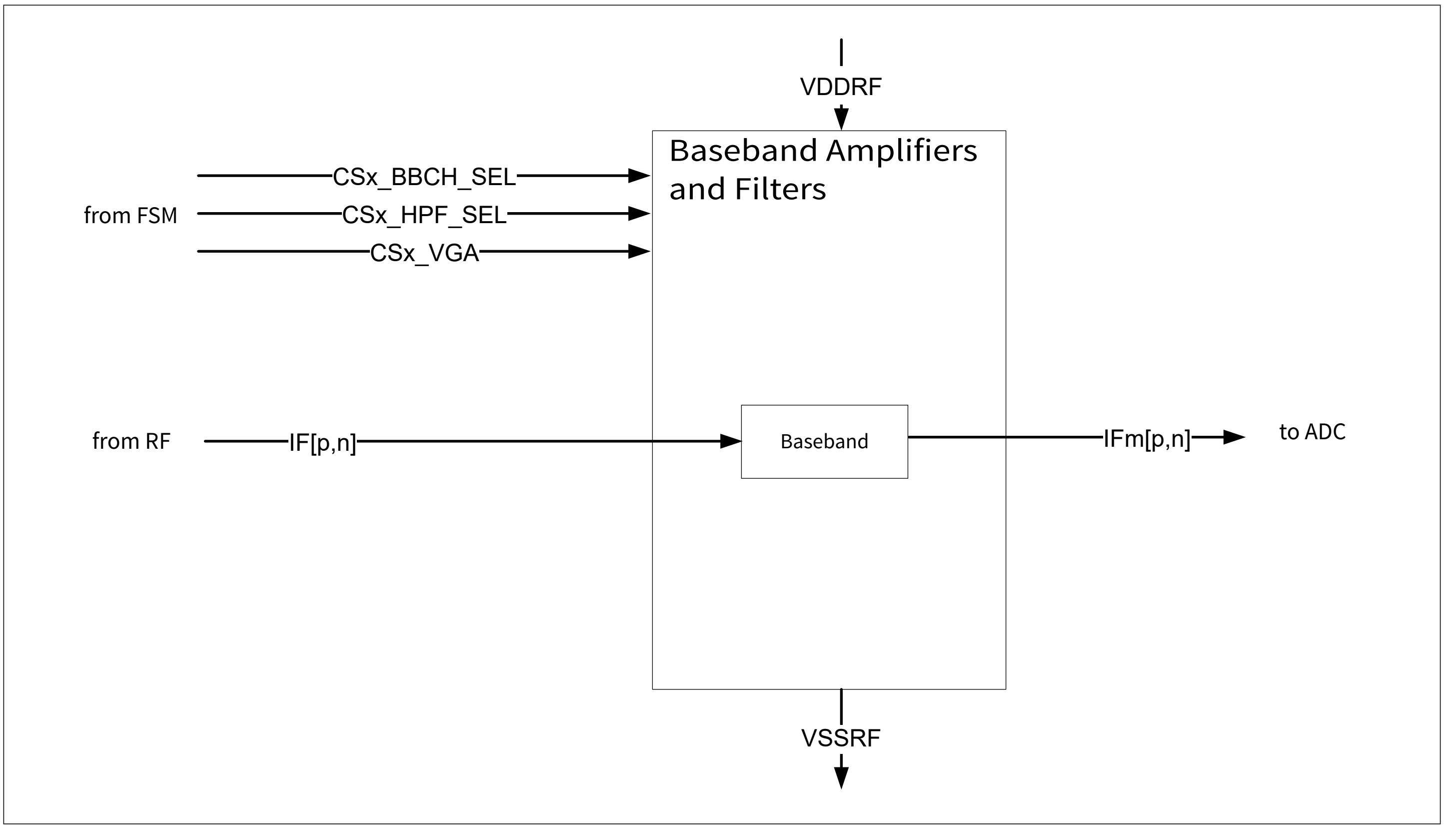

Figure 42 **Baseband amplifiers and filters block diagram**

7.2.1 Baseband characteristics

The baseband block consists of 1 channels. Each channel consists of a *HPF*, a *VGA*, and *AAF* plus a driver for the *ADC* (see Figure 44).

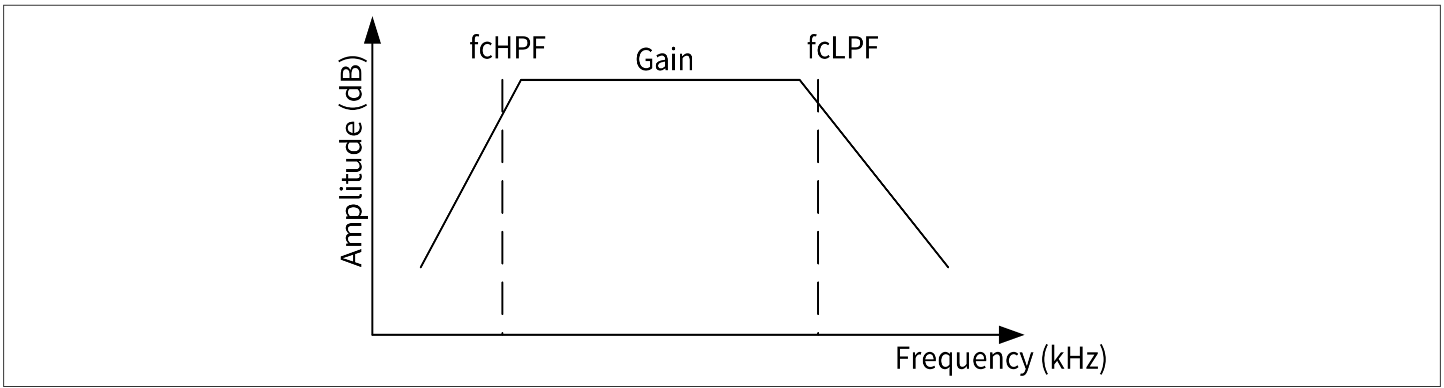

Figure 43 **Baseband characteristics**

The HPF is used in order to remove the *DC* offset at the output of the *RX* mixer and also suppress the reflected signal from close in unwanted targets (e.g., radome).

7.2.2 Baseband requirements

The *HPF* can be tuned to accommodate different fcHPF according to different modulation parameters. As presented in the following table, four different settings are possible.

Given the expected power levels the radar system will deal with, the HPF should not degrade the linearity of the system.

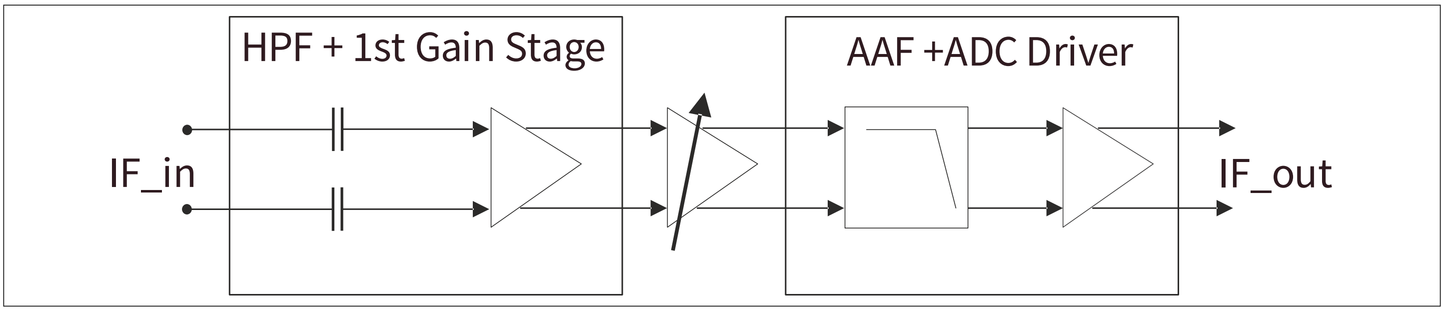

Figure 44 **Baseband simplified block diagram, one for each channel**

After the *alternating current (AC)* coupling, the *IF* signals are amplified by the first amplifier stage. The first stage shows a selectable voltage gain of 18 or 30 dB. The gain can be adjusted in the *VGA* in 6 steps of 5 dB each up to a maximum gain of 30 dB. The VGA is followed by a two-stages, four-poles *AAF*.

The AAF cutoff can be set to either 600 kHz or 1 MHz. The signal is then applied to an *ADC* driver amplifier, which has a gain of 1. The ADC driver shows a cut-off behavior above 1 MHz.

Overall, the baseband chain can be set to a maximum gain of 60 dB.

The specific parameters of the baseband chain are summarized in the following tables.

Table 34 **High pass filter selection**

VDD_{RF} = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C

Parameter	Value			Unit	Description
	Min.	Typ.	Max.		
Fc_HPF_0	-	20	-	kHz	HPF 3 dB cutoff frequency
Fc_HPF_1	-	40	-	kHz	HPF 3 dB cutoff frequency
Fc_HPF_2	-	80	-	kHz	HPF 3 dB cutoff frequency
Fc_HPF_3	-	140	-	kHz	HPF 3 dB cutoff frequency
Fc_HPF_4	-	160	-	kHz	HPF 3 dB cutoff frequency

Table 35 **Baseband gain stages**

VDD_{RF} = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C.

Parameter	Value			Unit	Description
	Min.	Typ.	Max.		
1^{st} Gain Stage	-	18/30	-	dB	Selectable, by design
VGA	-	30	-	dB	6 steps
VGA Step Size	4	5	6	dB	-

Table 36 **Anti-aliasing filter specification**

VDD_{RF} = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C.

Parameter	Value			Unit	Description
	Min.	Typ.	Max.		
fcLPF1	450	500	650	kHz	3 dB cutoff frequency
fcLPF2	-	1000	-	kHz	3 dB cutoff frequency

(table continues...)

Table 36 (continued) Anti-aliasing filter specification

VDD_{RF} = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C.

Parameter	Value			Unit	Description
	Min.	Typ.	Max.		
LPF_Order	-	4^{th}	-	-	Four poles, by design
LPF_Flatness	-	1	-	dB	In band flatness, ensured by design

8 MADC domain functional specification

The multichannel *ADC* (MADC) block consists of 1 differential *successive approximation register (SAR)* ADC. The ADC captures the differential *IF* output signals from the *ABB* and convert it into a digital representation of the same. The 1.5 V supply (VDD_C) is internally generated by a dedicated *LDO* (see Figure 5). For the ADC the parameters are set in ADC control register. Each channel of the MADC can be enable/disable together with the respective baseband channel by the bits MADC_BBCH_EN in Channel set up x register 1. To simplify the dataflow to the channel can be selected via the BBCH_SEL in Channel set up x register 1. See also APU and APD in PLL shape x register 3 and Chapter 5.2.

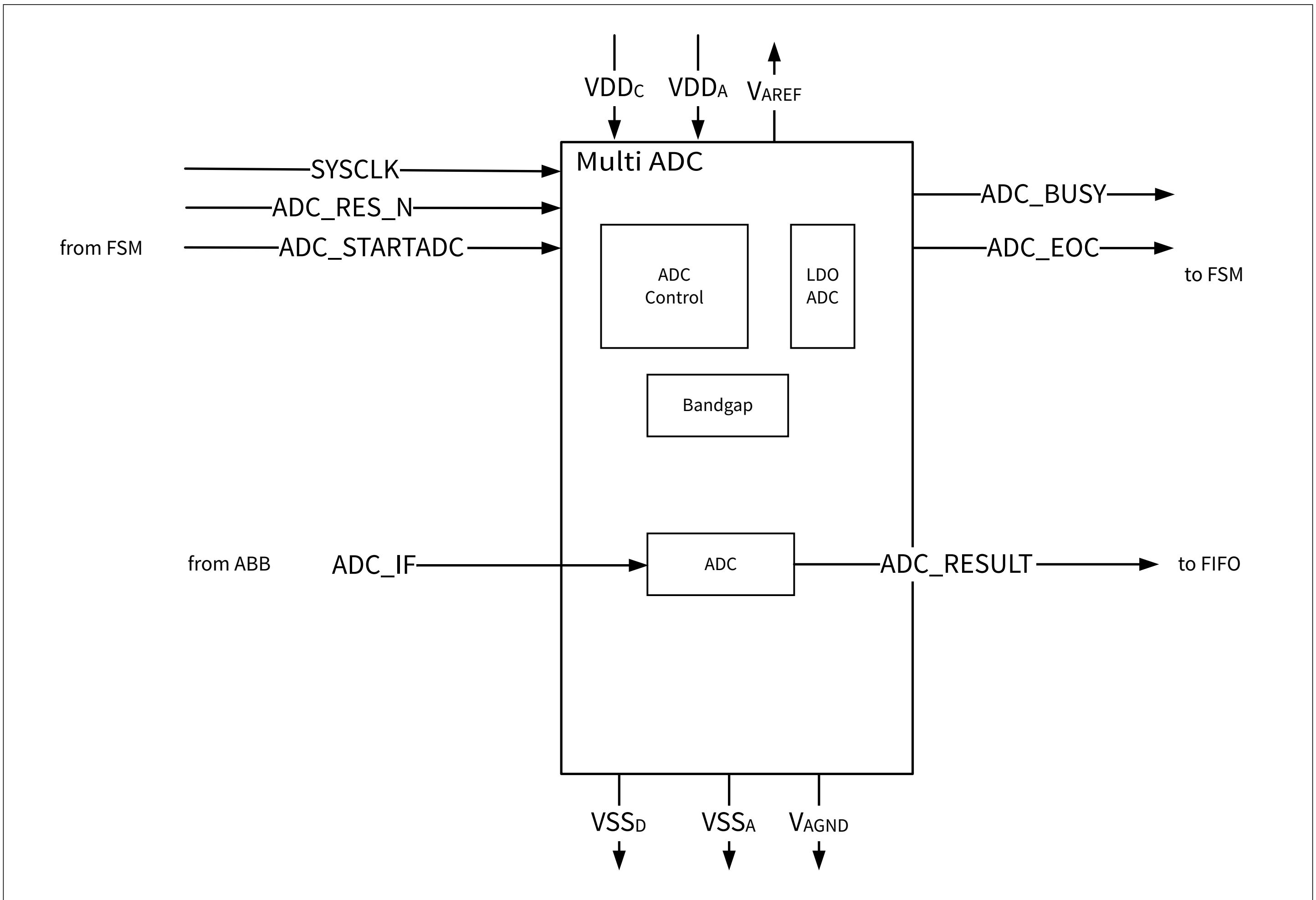

Figure 45 **MADC block diagram**

8.1 MADC supply voltage requirements

The voltage supply to the *ADC* domain is provided on pin VDD_A and the output of the internal ADC reference voltage is provided on pin V_{AREF}. In order to filter out the voltage ripples due to switching effects a low *equivalent series resistance (ESR)* bypass capacitor of C_{b2} = 470 nF should be used on the *printed circuit board (PCB)*.

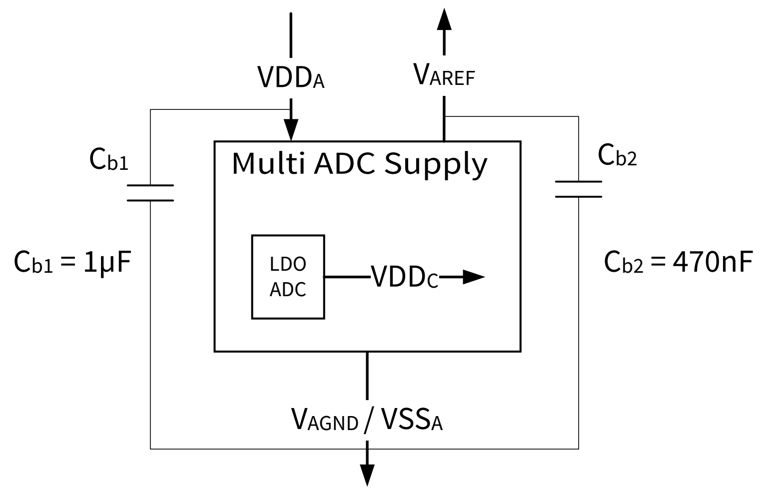

Figure 46 **MADC input pin requirements**

V_{AGND} shares the same analog ground connection pin VSS_A on PCB. The bypass capacitors should be mounted as close as possible to those pins.

Table 37 **MADC voltage reference**

VDD_A= 1.71 V to 1.89 V, T_b= -20 °C to +70 °C.

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Positive reference voltage with respect to V_{AGND}, generated internally	V_{AREF}	1.10	1.21	1.29	V	-
Negative analog reference voltage	VSS_A	-0.1	0	-	V	Refers to board design ground plane

8.2 MADC specifications

The following table specifies the *ADC* parameters. The numbers include one over-conversion. All parameters are only valid with executed start-up calibration. No parameter is targeted for production test.

***Note**:* $f_{ADC\_CLK}= f_{SYS\_CLK}$

REMARK:

If the ADC starts sampling before the bandgap is powered up (BG_EN in Channel set control x register), the results will show some gain errors. To avoid this, follow the bandgap power up timing presented in section Chapter 8.4.

Table 38 MADC specifications

VDD_A = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C.

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Resolution	Resolution	-	12	-	Bits	With default settings and tracking conversion Table 41
Analog input voltage	V_A	0.145	-	1.455	V	-
ADC Clock Frequency	f_{ADC_CLK}	75	80	85	MHz	$f_{ADC\_CLK} = f_{SYS\_CLK}$ See Chapter 2.2 78 MHz not allowed
Signal to noise ratio	*SNR*	55	64	-	dB	@ -6 dB FS
Spurious free dynamic range	*SFDR*	58	69	-	dB	@ -6 dB FS @ 600 kHz
Inter modulation product	*IM3*	-62	-69	-	dB FS	@ -12 dB FS each input tone @ 600 kHz max *f* @ 50 kHz Δ*f*
Bandwidth input buffer	*BW*	600	-	-	kHz	1st order Filter in input Buffer
Conversion time – excluding sample time	N_{conv}	-	24	-	Counts of clk	Including one tracking conversion, sampling time not included
Sampling time	T_s	4	-	-	Counts of clk	@ 76.8/80 MHz
Wake up time – bandgap and BG reference Buffer	T_{WUBGB}	300	600	1000	µs	-
Wake up time – ADC[1)]	T_{WUADC}	-	660	-	Counts of clk	without start-up calibration
Startup calibration time[2)]	T_{SUCAL}	3361	6049	16801	Counts of clk	ADC0:DSCAL= 0_B Typical conditions: ADC0:STC=1_B ADC0:MSB_CTRL= 1_B
Setup time common mode input voltage	T_{VCM}	-	-	1	µs	-
Power supply Rejection Ratio on VDD_S	*PSRR*	20	-	-	dB	-

1) Overall wake up time when calibration time is enabled = $T_{WUADC} + T_{SUCAL}$.
2) T_{SUCAL} = (1792 * $2^{ADC0:STC}$ + 896*ADC0:MSB_CTRL + 1569) * T_{SYS_CLK}.

Parameters ensured by design

8.3 MADC timing diagrams

The interface is fully synchronized to the main clock. The following figure shows the 12 bits conversion timing in case of one tracking and no oversampling. Thus, the maximum speed of the *ADC* is set to 2.5 MSps at 80 MHz clock input. Figure 47 shows the *SAR* ADC timing.

Important: All configuration signals must be stable during a running conversion (between start_adc and one cycle before eoc).

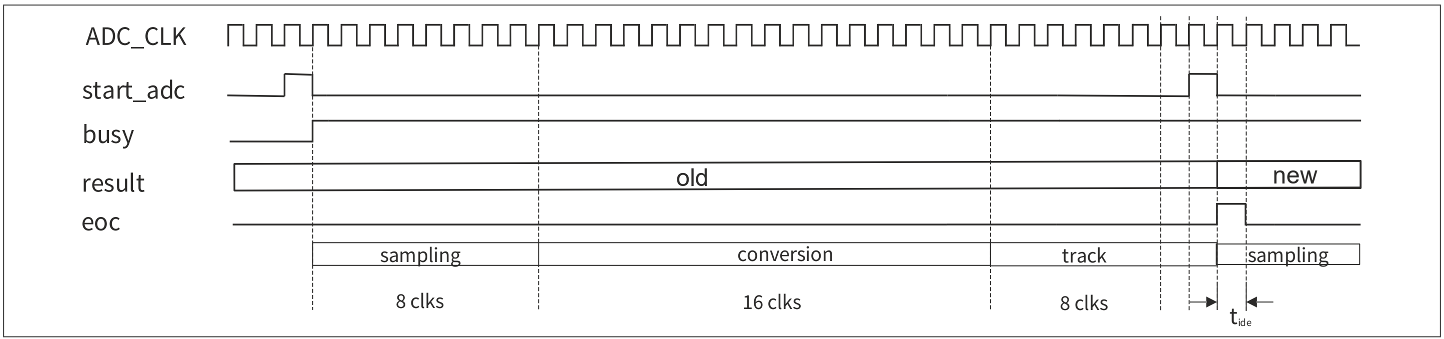

Figure 47 **SAR ADC conversion timing diagram**

8.4 MADC start-up sequence

The following figure shows the start-up sequence for the complete *ADC*.

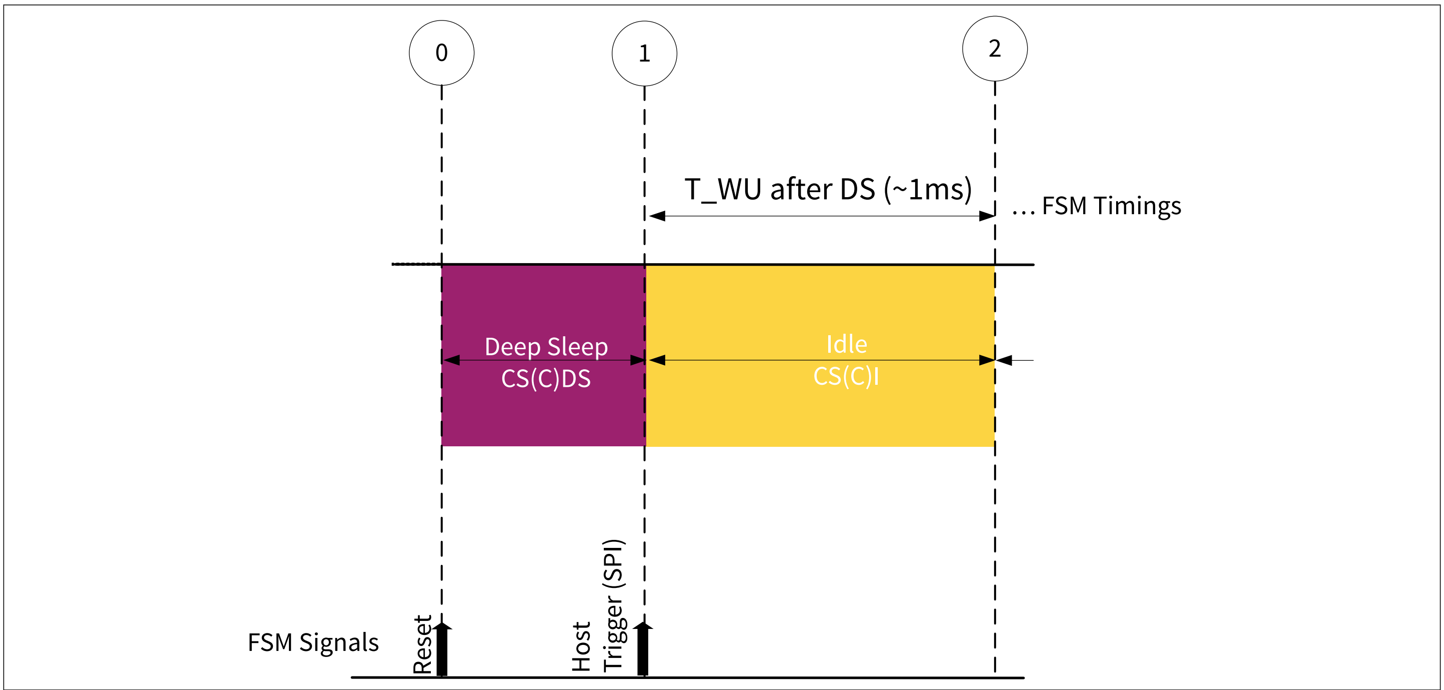

Figure 48 **MADC start-up timing constraints**

After a reset and trigger from the host, the *FSM* will move from the DS power mode into the Idle power mode. Here T_{WKUP} represents the overall time required by the bandgap to settle and it is the longest time required in the settling of the ADC.

Table 39 MADC start-up timing constraints

VDD_A = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C.

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
Wake up time	T_{WUADC}	8.25			µs	@ f_{SYS_CLK}
Setup time common mode input voltage	T_{VCM}			1	µs	
Wake-up time for bandgap and bandgap reference buffer	*T_WU*	300		1000	µs	

8.5 MADC conversion rate

The *ADC* clock input is f_{ADC_CLK}= f_{SYS_CLK} = 76.8/80 MHz and is derived from the system clock.

A conversion can include three different phases:

- Sampling
- Conversion
- Tracking

8.5.1 Sampling

During the first phase, the analog input voltage is sampled onto the input capacitor. The duration is controlled using the ADC0:STC bits (see ADC control register). The following table shows the link between the register value ADC0:STC the clock periods STC_NUM and the sampling time.

Table 40 ADC0:STC value table

ADC0:STC	Sampling clock periods STC_NUM	Sampling time t_{sample} in ns (f_{ADC_CLK} = 80 MHz)
0_D	4	50
1_D	8	100
2_D	16	200
3_D	32	400

The sampling time is calculated as: N_{sample} = STC_NUM.

8.5.2 Conversion

The charge from the sampling capacitor is redistributed to 13 + 2 capacitors. To identify the *least significant bit (LSB)* bits of the result, 13 clock cycles are needed.

To identify the *MSB* bit of the result, one or two clock cycles are used, depending on register setting ADC0:MSB_CTRL (see ADC control register):

- In case of MSB_CTRL is set to 0_B, just a single clock cycle is used (+1)
- In case of MSB_CTRL is set to 1_B, two clock cycles are used (+2)

The redistribution time is calculated as: N_{conv} = (13 + 2 + ADC0:MSB_CTRL) and results in either 16 clock cycles or 17 clock cycles.

8.5.3 Tracking

In this mode, the *ADC* performs a single sample conversion followed by several tracking conversions, depending on the setting of bits ADC0:TRACK_CFG (see ADC control register).

Table 41 ADC0:TRACK_CFG value

ADC0:TRACK_CFG	Additional conversions TRACK_CFG_NUM	Remarks
0_D	0	
1_D	1	Default
2_D	3	
3_D	7	

The duration of one tracking conversion is: N_{track} = 8.
The duration of all tracking conversions for a single result is: N_{track_all} = 8 * TRACK_CFG_NUM.

8.5.4 ADC conversion rate

Based on what is defined in Chapter 8.5.1, Chapter 8.5.2, and Chapter 8.5.3, the following cycles are defined for a single conversion:

$$N_{\mathrm{ADC\_CONV}} = N_{\mathrm{samp}} + N_{\mathrm{conv}} + N_{\mathrm{track\_all}} \tag{20}$$

with N_{samp} the number of sampling, N_{conv} conversion and N_{track} tracking cycles, respectively.
ADC are synchronized to f_{SYS_CLK}.

8.5.5 ADC sampling rate

The *ADC* sampling rate is controlled by the ADC0:ADC_DIV value (see ADC control register). The sampling rate of the ADC is given then by f_{ADC_SAMP}= f_{ADC_CLK}/ADC_DIV. The ADC0:ADC_DIV value needs to be greater than the number of clock cycles needed by a single ADC conversion as described in Chapter 8.5.4.
The sampling rate of the ADC is:

$$f_{\mathrm{ADC\_SAMP}} = f_{\mathrm{ADC\_CLK}} / \mathrm{ADC\_DIV} \tag{21}$$

with ADC_DIV >= N_{ADC_CONV}.

Table 42 ADC Sampling Rate

VDD_A = 1.71 V to 1.89 V, T_b = -20 °C to +70 °C.

Parameter	Symbol	Values			Unit	Condition
		Min.	Typ.	Max.		
ADC sampling rate	f_{ADC_SAMP}	-	2	4	MHz	-
Effective number of bits resolution	*ENOB*	-	10.5	-	Bits	-

9 On chip analog sensor

To measure RF power of TX output and temperature of BGT60UTR11AIP, the chip provides additional sensors. For this the input of the on chip ADC is switched between RX front-end, power sensor and temperature sensor. The conversion time depends on the settings of the ADC programmed in ADC0 register.

During normal operation the switching is done by the FSM without any interaction with the application processor or microcontroller. However, the correct timing and the correct settings must be ensured by the user. Each sensor can be enabled or disabled by programming the corresponding bit fields e.g. CSUx_0:PD_EN for power sensor and e.g. CSDx_0:TEMP_MEAS_EN for temperature sensor.

There is also the option to trigger and read out the on-chip sensors manually when no frame is active. For this the CW mode (see CW mode) can be activated, the required sensor be selected and a conversion be triggered.

9.1 Power sensor

To measure the RF power of TX output in the up chirp the following must be ensured (see #6).

1. 1. CSUx_0:PD_EN = 1_B
2. 2. T_PAEN + T_PSSTART >= 1 µs (switching time)
3. 3. T_PSSTART >= 0.5 µs (PA settling time)
4. 4. T_SSTART >= T_PSSTART + 1 µs + T_CONV (ADC conversion time)

After the conversion, the result is stored in the register Sensor ADC result register.

Anomaly: In some remote cases, due to a timing violation, the power sensor readout may show a 0_D value. 0_D is not a valid value.

Workaround: In that case the sensor result readout should be repeated. Up to 5 times readouts should avoid a wrong value.

9.2 Temperature sensor

To measure the temperature in the up chirp (sawtooth shape) or in the down chirp (triangular shape) following must be ensured.

Triangular shape (see #17)

1. 1. CSDx_0.TEMP_MEAS_EN = 1_B
2. 2. T_START + T_RAMP + T_END >= T_PAEN + T_SSTART + T_ACQx + 1 µs
3. 3. T_EDDMIN >= T_CONV[1)]

After the conversion, the result is stored in the register Sensor ADC result register.

Anomaly: In some remote cases, due to a timing violation, the temperature sensor readout may show a 0_D value. 0_D is not a valid value.

Workaround: In that case the sensor result readout should be repeated. Up to 5 times readouts should avoid a wrong value.

9.3 Manual sensor conversion

To measure the temperature or the RF power manually at any time outside of an active frame, the CW mode) can be used. For this the temperature sensor or power sensor must be enabled and the chip in a corresponding state. While the temperature can be measured in any finite state machine state the RX power can only be measured when the power amplifier is active. For this exact six (TRIG#6) FRAME_START trigger needs to be programmed to get the finite state machine to the state where the PA is active.

1 T_CONV : conversion time of ADC depends on the ADC setting

After the required sensor is selected via ADC1:SENSOR_SEL and triggered with ADC0:TRIG_MADC the sensor result can be read from the SENSOR_RESULT register. If the result is equal to the value 0_D, the sensor measurement procedure must be repeated again as only values different to 0_D are valid results.

A repeated measurement can be performed directly after a sensor reading of SENSOR_RESULT = 0_D by first toggling bit field ADC1:SENSOR_SEL to $0_D$and back to the desired ADC channel (1_D … Power sensor, 2_D … Temperature sensor) followed by a manual ADC trigger via ADC1:TRIG_MADC.

10 Enhanced functions

10.1 CHIP ID readout

Readout sequence:

1. Enable the EFUSE block by setting EFUSE0:EFUSE_EN = 1_B with a single dedicated *SPI* write (see EFUSE register 0)
2. Initiate the sense operation by setting EFUSE0:EFUSE_SENSE = 1_B with a single dedicated SPI write
3. Wait for 2 µs or poll the register field EFUSE1:EFUSE_READY = 1_B (see EFUSE register 1)
4. Read out the device ID from CHIP_ID0 and CHIP_ID1 (see Chip ID register 1 and)
5. Disable the EFUSE block EFUSE0:EFUSE_EN = 0_B

10.2 Data test mode

A *LFSR* is built-in on chip. It will generate a pseudo random bit M-sequence that can be used to fill up the *FIFO*. This module can be used to develop and test the complete pipeline from the FIFO on the BGT60UTR11AIP up to the *AP* memory, including firmware and drivers, with a defined bit sequence. For that the 12-bit ADC1 output data are replaced by the 12-bit generated by the LFSR.

The implemented LFSR is described by the following polynomial: $x^{12}+x^{11}+x^{10}+x^{4}+1$ and starts with the seed 1_D.

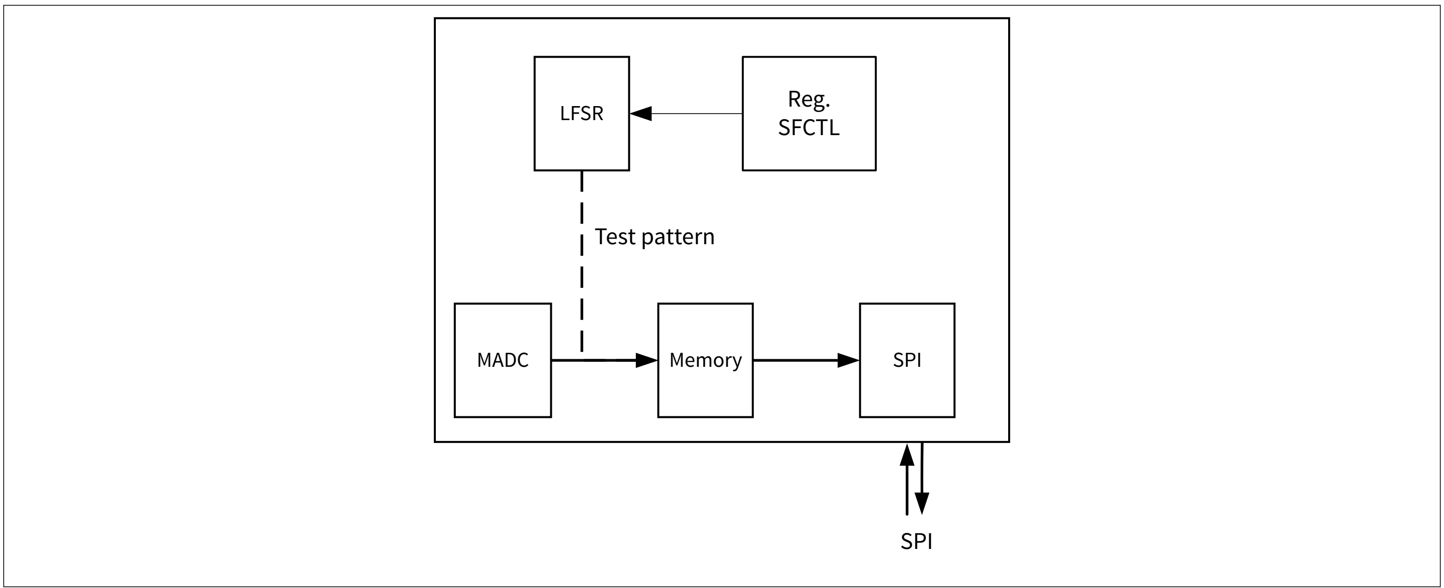

Figure 49 Digital pipeline simplified block diagram

The first *ADC* channel output data stream is bypassed by the data sequence coming from the LFSR generator.

Therefore, only ADC1 output data are replaced by LFSR data.

- Initialization of the LFSR with the start seed via MAIN:FSM_RESET = 1_B (see Main register)
- Enable bit SFCTL:LFSR_EN = 1_B (see SPI and FIFO control register) to activate LFSR and generate the known test data

10.3 CW mode

In the *continuous wave (CW)* mode the device will be set to provide a constant output frequency. During CW mode no shapes are executed.

During the execution of this mode:

- Freq/timing parameters defined in shape registers are ignored

- *PLL* / *RF* / *ADC* runs with values programmed in PLL DFT0 (see PLL test register 0) and CSU1 (see Channel set up x register 1).
- All other CSx / shape settings are not handed over to functional blocks
- The values for REPS/REPC/REPT and frame relevant timings are used to shape a “virtual frame”
- Data from the *FIFO* can be read out following the structure of that “virtual frame”

***Note**: For test purposes the “virtual frame” definition should be kept simple: 1 shape, 1 CS, e.g.*

10.3.1 Enabling the CW mode

The *CW* mode should be preceded by at least a *HW* reset after power up. In case the chip is already up and running a *SW* reset may be used instead.

After this in order to enable the CW mode, the steps below should be followed:

- Enable the MAIN:CW_MODE = 1_B (see Main register)
- Initialize the chip registers according to defined “virtual frame” (settings in Channel set up x register 0 and PLL shape x register 0)
- Enable the clock: PACR1:OSCCLKEN (see PLL analog control register 1)
- Set frequency via PLLx:FSU setting from shape 1
- Set channel set for CSDS/CSI/CSU1 (see Channel set deep sleep register 0)
- set PLL DFT0:byprmpen= 1_B (see PLL test register 0)

By using the FRAME_START as trigger, the chip can be set in the different states of a shape as shown in the following figure.

- TRIG#1: jump to 1 (DS -> Idle)
- TRIG#2: jump to 2 (Idle -> Init0)
- TRIG#3: jump to 3 (Init0 -> Init1)
- TRIG#4: jump to 4
- TRIG#5: jump to 6

Frequency update: at this stage the output frequency can be updated/programed (FSU) to any value and the current frequency will be updated immediately after PLL transition of PDFT0:byprmpen= 0_B -> 1_B.

- TRIG#6: jump to 7

At this stage, the APU number of samples is generated by the *ADC* according to the ADC0 settings. In case if APU = 0_D no triggers are generated, manual triggering of MADC can be done via ADC0:TRIG_MADC. Once the APU number of samples is generated another automatic generation of samples can be done after *FSM* reset.

- TRIG7: jump to 8
- TRIG8: jump to 10
- TRIG9: jump to 11
- TRIGx

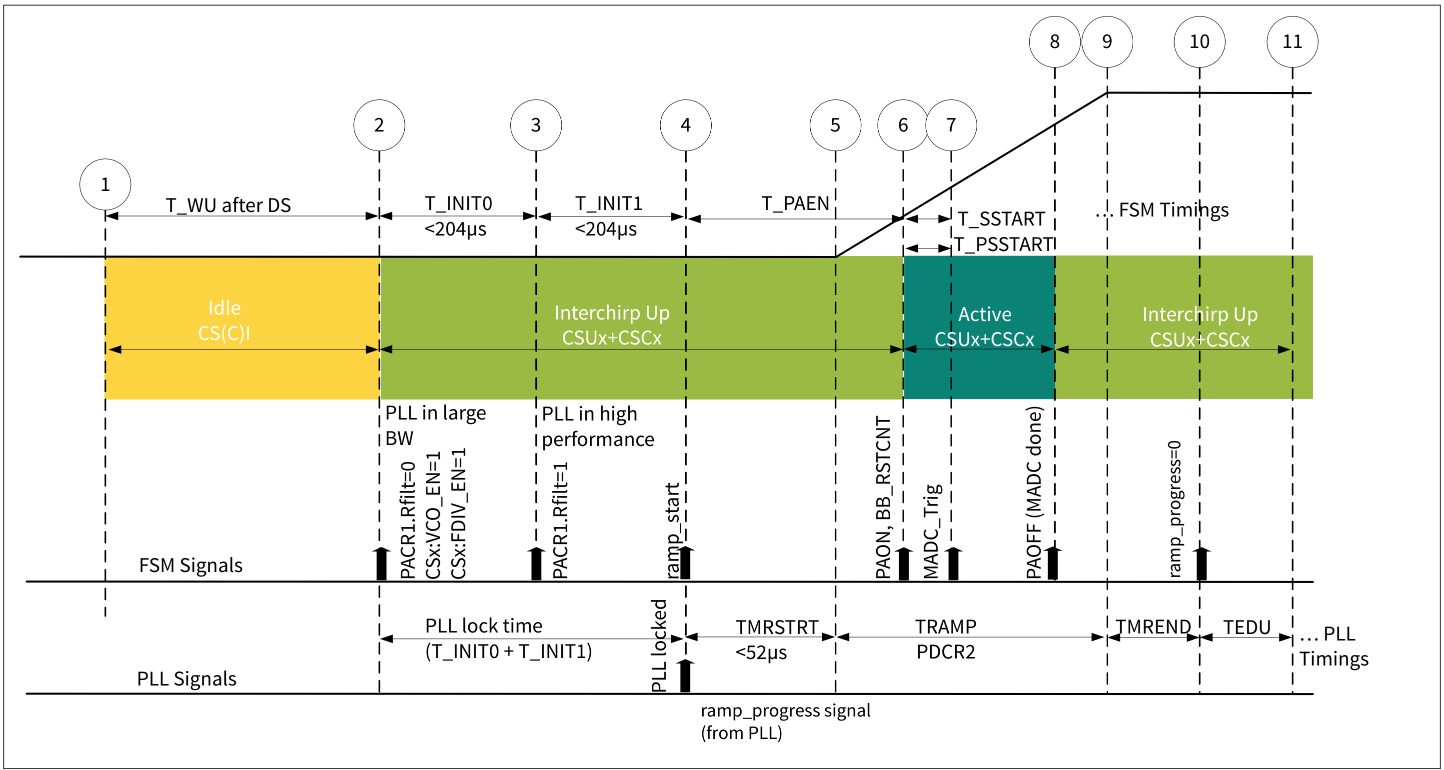

Figure 50 **Steps that can be followed during a "virtual frame"**

The FSM-reset will set back the FSM to initial state to start again with TRIG1.

This specific mode is intended also to test the power consumption of the chip during a specific sequence. It will offer the opportunity to break the expected shape that should be run during the radar (active) mode in static steps where the current consumption can be measured.

10.3.2 Baseband and ADC test mode

A test-tone generator can be used together with the *CW* mode. A test signal source derived from the system clock can be activated in the analog receiver chain; the same in each Rx chain. This test signal can be programmed in the register RFT0 (see RF test register 0). The test tone can propagate through to each baseband chain by enabling a dedicated path. The MADC is triggered by the TRIG7 and will sample the number of samples specified in the APU1 (see PLL shape x register 3). To run a new measurement, an FSM-reset is required.

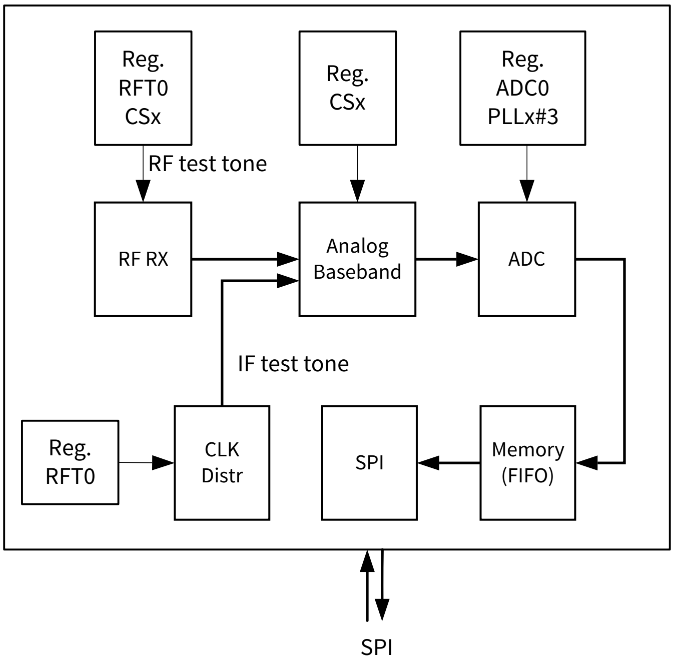

Figure 51 **Baseband/ADC test block diagram**

This feature represents a very convenient way to test and debug a complete system. The customer can program a dedicated frequency, set the baseband gain and cutoff filter of the *HPF* (Channel set up x register 2), set the *ADC*, and readout via *SPI* the sampled data into the *AP* or *MCU* to verify if the complete baseband chain is working as expected.

The following figure shows one example of ADC readout when the baseband is fed with a test tone at 400 kHz internally derived from the OSC_CLK input. Different readouts from different *VGA* settings are reported.

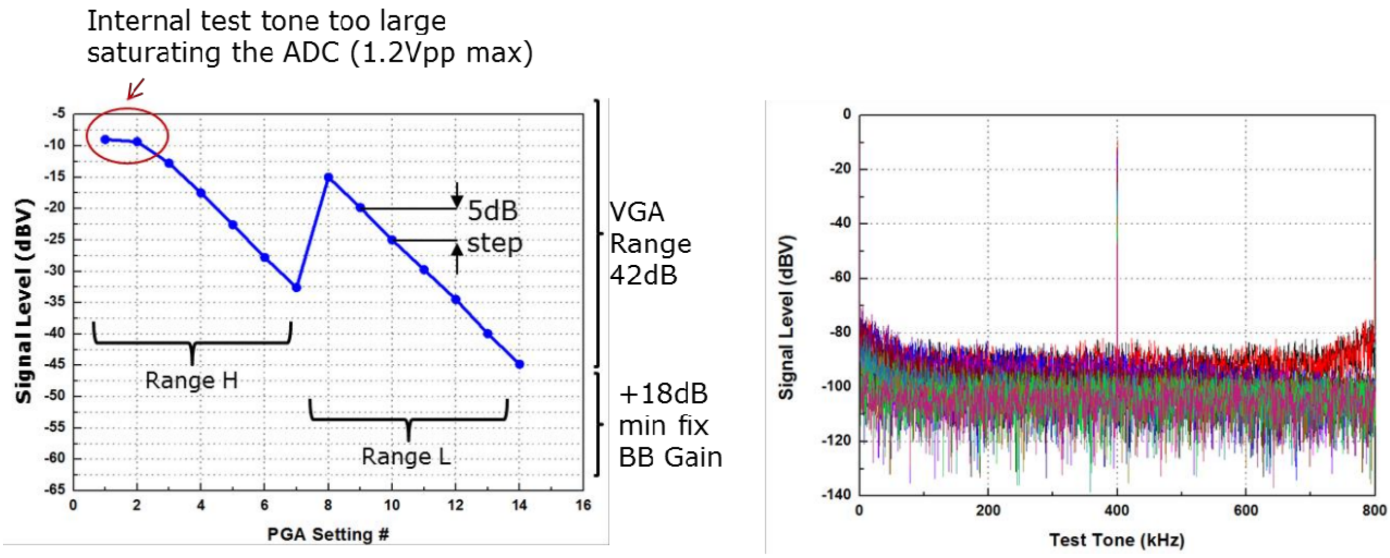

Figure 52 **Example: ADC readout after FFT**

10.4 IRQ output

BGT60UTR11AIP provides one interrupt pin output IRQ. In default mode, the IRQ pin is used to monitor the filling level of the *FIFO* as described below.

IRQ status definition:

- IRQ is high after:
  - CSN goes high and FSTAT:FILL_STATUS >= SFCTL:FIFO_CREF (see SPI and FIFO control register and FIFO status register)
- IRQ is low (as a consequence of):
  - CSN goes high and FSTAT:FILL_STATUS < SFCTL:FIFO_CREF (see also Chapter 4.9 and Chapter 4.48)
  - CSN is active low

The following figure shows the IRQ signal in case of FIFO burst reads.

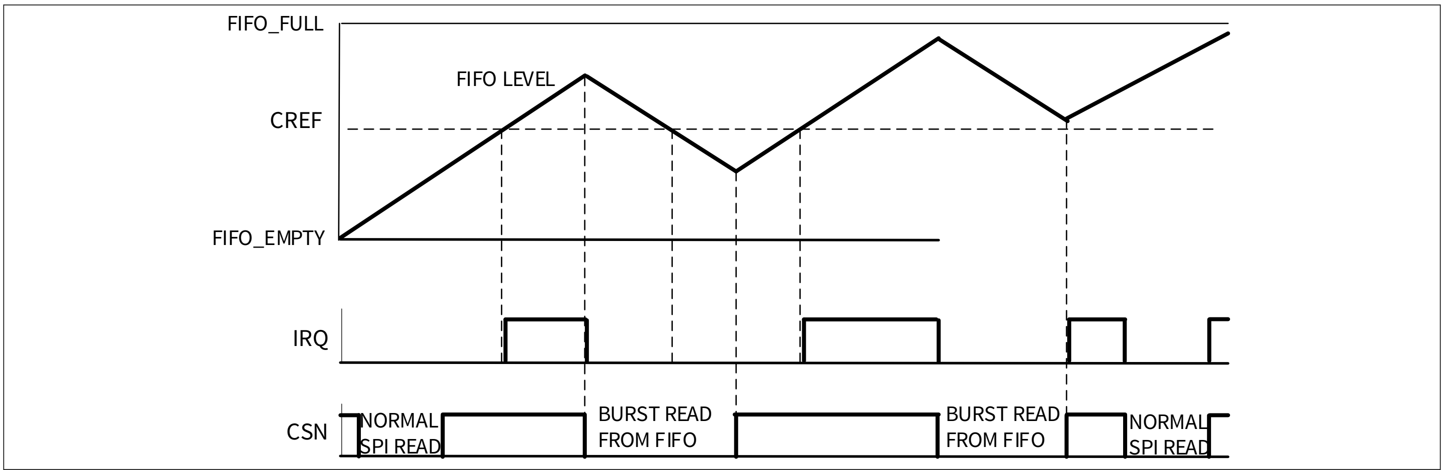

Figure 53 **IRQ status behavior during radar mode with FSM capturing data**

11 Package

The BGT60UTR11AIP chip is housed in a laminate package with solder balls of 300 µm diameter and integrates the antennas. According to IPC/JEDEC's J-STD0, the *moisture sensitivity level (MSL)* is 3. Figure 54 shows the top view of BGT60UTR11AIP package and the distances of antenna patch midpoints. The bottom view is presented in Figure 55. The package size is 4.05 x 4.05 x 0.86 mm^3 with ball pitch of 500 µm. Package outline is reported on Figure 56. Package name: PG-VF2BGA-28-1.

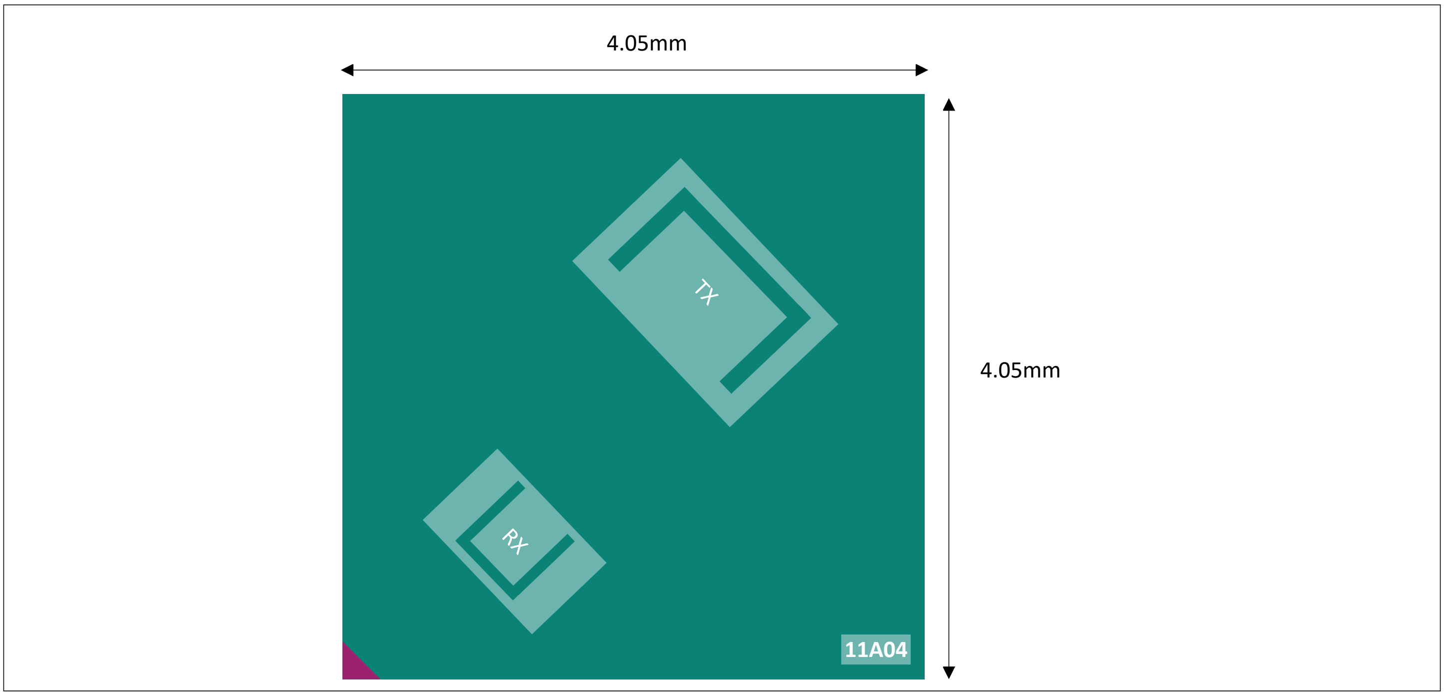

Figure 54 Top view of BGT60UTR11AIP

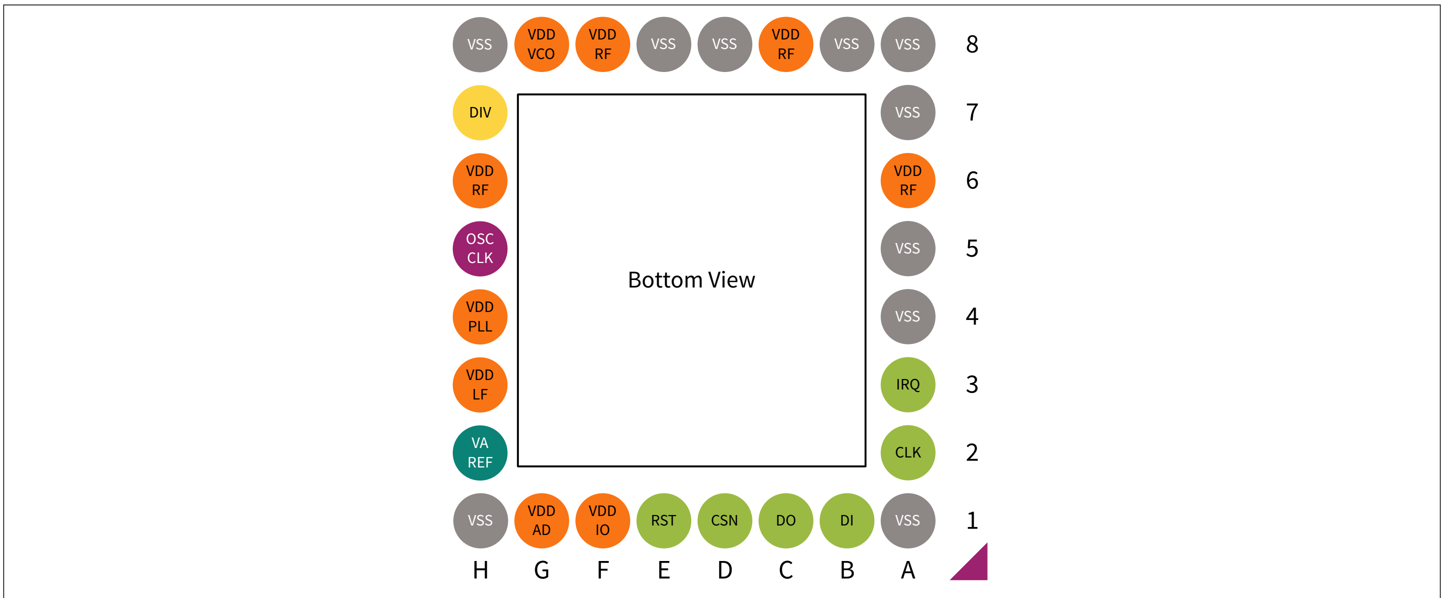

Figure 55 Bottom view of BGT60UTR11AIP

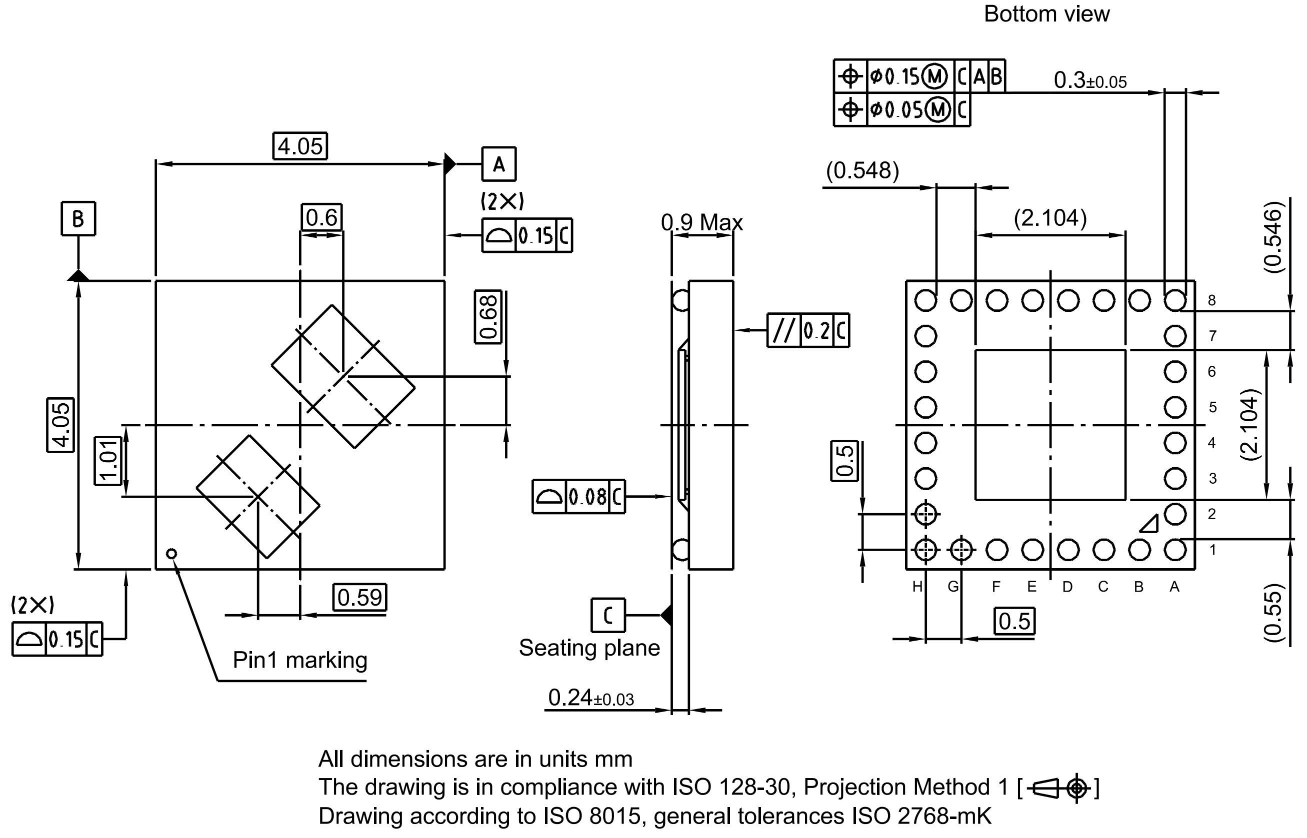

Figure 56 **Package outline PG-VF2BGA-28-1**

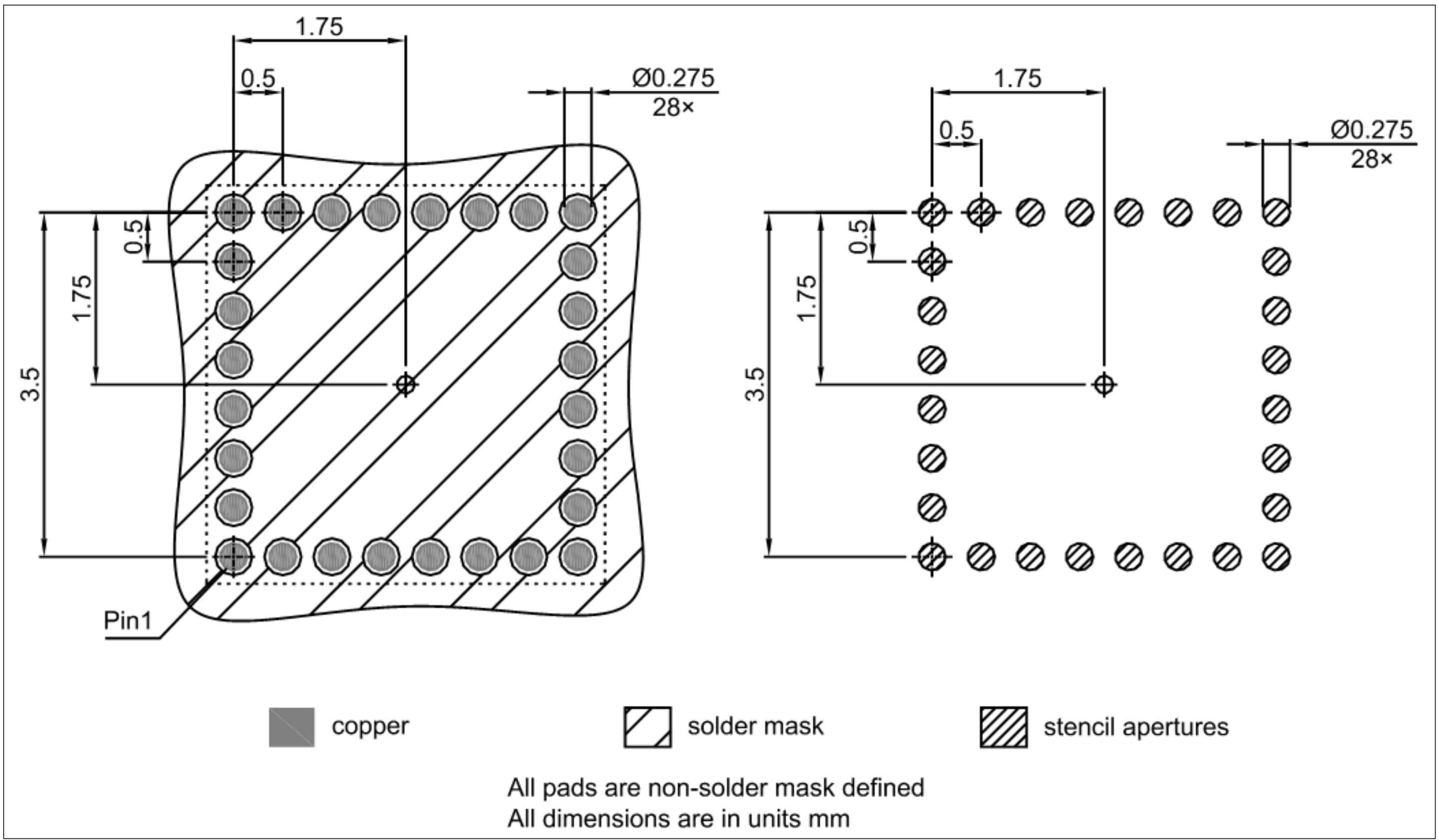

Figure 57 **Footprint of BGT60UTR11AIP**

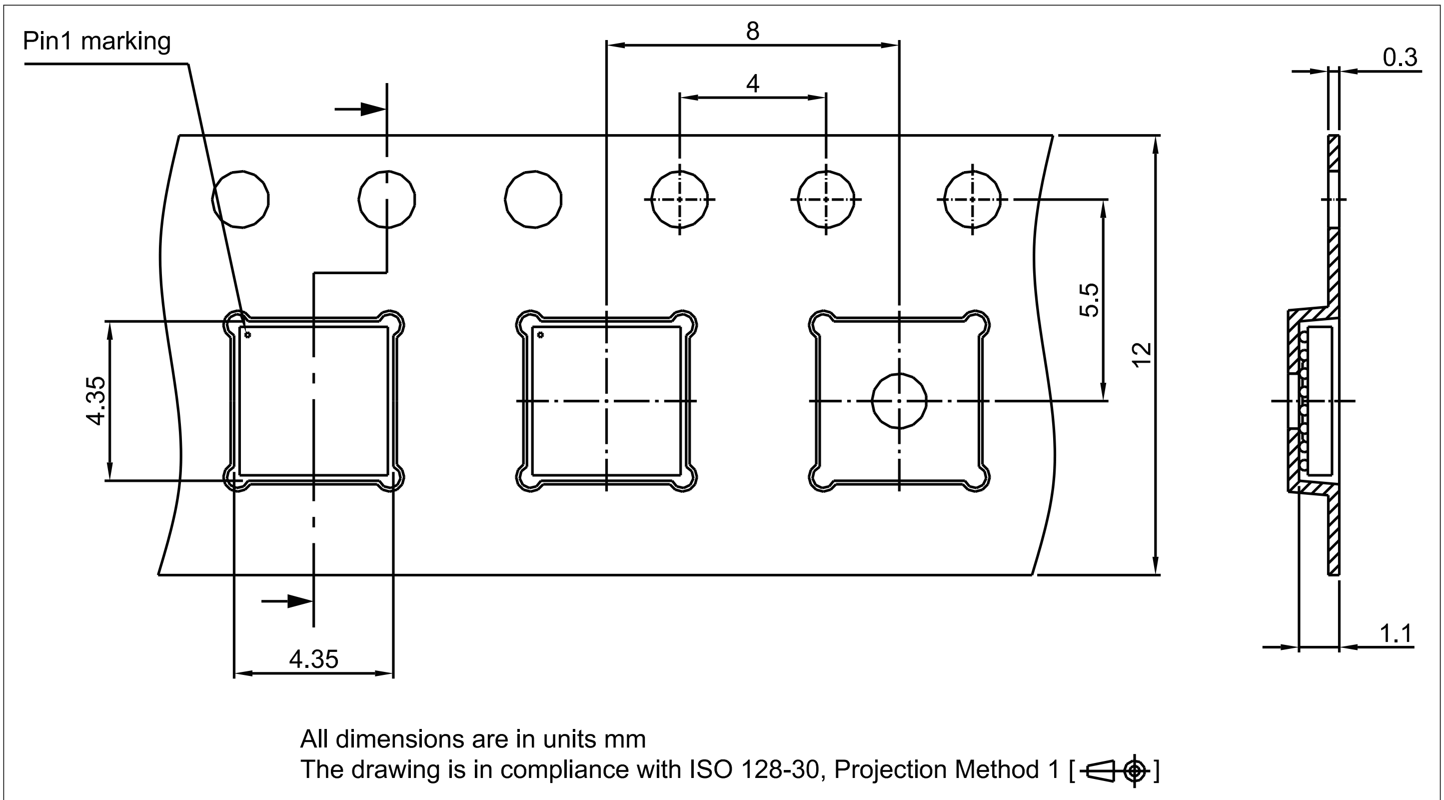

Figure 58 **Tape of PG-VF2BGA-28-1**

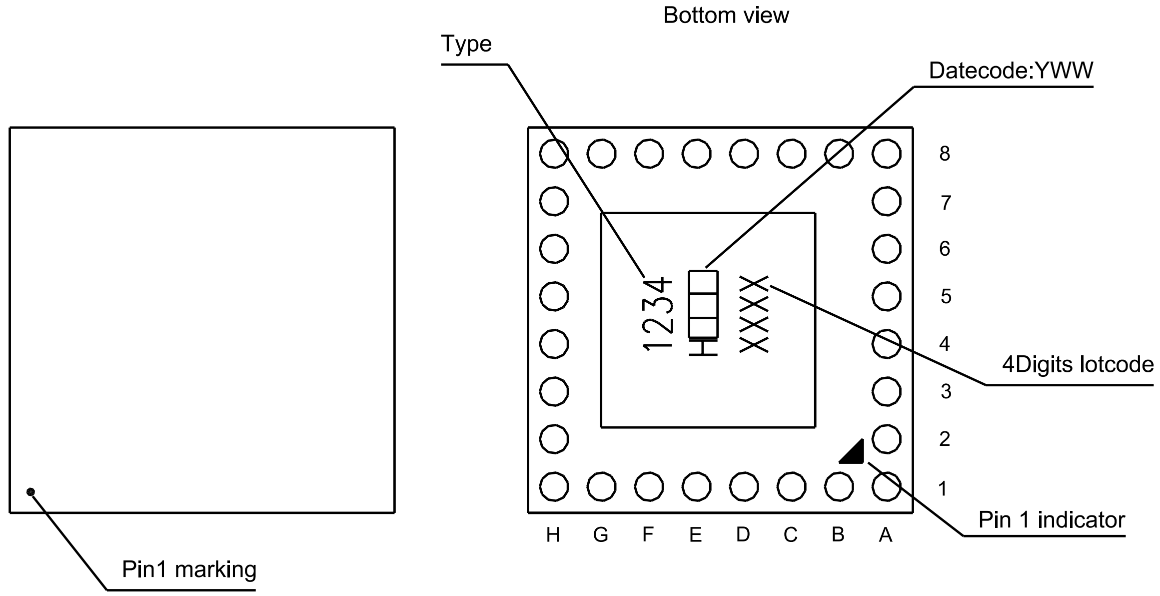

Figure 59 **Marking pattern details BGT60UTR11AIP**

11.1 Built-in antenna specifications

Antenna performance reported in the following table are ensured by design. Typical antenna behavior is measured on Infineon reference board (Hatvan+). Typical antenna beam plots are available in a specific application note and upon specific request.

Table 43 **Antennas in package specifications**

Parameter	Value			Unit	Condition
	Min.	Typ.	Max.		
RX_{BW}	57.4	61	63.0	GHz	Receiver antenna bandwidth
TX_{BW}	57.4	61	63.0	GHz	Transmitter antenna bandwidth
G_{TX}	-	3.0	-	dBi	Antenna gain of a single TX antenna Verified by design
G_{RX}	-	3.0	-	dBi	Antenna gain of a single RX antenna Verified by design

(table continues...)

Table 43 (continued) Antennas in package specifications

Parameter	Value			Unit	Condition
	Min.	Typ.	Max.		
FOV_E	-	120	-	Deg	Field of view of radar mode in the E-plane Verified by design
FOV_H	-	90	-	Deg	Field of view of radar mode in the H-plane Verified by design
ISO_{TX_RX}	-	25	-	dB	Isolation from TX antenna to RX antenna in package.

***Attention**: As of today, it is not possible to test in production the antenna parameters relating to the gain and phase of millimeter-wave antennas integrated into a laminate package. Therefore, deviations of the antenna parameters are not detectable in Infineon's production tests. In addition, the housing of the user's system comprising the Infineon product may impact the antenna parameters. Infineon assumes no responsibility for the compliance of the Infineon product with the antenna parameters. It is the responsibility of the user of the Infineon product to perform an end of line test of user's system which is suitable to detect deviations from the antenna parameters.*

Glossary

AAF

anti-aliasing filter (AAF)

A filter used before a signal sampler to restrict the bandwidth of a signal to satisfy the Nyquist–Shannon sampling theorem over the band of interest.

ABB

analog base band (ABB)

A signal that has a near-zero frequency range, this is, a spectral magnitude that is nonzero only for frequencies in the vicinity of the origin and negligible elsewhere.

AC

alternating current (AC)

A form of power supply in which the flow of electric charge periodically reverses direction.

ADC

analog-to-digital converter (ADC)

A device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

AP

application processor (AP)

A chip that is used to run primary user applications.

BITE

built-in test equipment (BITE)

Passive diagnosis equipment built into a system to support test processes during production.

CDM

charged device model (CDM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD).

CMOS

complementary metal-oxide semiconductor (CMOS)

A technology for constructing integrated circuits that uses a combination of p-channel and n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates.

CW

continuous wave (CW)

The emission of a sinusoidal radio wave, which may be modulated by signals.

DC

direct current (DC)

A form of power supply in which the flow of electric charge is only in one direction.

EOL

end of line (EOL)

The last stage of a production process, where the functional tests are executed.

ESR

equivalent series resistance (ESR)

The internal alternating current resistance that appears in series with an ideal capacitance or an ideal inductance of the device.

FIFO

first in first out (FIFO)

A method for organizing the manipulation of a data structure where the first entry is processed first.

FMCW

frequency-modulated continuous wave (FMCW)

A type of radar system where a known frequency continuous wave radio energy is transmitted and then received from any reflecting object.

FM

frequency-modulated (FM)

A angle modulation in which the instantaneous frequency deviation varies in accordance with a given function, generally linear, of the instantaneous value of the modulating signal.

FSM

finite state machine (FSM)

An abstract machine that can be in exactly one of a finite number of states at any given time.

HBM

human body model (HBM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD) based on a human body.

HPF

high-pass filter (HPF)

An electronic filter that passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency.

HW

hardware (HW)

The collection of physical components that comprise a computer or any other electronic system.

IBIS

Input/output Buffer Information Specification (IBIS)

A specification of a method for integrated circuit (IC) vendors to provide information about the input/output buffers of their product to their prospective customers without revealing the intellectual property of their implementation.

IF

intermediate frequency (IF)

The frequency corresponding to the carrier frequency or another characteristic frequency of an input radio-frequency signal in a signal resulting from each frequency translation.

LDO

low-dropout voltage regulator (LDO)

A direct current linear voltage regulator that can regulate the output voltage even if the supply voltage is very close to the output voltage.

LFSR

linear feedback shift register (LFSR)

A shift register whose input bit is a linear function of its previous state.

LO

local oscillator (LO)

An electronic oscillator used with a mixer to change the frequency of a signal.

LSB

least significant bit (LSB)

The binary digit of the least significance within a code word.

MCU

microcontroller unit (MCU)

A small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals.

MISO

master in slave out (MISO)

The input line of a serial peripheral interface master.

MOSI

master out slave in (MOSI)

The output line of a serial peripheral interface master.

MSB

most significant bit (MSB)

The binary digit of the most significance within a code word.

MSL

moisture sensitivity level (MSL)

An electronic standard for the time period in which a moisture-sensitive device can be exposed to ambient room conditions.

NDA

non-disclosure agreement (NDA)

A legal contract or part of a contract between at least two parties that outlines confidential material, knowledge, or information that the parties wish to share with one another for certain purposes, but wish to restrict access to.

PCB

printed circuit board (PCB)

A board that mechanically supports and electrically connects electronic components using conductive tracks, pads, and other features etched from copper sheets laminated onto a non-conductive substrate.

PLL

phase-locked loop (PLL)

A feedback circuit for synchronizing an oscillator with the phase of an input signal.

RF

radio frequency (RF)

A frequency of a periodic radio wave or of the corresponding electric oscillation.

RSVD

reserved (RSVD)

A placeholder for future functionalities or features.

RX

receiver (RX)

A device that accepts signals from remote transmitters.

SAR

successive approximation register (SAR)

A type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation using a binary search through all possible quantization levels.

SPI

serial peripheral interface (SPI)

A synchronous serial communication interface specification used for inter-chip communication, primarily in embedded systems.

STS

simplified timing shell (STS)

A wrapper around a module that includes timing information to enable static timing checks for this module.

SW

software (SW)

The collection of non-physical components that comprise a set of instructions executed by a processor.

TX

transmitter (TX)

A device that sends out signals.

VCO

voltage controlled oscillator (VCO)

An oscillator whose frequency is a function of the voltage of an input signal.

VGA

variable gain amplifier (VGA)

An electronic amplifier that varies its gain depending on a control voltage.

Revision history

Document version	Date of release	Description of changes
1.0	2023-06-06	Initial datasheet
1.1	2023-08-30	• Updated LPF order from 2nd to 4th • Fixed typo in 'CHIP ID readout' chapter • Updated Register chapter name • Updated introduction chapter • Added package tape figure
1.2	2023-12-15	• Updated antenna in package specification table • Replaced package outline drawing • Updated minimum current consumption value of VDD_{RF} + VDD_{VCO} $RFIdd_{Active}$ • Updated minimum overall current consumption value Idd_{Active}
1.3	2025-02-26	• Changed "Marking" to "Marking type" in ordering information table (cover page) • Added marking layout Figure 59 • Fixed typos

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